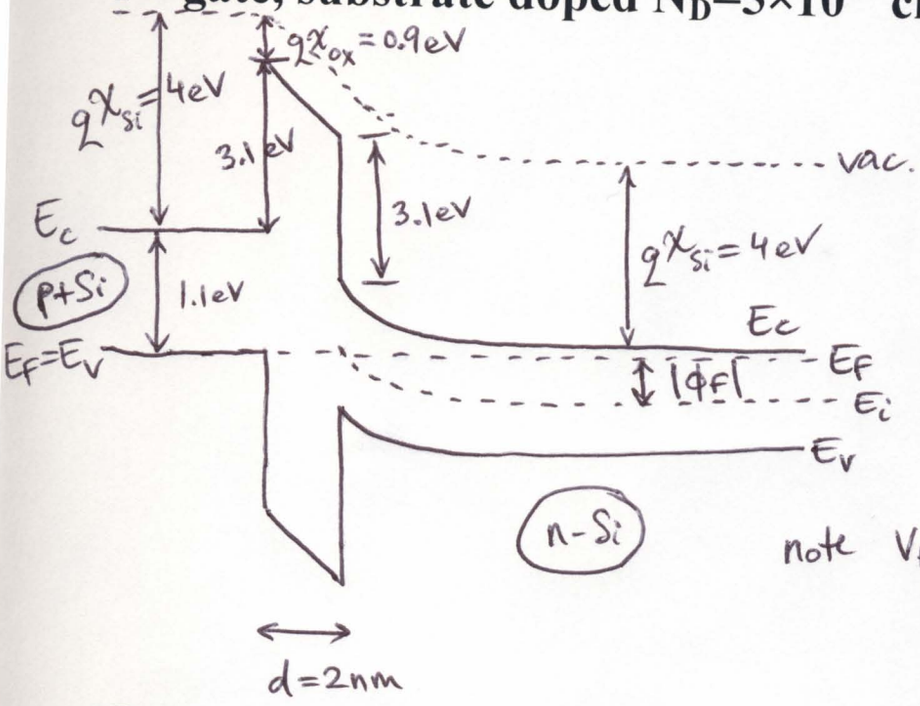
Ex: Plot and label the C-V curve of a PMOS capacitor with P+ gate, substrate doped $N_D = 5\times10^{17}$ cm^{-3}, and SiO_2 d = 2 nm.



$$C_{ox} = \frac{\epsilon_{ox}}{d} = \frac{3.9\times8.854\times10^{-14}\ F/cm}{2\times10^{-7}\ cm}$$

$$C_{ox} = 1.726\times10^{-6}\ F/cm^2$$

$$|\phi_F| = \frac{kT}{q}\ln\frac{N_D}{n_i} \approx 0.45\ V$$

note $V_{FB} > 0 \leftrightarrow$ must "drag down" Fermi level on gate to reach flat bands ($\mathcal{E}=0$)

$$V_{FB} = \frac{1}{q}(\phi_{gate} - \phi_{subs}) = \frac{1}{q}(q\chi_{Si} + E_G) - \frac{1}{q}(q\chi_{Si} + \frac{E_G}{2} - q|\phi_F|)$$

$$= \frac{1}{q}\left(\frac{E_G}{2} + |\phi_F|\right) \approx 0.55\ V + 0.45\ V = \boxed{1\ V}$$

$$V_T = V_{FB} - |2\phi_F| - \frac{1}{C_{ox}}\sqrt{2qN_D\epsilon_{Si}|2\phi_F|} = 1V - 0.9V - \frac{\sqrt{2\times1.6e\text{-}19C\times5e17cm^{-3}\times11.9\times8.854e^{-14}F/cm\times0.9V}}{1.726\times10^{-6}\ F/cm^2}$$

$$\Rightarrow \boxed{V_T = 1V - 0.9V - 0.226V = -0.126\ V}$$

$$\boxed{C_{max} = C_{ox} = 1.726\times10^{-6}\ F/cm^2}$$

$$\boxed{C_{min} = \left(\frac{1}{C_{ox}} + \frac{W_{max}}{\epsilon_{Si}}\right)^{-1} = \left(\frac{1}{C_{ox}} + \frac{2|2\phi_F|}{\sqrt{qN_D\epsilon_{Si}}}\right)^{-1} \approx 1.923\times10^{-7}\ F/cm^2}$$