Metal-semiconductor-metal photodetectors based on graphene/p-type silicon Schottky junctions

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Metal-semiconductor-metal (MSM) photodetectors based on graphene/p-type Si Schottky junctions are fabricated and characterized. Thermionic emission dominates the transport across the junctions above 260 K with a zero-bias barrier height of 0.48 eV. The reverse-bias dependence of the barrier height is found to result mostly from the Fermi level shift in graphene. MSM photodetectors exhibit a responsivity of 0.11 A/W and a normalized photocurrent-to-dark current ratio of 4.55 × 10^4 mW^-1, which are larger than those previously obtained for similar detectors based on carbon nanotubes. These results are important for the integration of transparent, conductive graphene electrodes into existing silicon technologies. © 2013 American Institute of Physics.

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The good electrical conductivity, high optical transparency, mechanical flexibility, and two-dimensional (2D) structure of graphene make it a promising candidate for transparent and conductive electrodes.1–3 In the recent studies, it has been shown that graphene forms a Schottky junction with conventional semiconductors such as GaAs,4 SiC,4,5 GaN,4,6 and Si.4,7–9 In particular, there has been a growing interest in electronic and optoelectronic applications of graphene-silicon Schottky junctions, such as barriers8 and solar cells based on graphene/bulk silicon9,10 and graphene/silicon nanowire11–13 junctions. Unlike conventional metal electrodes, graphene has the advantage that its Fermi level and hence workfunction can be tailored by chemical doping14 or electrostatic gating.15 This property has been utilized recently in device applications such as high efficiency chemically doped solar cells9 and gate-controlled variable Schottky barrier devices.8

Most studies so far have extracted the Schottky barrier height Φb from room temperature I-V measurements. Temperature dependent I-V measurements, on the other hand, would enable the determination of barrier height without any assumptions of the electrically active area or the presence of any interfacial layer.16,17 In addition, in contrast to solar cells, photodetector applications using graphene electrodes are much less explored, and most reports have focused on graphene junctions with n-type Si; p-type Si has been much less studied.

In this letter, we fabricate and characterize metal-semiconductor-metal (MSM) photodetectors where chemical vapor deposition (CVD)-grown monolayer graphene plays the role of the metal and the semiconductor is p-type silicon (p-Si). In order to understand the operation of these MSM photodetectors, we first investigate the electronic properties of graphene/p-Si Schottky junctions using metal-semiconductor (MS) structures as a function of temperature. With temperature-dependent I-V measurements, we also investigate the reverse-bias dependence of the Schottky barrier height. Finally, we characterize the photoreponse of interdigitated finger MSM photodetectors based on graphene/p-Si Schottky junctions. Our results provide important insights for the future integration of graphene based materials into existing semiconductor technologies.

Figure 1 shows a schematic of the fabrication process flow for the graphene/p-Si MSM photodetectors. A 1 mil copper foil (∼25 μm thick, 99.8% pure) was first cleaned and annealed at 1000 °C in a CVD chamber. Graphene was then grown on the foil at the same temperature under the flow of 100 sccm CH4 and 50 sccm H2 at a pressure of 400 mTorr (Refs. 2, 3, 18, and 19) [Fig. 1(a)]. After growth, poly(methyl methacrylate) (PMMA) was deposited on top of graphene, followed by etching of the copper foil in FeCl3 [Fig. 1(b)]. Si substrates with a p-type doping of ∼3 × 10^16 cm^-3 and a 300 nm thermally grown SiO2 layer on top were cleaned [Fig. 1(c)] and windows were opened in the oxide layer [Fig. 1(d)]. Graphene was then transferred onto the patterned Si/SiO2 substrates and the PMMA layer was removed. The Raman spectrum of graphene transferred onto SiO2 measured at a laser wavelength of 632 nm is shown in Fig. 1(f), depicting the locations and relative intensities of the D, G, and 2D peaks. The strong G peak and the weak D peak indicate good graphic quality, and the large 2D to G peak intensity ratio (I2D/I_G > 2) confirm the monolayer nature of the CVD-grown graphene.20,21 The full width at half maximum (FWHM) of the G, 2D, and D peaks for the transferred graphene calculated from Fig. 1(f) are 17.7, 35.3, and 14.8 cm^-1, respectively, which are in good agreement with the values reported in the previous studies on monolayer graphene.15,22,23 Furthermore, we found that the Raman spectrum does not change significantly after device fabrication in the center of the patterned fingers. Only at the edges of the fingers, a larger D-peak is observed due to the presence of edge defects and dangling bonds, consistent with the previous Raman studies on patterned graphene nanoribbons.24–26

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of the junction between graphene and p-Si through thermionic emission at temperatures above 260 K, which in turn transports in the graphene/p-Si interface. The reverse saturation current suggests that the electronic temperature dependence of the low forward-bias current and temperature-dependent exponential slopes are visible. The range is shown in the upper inset of Fig. 2(a), where the Schottky barrier height can be obtained, as shown in Fig. 2(c).

The Schottky barrier height can be extracted from the slope of the Richardson plot ($\log (I/T^2)$ vs. $1/T$) of the reverse saturation current in the temperature region dominated by thermionic emission, as shown in Fig. 2(b). The figure shows the Richardson plot at a reverse bias of 2 V and the linear best-fit, from which the barrier height $\Phi_B$ is extracted to be 0.46 eV. Furthermore, by performing the barrier height extraction at various reverse bias values in the saturation region, the reverse bias dependence of the Schottky barrier height can be obtained, as shown in Fig. 2(c).

There are two main factors which could contribute to the reverse bias dependence of the Schottky barrier height.
FIG. 2. (a) Current-voltage characteristics for a graphene/p-Si Schottky junction with 2.5 × 10^11 cm^-2 area at various temperatures ranging from 260 K to 380 K. The upper inset depicts a magnified view of the low forward-bias region of the same I-V characteristics as in the main panel. The lower inset is an Arrhenius plot of the reverse saturation current at 2 V bias in the temperature range 95 K to 380 K for the same device as in the main panel, which shows the transition from thermionic emission to tunneling transport. (b) The experimental Richardson plot (log I/V^2 vs. 1/T) for the device in part (a) at a reverse bias of 2 V in the thermionic emission dominated temperature range and the linear best-fit, which yields the Schottky barrier height. (c) The experimentally extracted Schottky barrier height Φ_b (left y-axis) and the calculated change in the Schottky barrier height due to the Fermi level shift in graphene δΦ_b in the Schottky barrier height due to the Fermi level shift in graphene with reverse bias is then given by

$$E_F(V_R) = -h\nu_F \sqrt{\pi |n_0|},$$

where $h$ is the reduced Planck constant, $\nu_F = 1.1 \times 10^8$ cm/s is the Fermi velocity of graphene, and the carrier concentration $n_0$ is defined to be positive for holes and negative for electrons. Once the graphene/p-Si junction is formed, a space charge $Q_s$ (per unit area) forms in the depletion region of Si given under the depletion approximation by

$$Q_s = -qN_Ax_d = -\sqrt{2e_0\epsilon NA(V_{bi} + V_R)},$$

where $N_A$ is the acceptor density, $x_d$ is the depletion region width, $\epsilon$ is the permittivity of silicon, $V_{bi}$ is the built-in voltage, and $V_R$ is the magnitude of reverse bias. $V_{bi}$ is given by

$$qV_{bi} = \Phi_0^0 - (E_{FSi} - E_F),$$

where $\Phi_0^0$ is the zero-bias barrier height, and $E_{FSi}$ and $E_F$ denote the Fermi level and the valence band of Si, respectively, as shown in the thermal equilibrium band diagram of Fig. 3(a). Neglecting any interface state charges, an equal and opposite charge $Q_G$ develops on the graphene side, i.e., $Q_G = -Q_s$. This charge induces additional holes and makes the new carrier density $n$ in graphene $n = n_0 + Q_G/q$, neglecting any thermally generated carriers. Replacing $n_0$ in Eq. (2) with this new $n$, and using the expression for $Q_s$ in Eq. (3), the total Fermi level shift in graphene relative to the Dirac point now becomes reverse-bias dependent, i.e.,

$$E_F(V_R) = -h\nu_F \sqrt{\pi (|n_0| + \sqrt{2e_0\epsilon NA(V_{bi} + V_R)/q}),}$$

The expression in Eq. (4) includes the Fermi level shift due to extrinsic doping, thermal equilibrium contact with Si, and reverse bias. Assuming an ideal Schottky junction where surface-state effects are neglected, the corresponding change $\delta\Phi_b$ in the Schottky barrier height due to the Fermi level shift in graphene with reverse bias is then given by

$$\delta\Phi_b(V_R) = \Phi_b(V_R) - \Phi_b^0 = E_F(V_R) - E_F^0,$$

where $E_F^0$ is the zero-bias graphene Fermi-level shift [i.e., $E_F(V_B = 0)$]. Note that, in the case of a graphene junction with p-Si, the decrease in $E_F$ of graphene with increasing reverse bias decreases $\Phi_b$ as shown in Fig. 3(b), i.e., $\delta\Phi_b$ is negative. The opposite would be true for n-type Si.

We can calculate and plot $\delta\Phi_b$ as a function of $V_R$ using Eqs. (4) and (5), as shown in Fig. 2(c) along with the experimental $\Phi_b$ vs. $V_R$ curve. Since $V_{bi}$ in Eq. (4) depends on $\Phi_b^0$, a self-consistent calculation was performed by iteration in order to find $V_{bi}$. Since $\Phi_b$ vs. $V_B$ and $\Phi_b$ vs. $V_R$ curves in Fig. 2(c) exhibit relatively similar slopes, we can conclude that most of the contribution to the reverse bias dependence of $\Phi_b$ comes from the Fermi level shift in graphene.

FIG. 3. Energy band diagram of the graphene/p-Si Schottky junction (a) at thermal equilibrium and (b) under reverse bias $V_B$. $E_{vac}$ is the vacuum level, $E_C$, $E_E$, $E_{i0}$, and $E_i$ are the electron affinity, conduction band, bandgap, Fermi level, and valence band of Si, respectively. Furthermore, $V_{bi}$ is the built-in voltage, $\Phi_0$ is the workfunction of intrinsic graphene, $E_F$ is the graphene Fermi-level shift, and $\Phi_b$ is the Schottky barrier height. The superscripts “0” in part (a) denote thermal equilibrium (i.e., zero-bias) values. Note that the graphene Fermi level shifts further down relative to the Dirac point under reverse bias, decreasing $\Phi_b$.
Furthermore, the slightly larger slope of the $\Phi_B$ vs. $V_R$ curve indicates that there could also be a contribution from image-force barrier lowering. This is different from Schottky junctions with conventional metals in which the Fermi level is fixed and the reverse bias dependence of barrier height is primarily due to image force lowering. Extrapolating the experimental data to zero-bias using Eqs. (4) and (5), we obtain $E_F^0 = -0.25$ eV and a zero-bias barrier height of $\Phi_B^0 = 0.48$ eV. Furthermore, the workfunction of intrinsic (i.e., $E_F = 0$) graphene $\Phi_g$ can be calculated from $\Phi_g = [E_F^0] + \Phi_B^0 = \chi + E_{Si}$, where $\gamma$ and $E_{Si}$ are the electron affinity and band gap, respectively, of Si, as shown in Fig. 3. By using the extracted values of $E_F^0$ and $\Phi_B^0$, we obtain $\Phi_g = 4.45$ eV, which is in good agreement with the values reported in the literature. Previous studies have suggested that charge puddles could form after transferring graphene onto SiO$_2$ substrates. Therefore, the extracted barrier height is an “effective” value over the contact area.

With the extracted Schottky barrier height, we find that the calculated reverse saturation current levels from Eq. (1) are significantly higher than the experimental data. This difference in the measured and calculated current levels could be explained by the presence of a thin interfacial native oxide layer between graphene and Si, which lowers the current by introducing quantum tunneling. The interfacial native oxide layer could grow during the time between the etching of the thermal oxide and the graphene transfer as the Si substrate is exposed to air. We found that devices fabricated with an additional HF cleaning step immediately prior to graphene transfer also exhibited this lower current, indicating that the native oxide could also grow during the graphene transfer process since it involves wet chemical processing in H$_2$O. Another possibility is that oxygen molecules could diffuse through holes or cracks in the graphene after deposition and form the native oxide at the silicon surface. Recently, it was shown that a native oxide layer is beneficial to the performance of graphene/Si Schottky junction solar cells, which was attributed to surface passivation effects. In the case of MSM photodetectors, the interfacial native oxide layer acts as a tunnel barrier and helps reduce the dark current and increase the sensitivity. An interfacial oxide layer has been intentionally introduced previously in conventional Aluminum-Silicon MSM photodetectors to minimize the dark current.

The effect of carrier tunneling through the thin interfacial oxide layer can be incorporated into Eq. (1) as an exponential prefactor $\exp(-\gamma^{0.5}\delta_t)$, where $\delta_t$ is the thickness of the thin native oxide layer and $\gamma$ is the effective tunneling barrier height of the oxide (which also depends on $\delta_t$) as

$$I = AA^{*+}T^2 \exp(-\gamma^{0.5}\delta_t) \exp\left(-\frac{\Phi_B}{kT}\right) \left[\exp\left(\frac{qV}{nkT}\right) - 1\right].$$

By comparing the experimental and theoretically calculated current values, the tunneling factor is estimated as $\gamma^{0.5}\delta_t \approx 8.23-8.95$ eV$^{0.5}$ Å depending on the reverse bias chosen, corresponding to an oxide thickness $\delta_t$ between 1.9 and 2.6 nm. It is worth noting that extracting $\Phi_B$ using the Richardson plot was critical in obtaining the value of $\gamma^{0.5}\delta_t$, since values of $\Phi_B$ and $\gamma^{0.5}\delta_t$ cannot be obtained independently at a fixed temperature.

After the analysis of the electronic properties of reverse-biased graphene/p-Si junctions, we turn to characterize the device performance of graphene/p-Si graphene MSM photodetectors based on these junctions. The inset of Fig. 4 shows the dark I-V characteristics at room temperature for the graphene/p-Si MSM structure in the bias range from −3 V to 3 V, which shows the typical characteristics expected for two back-to-back Schottky diodes. The dark I-V characteristics in the figure are symmetric, suggesting that the Schottky junctions formed at different graphene fingers are uniform.

To characterize the photoresponse of the graphene/p-Si MSM photodetectors, they were illuminated with a He-Ne laser (633 nm wavelength, 5.1 mW power, and ~830 μm spot size) at room temperature. The main panel of Fig. 4 shows the dark and photocurrent of the same MSM device as in the inset as a function of voltage bias up to 5 V. As we can see from the figure, the device current increases by close to five orders of magnitude at 5 V bias under laser illumination. An important performance metric for MSM photodetectors is the normalized photocurrent-to-dark current ratio (NPDR) defined as

$$NPDR = \frac{I_{photo}/I_{dark}}{P_{inc}} = \frac{\gamma}{I_{photo}/P_{inc}},$$

where $I_{photo}$ and $I_{dark}$ are the photo and dark current, respectively, $P_{inc}$ is the incident optical power, and $\gamma$ is the responsivity given by $\gamma = I_{photo}/P_{inc}$. Responsivity and NPDR values at 5 V are 0.11 A/W and 4.55 × 10$^4$ mW$^{-1}$, respectively. This NPDR value is larger than those reported for carbon nanotube film-Si MSM photodetectors due to the lower dark current. It can also be observed in Fig. 4 that the photocurrent increases with increasing bias, which could be due to defects at the graphene/p-Si interface.38

![FIG. 4. Dark current and photocurrent as a function of bias voltage measured at room temperature for a graphene/p-Si MSM photodetector with finger width $W = 10$ μm, finger spacing $S = 10$ μm, active area feature length $FL = 400$ μm, and active area feature width $FW = 400$ μm. The photocurrent is measured under 633 nm He-Ne laser illumination with 5.1 mW power and ~830 μm spot size. The inset shows the dark I-V characteristics for the same device as in the main panel.](image-url)
It is also worth noting that the series resistances of the MSM devices do not limit the photocurrent even at the highest voltage bias measured. The contact resistance between the Ti/Au metal electrode and graphene dominates the total series resistance. Based on the contact resistivity obtained from four-point and two-point measurements of graphene patterned into four-point-probe structures, the series resistance of the device in the main panel of Fig. 4 is more than 20 times smaller than the measured MSM device resistance even under laser illumination at 5 V.

In conclusion, we fabricated and characterized CVD-grown monolayer graphene/p-Si MSM photodetectors as well as MS Schottky junctions. The reverse-bias dependence of the Schottky barrier height, which is extracted from Richardson plots, is found to result mainly from the Fermi level shift the Schottky barrier height, which is extracted from Richardas MS Schottky junctions. The reverse-bias dependence of the device in the main panel of Fig. 4 is more than 20 times smaller than the measured MS Schottky junctions. The reverse-bias dependence of the Schottky barrier height, which is extracted from Richardson plots, is found to result mainly from the Fermi level shift. In addition, comparison of the experimental and theoretically calculated reverse saturation current values suggests the presence of a thin interfacial native oxide layer between graphene and Si. Finally, we studied the photoresponse of the MSM photodetectors under laser illumination and extracted the responsivity and NPDR values. Although further research is needed to understand and control the microscopic properties of the interface between graphene and Si, graphene holds promise as a transparent, conductive electrode that can be integrated with existing silicon technologies.

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