Correction to Improved Contacts to MoS$_2$ Transistors by Ultra-High Vacuum Metal Deposition

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Additional text is required to explain the relationship between Figure 5a and 5b. The revised caption of Figure 5b, shown below, contains the new text:

Figure 5: (b) $I_D$ vs $V_D$ for the smallest device measured ($L_C \approx 20$ nm) showing $I_D > 300 \mu A/\mu m$, a record for a TMD FET at $\sim 70$ nm contact pitch. The data in Figure 5a and 5b were obtained before and after a reduction in threshold voltage from $V_T \approx 2V$ to $-2V$, respectively, after device stress up to $V_D = 3V$. The device was stable before and after this point, as shown by dual forward–backward sweeps revealing minimal hysteresis.

The analysis and conclusions of our work remain unaffected.

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