Mobility and saturation velocity in graphene on SiO_2

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(Received 15 May 2010; accepted 3 August 2010; published online 27 August 2010; publisher error corrected 31 August 2010)

We examine mobility and saturation velocity in graphene on SiO_2 above room temperature (300–500 K) and at high fields (~ 1 V/μm). Data are analyzed with practical models including gated carriers, thermal generation, "puddle" charge, and Joule heating. Both mobility and saturation velocity decrease with rising temperature above 300 K, and with rising carrier density above 2×10^{12} cm^{-2}. Saturation velocity is $>3\times10^{7}$ cm/s at low carrier density, and remains greater than in Si up to 1.2×10^{13} cm^{-2}. Transport appears primarily limited by the SiO_2 substrate but results suggest intrinsic graphene saturation velocity could be more than twice that observed here. © *2010 American Institute of Physics*. [doi:10.1063/1.3483130]

The excellent electrical and thermal properties of graphene hold great promise for applications in future integrated-circuit technology.[1] For instance, the electron and hole energy bands are symmetric,[1,2] leading to equal and high electron and hole mobilities, unlike in typical semiconductors like Si, Ge, or GaAs where hole mobility is lower. However, despite many measurements at low fields and low temperatures,[3] surprisingly little data or models exist for transport in graphene at temperatures and high electric fields typical of modern transistors.

In this study we measure mobility in the $T=300-500$ K range and velocity saturation at fields $F\sim 1$ V/μm in monolayer graphene on SiO_2, both as a function of carrier density. We also introduce simple models including proper electrostatics, and self-heating[4] at high fields. We find that mobility and saturation velocity decrease with rising temperature above 300 K, and with rising carrier density above 2×10^{12} cm^{-2}, and appear limited by the SiO_2 substrate. The relatively straightforward approach presented can be used for device simulations or extended to graphene on other substrates.

We fabricated four-probe graphene structures on SiO_2 with a highly doped Si substrate as the back-gate [Fig. 1(a) and Ref. 5]. To obtain mobility and drift velocity from conductivity measurements, we model the carrier density including gate-induced (n_{cv}), thermally generated (n_{th}) carriers, electrostatic spatial inhomogeneity (n^*) and self-heating at high fields. Previous mobility estimates using only n_{cv} could lead to unphysically high mobility ($\mu\rightarrow\infty$) near the Dirac voltage ($V_G=V_0$) at the minimum conductivity point.

First, we note the gate voltage imposes a charge balance relationship as

$$n_{cv}=p-n=-C_{ox}V_{G0}/q, \tag{1}$$

where $C_{ox}=\varepsilon_{ox}/t_{ox}$ is the capacitance per unit area (quantum capacitance can be neglected here[6,7]), ε_{ox} is the dielectric constant of SiO_2, q is the elementary charge, and $V_{G0}=V_G-V_0$ is the gate voltage referenced to the minimum conductivity point. Then, we define an average Fermi level E_F such that $\eta=E_F/k_BT$, leading to the mass-action law,[6]

$$pn=n_{th}^2\frac{\mathfrak{I}_1(\eta)\mathfrak{I}_1(-\eta)}{\mathfrak{I}_1^2(0)}, \tag{2}$$

where $n_{th}=(\pi/6)(k_BT/\hbar v_F)^2$ is the thermal carrier density, $v_F\approx10^8$ cm/s is the Fermi velocity, and $\mathfrak{I}_j(\eta)$ is the Fermi–Dirac integral, $\mathfrak{I}_1(0)=\pi^2/12$.

Next, we account for the spatial charge ("puddle") inhomogeneity of graphene due to substrate impurities.[8,9] The puddle surface potential can be approximated[7] as a periodic step function with amplitude $\pm\Delta$ related to the width of the minimum conductivity plateau,[5,10] as given by the residual carrier puddle density (n^*) due to charged impurities in the SiO_2 (n_{imp}). We find $n^*\approx0.297n_{imp}\approx2.63\times10^{11}$ cm^{-2} here,[5] i.e., a surface potential variation $\Delta\approx59$ meV. This is similar to a previous study (~54 meV),[7] to scanning tunneling microscopy results (~77 meV),[9] and this translates into a Dirac voltage variation $\Delta V_0=qn^*/C_{ox}\approx3.66$ V.

The total carrier density can be determined numerically by averaging Eqs. (1) and (2) for the regions of $\pm\Delta$, but does not yield an analytic expression. In order to simplify this, we note that at low charge density ($\eta\rightarrow0$) the factor $\mathfrak{I}_1(\eta)\mathfrak{I}_1(-\eta)/\mathfrak{I}_1^2(0)$ in Eq. (2) approaches unity. At large $|V_{G0}|$ the gate-induced charge dominates, i.e., $n_{cv}\gg n_{th}$ when

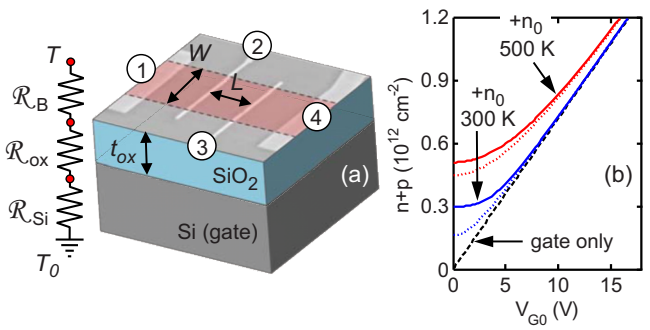

FIG. 1. (Color online) (a) Schematic of a graphene sample ($W=7$ μm, $L=4$ μm, and $t_{ox}=300$ nm) connected to four-probe electrodes; graphene colorized for clarity. Thermal resistance model is used to calculate average temperature rise at high bias. (b) Calculated carrier density vs. gate voltage at 300 K and 500 K in electron-doped regime ($n>p$). Solid lines include contribution from electrostatic inhomogeneity n^* and thermal carriers n_{th} (both relevant at 300 K), dotted lines include only n_{th} (dominant at 500 K). Dashed line shows only contribution from gating, n_{cv}.

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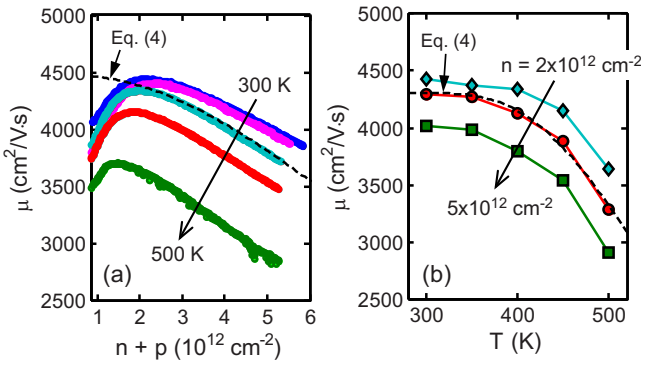

FIG. 2. (Color online) (a) Mobility vs. carrier density in the electron-doped regime ($V_{G0}>0$, $n>p$), obtained from conductivity measurements at $T=300-500$ K, in 50 K intervals. The qualitative dependence on charge density is similar to that found in carbon nanotubes, see Ref. 22. Dashed line shows fit of Eq. (4) with $T=400$ K (also see Ref. 14). (b) Mobility vs. temperature at $n=2\times10^{12}$ (top), 3.5×10^{12} (middle), and 5×10^{12} cm^{-2} (bottom). Dashed line shows fit of Eq. (4) with $n=3.5\times10^{12}$ cm^{-2}.

$\eta \gg 1$. Finally, we add a correction for the spatial charge inhomogeneity which gives a minimum carrier density $n_0=[(n^*/2)^2+n_{th}^2]^{1/2}$ resulting from averaging the regions of $\pm\Delta$. Solving Eqs. (1) and (2) above with these approximations results in an *explicit* expression for the concentration of electrons and holes, as follows:

$$n,p \approx \tfrac{1}{2}[\pm n_{cv} + \sqrt{n_{cv}^2 + 4n_0^2}], \tag{3}$$

where the lower (upper) sign corresponds to electrons (holes). Equation (3) can be readily used in device simulations and is similar to a previous empirical formula[11] but derived here on rigorous grounds. We note Eq. (3) reduces to the familiar $n=C_{ox}V_{G0}/q$ at high gate voltage, and to $n=n_0$ (puddle regime) at $V_G \sim V_0$. Figure 1(b) displays the role of thermal and "puddle" corrections to the carrier density at 300 and 500 K. These are particularly important near $V_{G0}=0$ V, when the total charge density relevant in transport $(n+p)$ approaches a constant despite the charge neutrality condition imposed by the gate $(n-p=0)$. At higher temperatures ($k_BT \gg \Delta$) the spatial potential variation becomes less important due to thermal smearing and higher n_{th}.

Using the above, we obtain the mobility $\mu=(L/W)\times(I_{14}/V_{23})/[q(p+n)]$ at low fields ($\sim$2 mV/μm), where subscripts are terminals labeled in Fig. 1(a). Mobility is shown in Fig. 2(a) at various temperatures and $V_{G0}>0$ electron majority carriers.[12] (See supplement[5] for hole mobility and additional discussion). The mobility here peaks[14] at $\sim$4500 cm^2/V·s and decreases at carrier densities greater than $\sim 2\times10^{12}$ cm^{-2}, at 300 K. Mobility decreases with rising $T>300$ K for all carrier densities [Fig. 2(b)], as was also noted by Ref. 7 albeit in a lower temperature range. The dependence of mobility on carrier density and temperature suggests the dominant scattering mechanism changes from Coulomb to phonon scattering at higher densities and temperatures.[7] Inspired by empirical approximations for Si device mobility,[13] the data can be fit as (dashed lines in Fig. 2):[14]

$$\mu(n,T) = \frac{\mu_0}{1+(n/n_{ref})^{\alpha}} \times \frac{1}{1+(T/T_{ref}-1)^{\beta}}, \tag{4}$$

where $\mu_0=4650$ cm^2/V s, $n_{ref}=1.1\times10^{13}$ cm^{-2}, $T_{ref}=300$ K, $\alpha=2.2$, and $\beta=3$.

We now turn our attention to high-field drift velocity measurements, which pose challenges due to Joule heating and non-uniform potential along the channel.[4] To account for self-heating we estimate the average device temperature via its thermal resistance $\mathcal{R}_{th}$ [Fig. 1(a)]:[2]

$$\Delta T = T - T_0 \approx P(\mathcal{R}_B + \mathcal{R}_{ox} + \mathcal{R}_{Si}), \tag{5}$$

where $P=I_{14}V_{23}$, $\mathcal{R}_B=1/(hA)$, $\mathcal{R}_{ox}=t_{ox}/(\kappa_{ox}A)$, and $\mathcal{R}_{Si} \approx 1/(2\kappa_{Si}A^{1/2})$ with $A=LW$ the area of the channel, $h\approx10^8$ W m^{-2} K^{-1} the thermal conductance of the graphene-SiO$_2$ boundary,[15] κ_{ox} and κ_{Si} the thermal conductivities of SiO$_2$ and of the doped Si wafer.[5] At 300 K for our geometry $\mathcal{R}_{th}\approx10^4$ K/W, or $\sim 2.8\times10^{-7}$ m^2 K/W per unit of device area. Of this, the thermal resistance of the 300 nm SiO$_2$ ($\mathcal{R}_{ox}$) accounts for $\sim$84%, the spreading thermal resistance into the Si wafer ($\mathcal{R}_{Si}$) $\sim$12% and the thermal resistance of the graphene-SiO$_2$ boundary ($\mathcal{R}_B$) $\sim$4%. The role of the latter two will be more pronounced for smaller devices on thinner oxides. The thermal model in Eq. (5) can be used when sample dimensions are $W,L \gg t_{ox}$ but much less than the Si wafer thickness.[2]

To minimize charge non-uniformity and temperature gradients along the channel at high field[4] we bias the device at high $|V_G|$ and avoid ambipolar transport ($V_{GS}-V_0$ and $V_{GD}-V_0$ have same sign).[11] We confirm this with finite-element simulations.[4,5] The drift velocity is $v=I_{14}/(Wqn_{23})$ where n_{23} is the average carrier density between terminals 2 and 3, and the background temperature is held at $T_0=80$ K and 300 K. Due to self-heating ($T=T_0+\Delta T$), these enable measurements of saturation velocity (v_{sat}) near room temperature and above, respectively.

Figures 3(a) and 3(b) show the velocity-field relationship at the two background temperatures, indicating saturation tendency at fields $F>1$ V/μm. We fit the drift velocity by

$$v(F) = \frac{\mu F}{[1+(\mu F/v_{sat})^{\gamma}]^{1/\gamma}}, \tag{6}$$

where μ is the low-field mobility from Eq. (4) and $\gamma\approx2$ provides a good fit for the regime probed here. To limit the role of self-heating, data was only fit up to $\Delta T\sim200$ K (solid symbols).[16] To ensure no sample degradation due to high field stress we checked that low-field $I-V_G$ characteristics were reproducible after each high bias measurement.[16]

Figure 3(c) shows extracted drift velocity vs. electron density (symbols) at $F=2$ V/μm, for the two background temperatures. We compare these experimental results with an analytic model (dashed lines) which approximates the high-field distribution with the two half-disks shown in the Fig. 3(c) inset, suggested by previous simulations.[17] This model assumes v_{sat} is limited by inelastic emission of optical phonons (OPs) and leads to:[18]

$$v_{sat}(n,T) = \frac{2}{\pi}\frac{\omega_{OP}}{\sqrt{\pi n}}\sqrt{1-\frac{\omega_{OP}^2}{4\pi n v_F^2}}\frac{1}{N_{OP}+1}, \tag{7}$$

where $\hbar\omega_{OP}$ is the OP energy and $N_{OP}=1/[\exp(\hbar\omega_{OP}/k_BT)-1]$ is the phonon occupation. At low temperature and low carrier density the result is a constant, $v_{max}=(2/\pi)v_F\approx6.3\times10^7$ cm/s (six times higher than v_{sat} in Si); at high carrier density it scales as $v_{sat}=(2/\pi)\omega_{OP}/(\pi n)^{1/2}$, dependent both on the OP energy and the carrier density n.

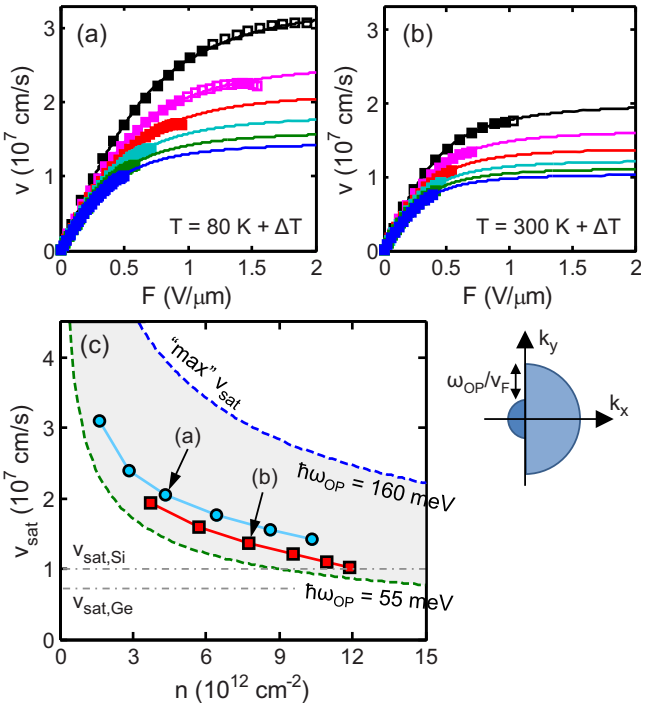

FIG. 3. (Color online) Electron saturation velocity. (a) Background temperature T_0=80 K with V_{G0}=10.5–60.5 V, and (b) T_0=300 K with V_{G0} =23.5–73.5 V (in 10 V steps from top to bottom). Squares represent data, lines are empirical fits with Eq. (6); open squares have $\Delta T > 200$ K from Joule heating and were not used for fit. Changing fitting criteria results in ±8% uncertainty. (c) Saturation velocity vs. electron density at F =2 V/μm. Side panel shows carrier distribution assumed for analytic model. Dashed lines show Eq. (7) with $\hbar\omega_{OP}$=55 meV (SiO_2) and 160 meV (graphene), the latter suggesting the maximum v_{sat} that could be achieved in graphene. Theoretical studies (Ref. 23) predict comparable $v_{sat} \approx 2-5 \times 10^7$ cm/s in carbon nanotubes. Electron v_{sat} for Si and Ge are appreciably lower but largely independent of carrier density (Ref. 21).

We consider two dominant phonon mechanisms in Fig. 3(c), $\hbar\omega_{OP}$=55 meV (lower dashed, SiO_2 substrate OP)[19] and $\hbar\omega_{OP}$=160 meV (upper dashed, graphene zone-edge OP).[20] The model limited by SiO_2 phonons slightly underestimates v_{sat}, while the model with graphene OPs significantly overestimates the measured v_{sat}. This suggests that both phonons play a role in limiting v_{sat}, but that substrate phonons are dominant for graphene on SiO_2. (For device simulations the fit can be optimized using an intermediate value $\hbar\omega_{OP} \approx 81$ meV). Nevertheless, v_{sat} is greater than in Si for charge densities $n < 1.2 \times 10^{13}$ cm^{-2} and more than twice that of Si at $n < 4 \times 10^{12}$ cm^{-2}. With only the graphene OP ($\hbar\omega_{OP}$=160 meV) the model suggests an upper limit for the "maximum" v_{sat} that could be expected. This intrinsic v_{sat} could be more than twice as high as that measured here on SiO_2 and from two to six times higher than in Si for the carrier densities considered here.

Finally, we note the data in Fig. 3(c) suggest a temperature dependence of v_{sat}, included here through the last term in Eq. (7). This term is qualitatively similar to that in Si,[21] and due to the OP scattering (emission) rate being proportional to $(N_{OP}+1)$.[22] The model yields a ~20% decrease in v_{sat} between ~280 K and ~500 K if the SiO_2 phonon is dominant, and a ~2% decrease if the graphene OP is dominant. The data in Fig. 3(c) show much closer agreement with the former, once again indicating the effect of the SiO_2 in limiting graphene transport.

In summary, we examined mobility and saturation velocity in graphene on SiO_2, including the roles of carrier density and temperature. We focused on the $T > 300$ K and high field $F > 1$ V/μm regime, where few studies exist. Both data and models point to the SiO_2 substrate limiting graphene transport. Nevertheless, the maximum saturation velocity could be two to six times greater than in Si up to carrier densities of 1.2×10^{13} cm^{-2}. The models introduced are simple yet practical, and can be used in future simulations of graphene devices operating near room temperature and up to high fields.

We acknowledge financial support from the Nanotechnology Research Initiative (NRI), ONR (N00014-10-1-0061), NSF (CCF 0829907), and valuable discussions with S. Datta, D. Estrada, M. Fuhrer, and E. Tutuc.

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