

Electronic, Thermal, and Unconventional (?) Applications of 2D Materials

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SystemX Alliance and Precourt Institute for Energy (PIE)
Stanford University**

<http://poplab.stanford.edu>



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Acknowledgements

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- **Alumni:**

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- **S. Suryavanshi**, **N. Wang**, R.L. Xu, **C. McClellan**, **C. Bailey**

- **Undergrads:**

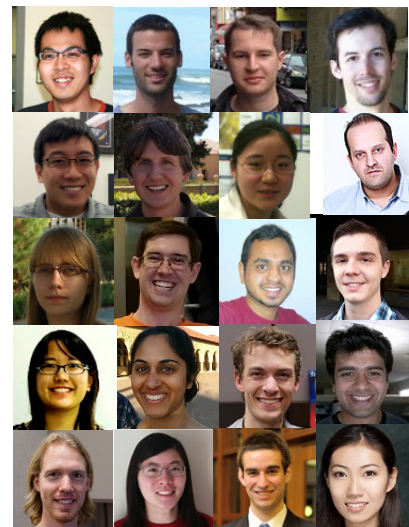
- **Andrew**, **Aria**, **Megan**, Stephone, Tim, Job, Justin, Erin, Priyanka...

- **Sponsors:**

- National Science Foundation (NSF), Army Research Office (ARO)
- Air Force (AFOSR), Intel, STARnet-SONIC, SystemX Alliance

- **Collaborators:**

- Z. Bao, K. Goodson, A. Lindenberg, S. Mitra, Y. Nishi, E. Reed, K. Saraswat, H.-S.P. Wong, X. Zheng (Stanford), D. Cahill, W. King, J. Lyding, J. Rogers, M. Shim (UIUC), M. Rudan (Bologna), C. Jacoboni (Modena), D. Jena (Cornell), T. Grasser (TU Wien), D. Ielmini, R. Sordan (Milano), J. Shiomi (Tokyo)



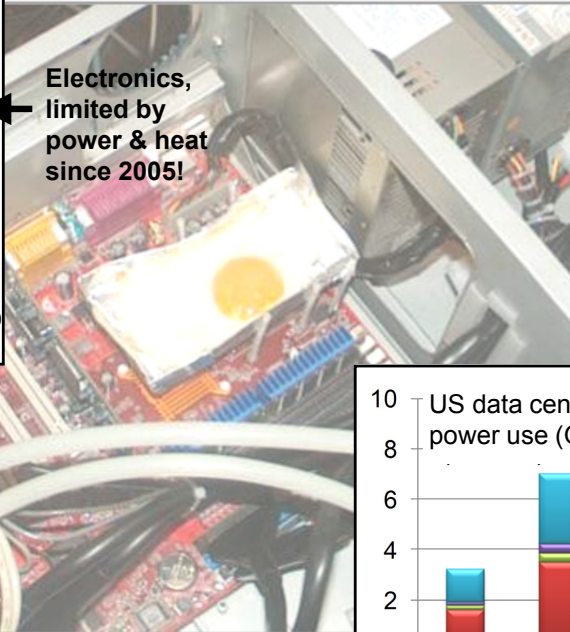
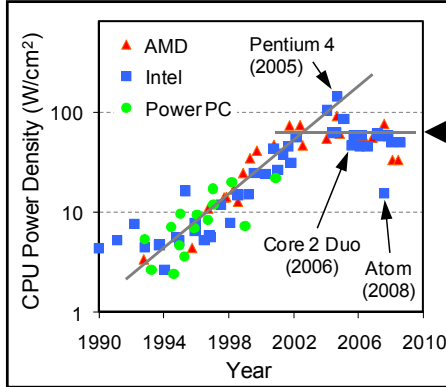
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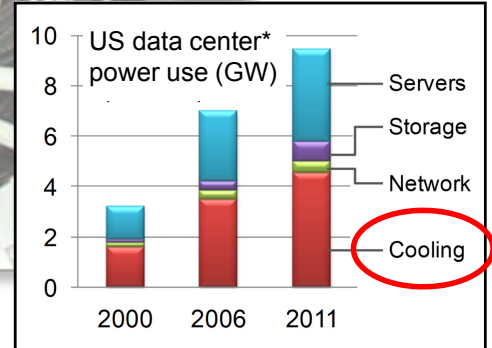
2

Electronics Use (and Waste) Much Power

E. Pop, *Nano Research* 3, 147 (2010)
new course: Energy in Electronics, EE 323



J. Koomey (Stanford)



Calibrating: 1 GW ~ 1 nuclear power plant
12 GW ~ all electricity used by Argentina

*World-Wide about 30 GW

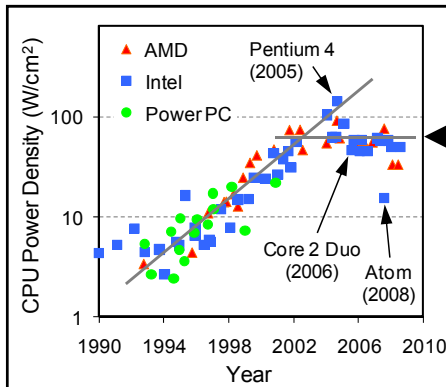
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Pop Lab: Energy and Electronics

Review: E. Pop, *Nano Research* 3, 147 (2010); new course: EE 323 "Energy in Electronics" at Stanford



Electronics, limited by power & heat since 2005!

Computing on flexible 2D fabrics (graphene, MoS₂)

Energy-efficient data storage:

100x lower power in phase-change memory (PCM)

Xiong et al, *Science* (2011)

Energy harvesting: up to ~1 W from body heat using flexible thermoelectrics (TE)

flexible TEs
usable body heat ~1 W
~50 mW

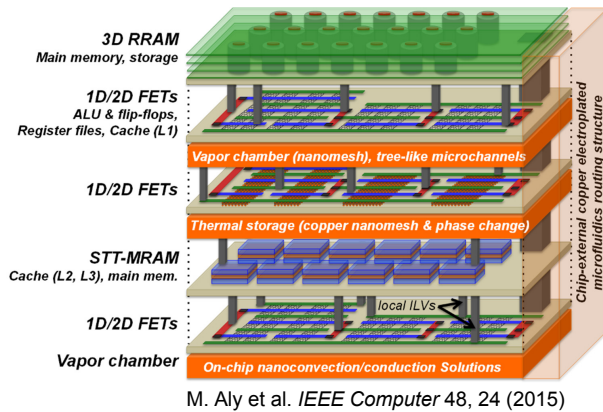
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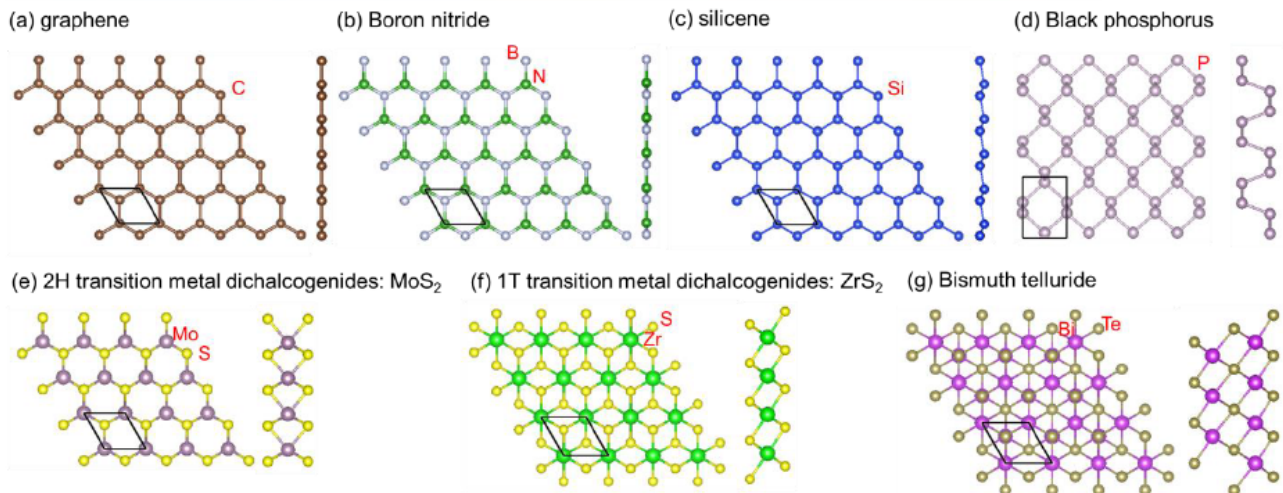
What's Driving the 2D Work at Stanford?

- Heterogeneous Integration (HI) in SystemX Alliance
- Integration of “beyond-Si” platforms for “beyond Moore” applications
 - **3D integration** of logic, memory, sensors, thermal management, flexible substrates...
 - **Energy-efficient** design and energy-harvesting opportunities

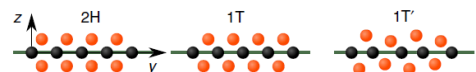


- Collaborators: Y. Cui, D. Goldhaber-Gordon, K. Goodson, T. Heinz, A. Lindenberg, Y. Nishi, E. Pop, E. Reed, A. Salleo, K. Saraswat, H.-S.P. Wong, X. Zheng

Atomic Structure of Some 2D Materials

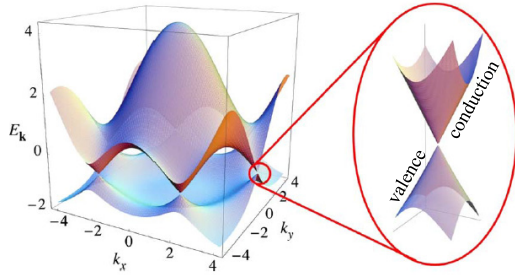


- 2D lattices can be planar (graphene, BN), buckled (Xenes), 1T, 2H, 3R
- Transition metal dichalcogenides (TMDs) are 2H or 1T(')
- Phase change 2H (semic.) to 1T or 1T' (metallic) by ΔT , strain or Li interc.

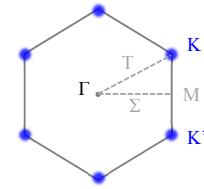


Electronic Band Structure of 2D Materials

graphene: semimetal



Castro-Neto, Rev. Mod. Phys. (2009)

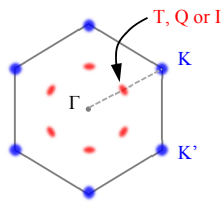


$$E = \hbar v_F k$$

$$v_F \approx 10^8 \text{ cm/s}$$

$K = K'$ degeneracy

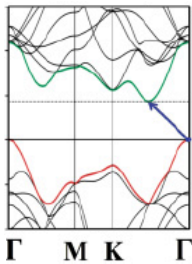
MX_2 TMDs



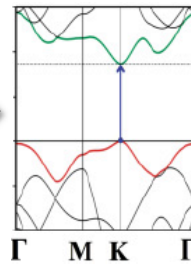
$K = 2x$ degenerate

$Q = 6x$ degenerate (along T line, sometimes mislabeled Σ or Λ)

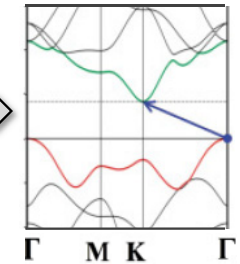
Bulk MoS_2
(indirect gap)



1L MoS_2
(direct gap)



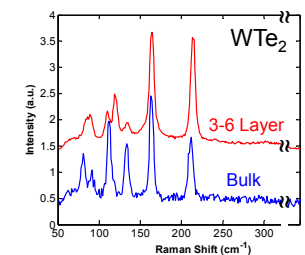
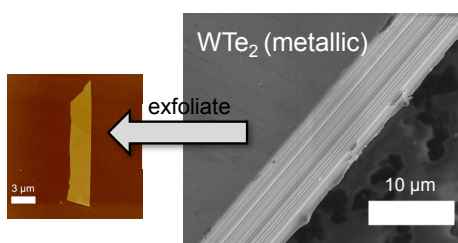
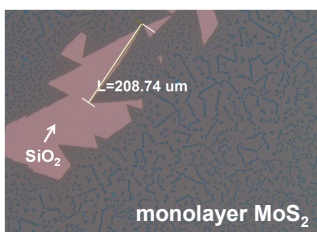
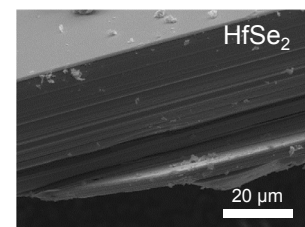
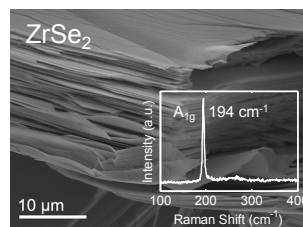
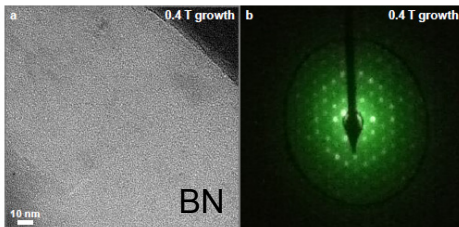
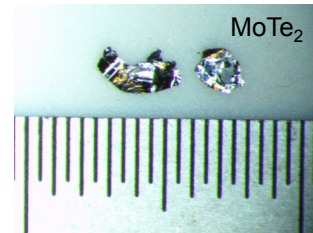
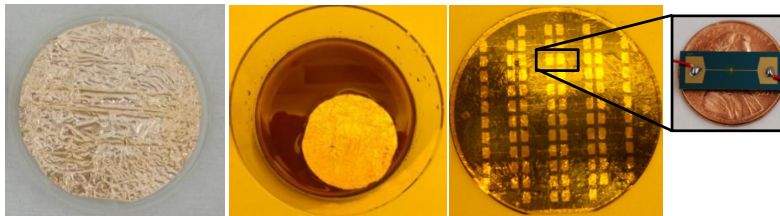
1L MoS_2
(tensile strain*)



(*less is known about strain)

2D Materials at Stanford

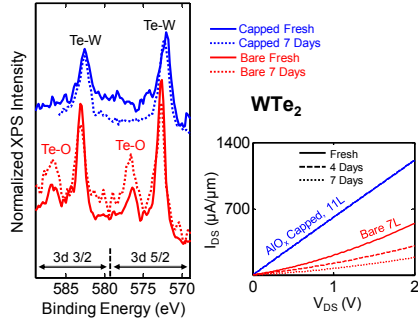
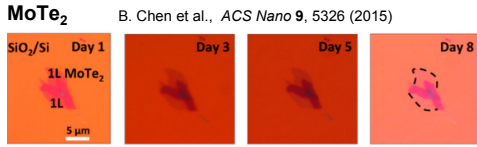
CVD growth of monolayer graphene, BN and MoS_2



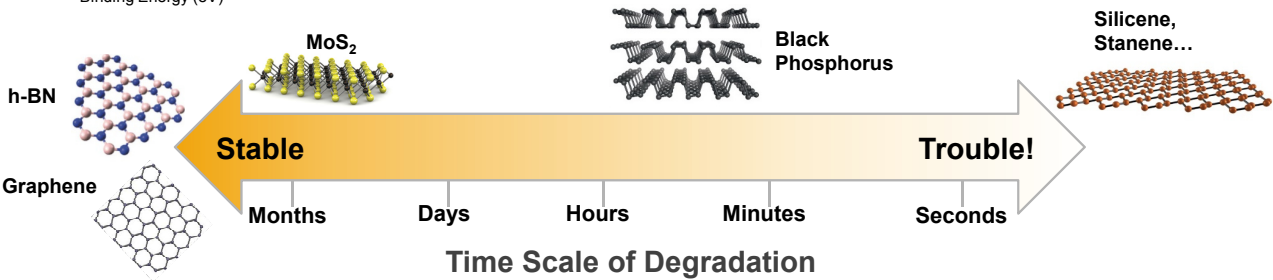
Ambient Stability of 2D Materials*

M. Mleczo, L. Xu, E. Pop, et al., *ACS Nano* **10**, 7507 (2016)

*monolayers will be least stable



	-S ₂	-Se ₂	-Te ₂
Mo	Yellow	Yellow	Yellow
W	Yellow	Yellow	Yellow
Nb, Sn	Yellow	Yellow	Yellow
Hf, Zr Ta, Ti	Yellow	Yellow	Yellow



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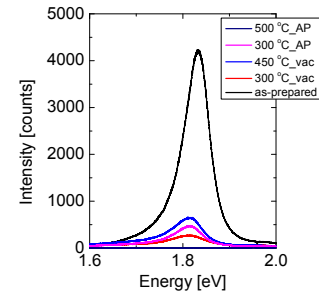
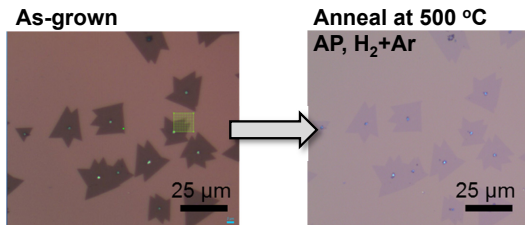
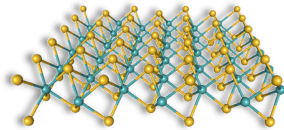
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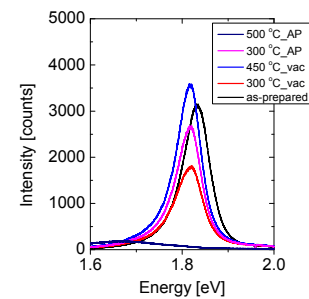
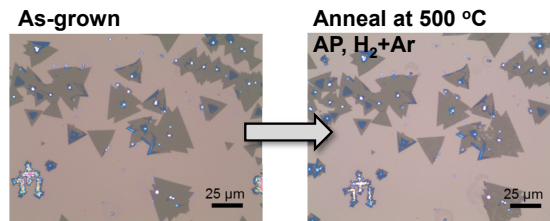
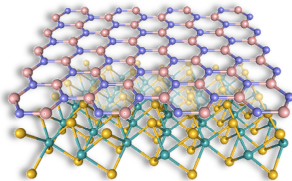
Enhanced Stability by Capping with h-BN

work of Y.C. Shin and V. Chen (Pop Lab)

Unprotected MoS₂



h-BN capped MoS₂



- Monolayer h-BN protects monolayer MoS₂ up to ~500 °C
- AlO_x (by ALD) can also be used as encapsulation layer (but can dope)

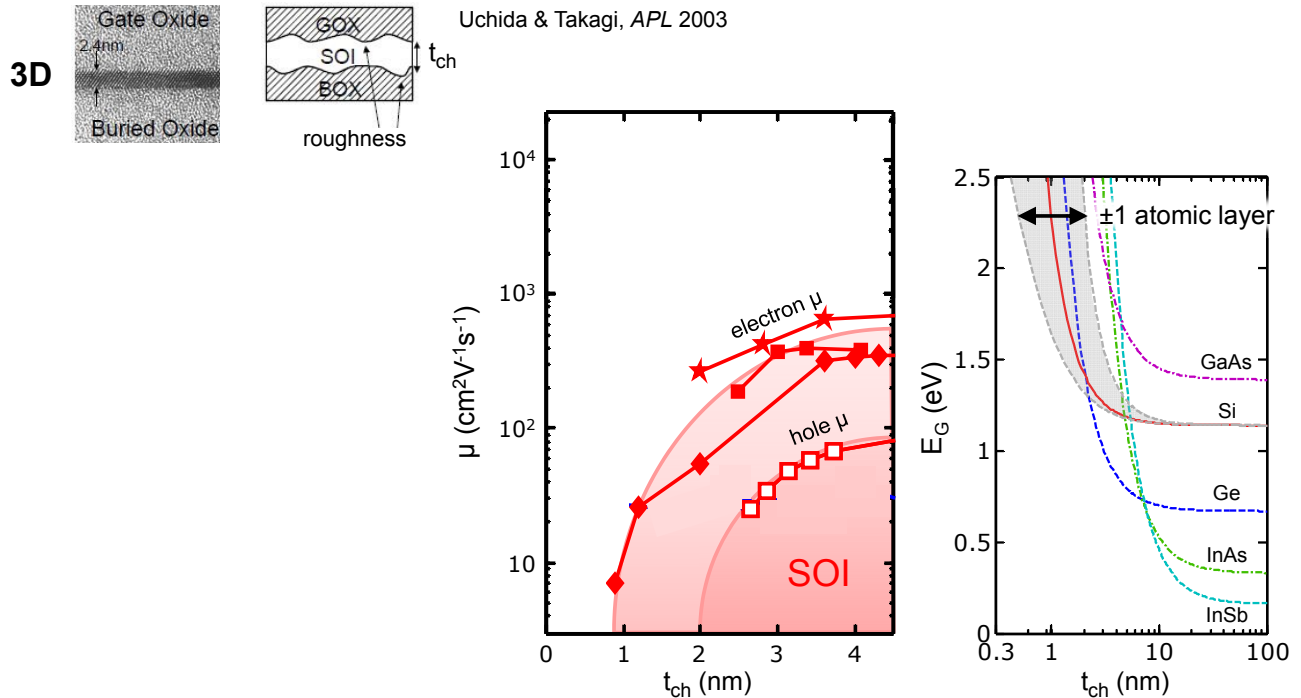
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Transistors Beyond Silicon?

- **Problem:** 20th century transistors “carved” out of bulk materials (Si) → surface roughness restricts mobility, band gap, variability



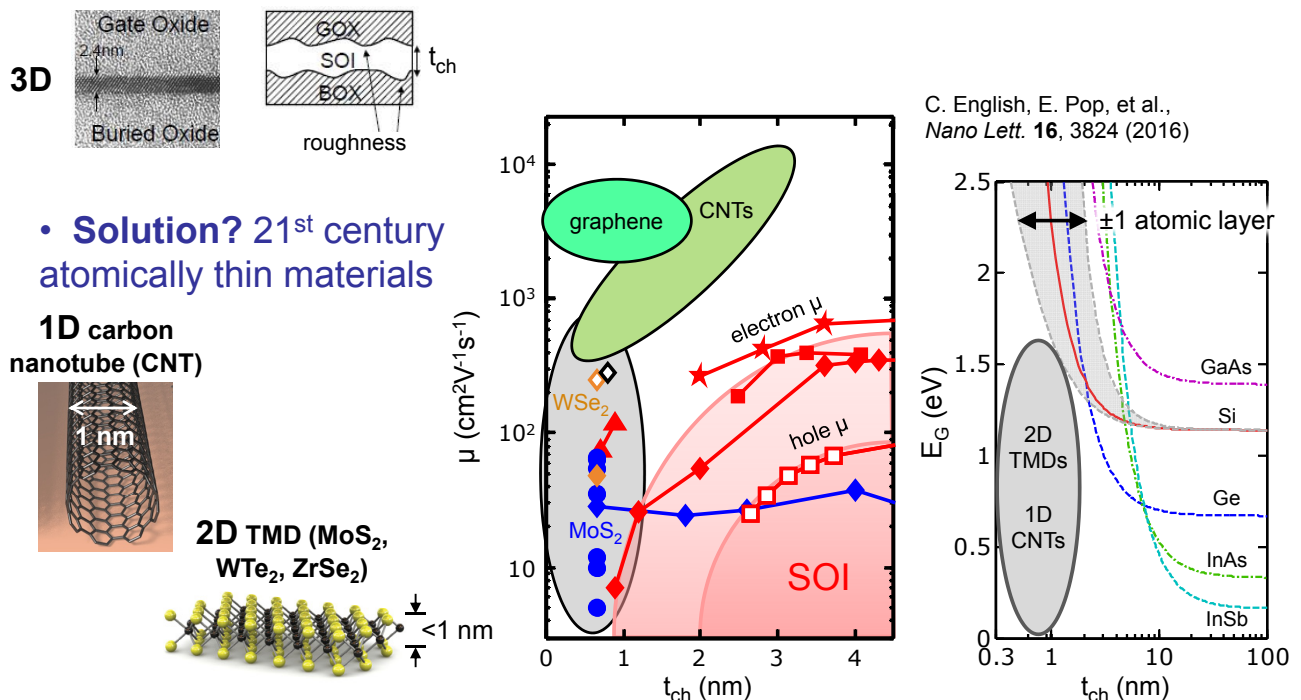
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Transistors Beyond Silicon?

- **Problem:** 20th century transistors “carved” out of bulk materials (Si) → surface roughness restricts mobility, band gap, variability

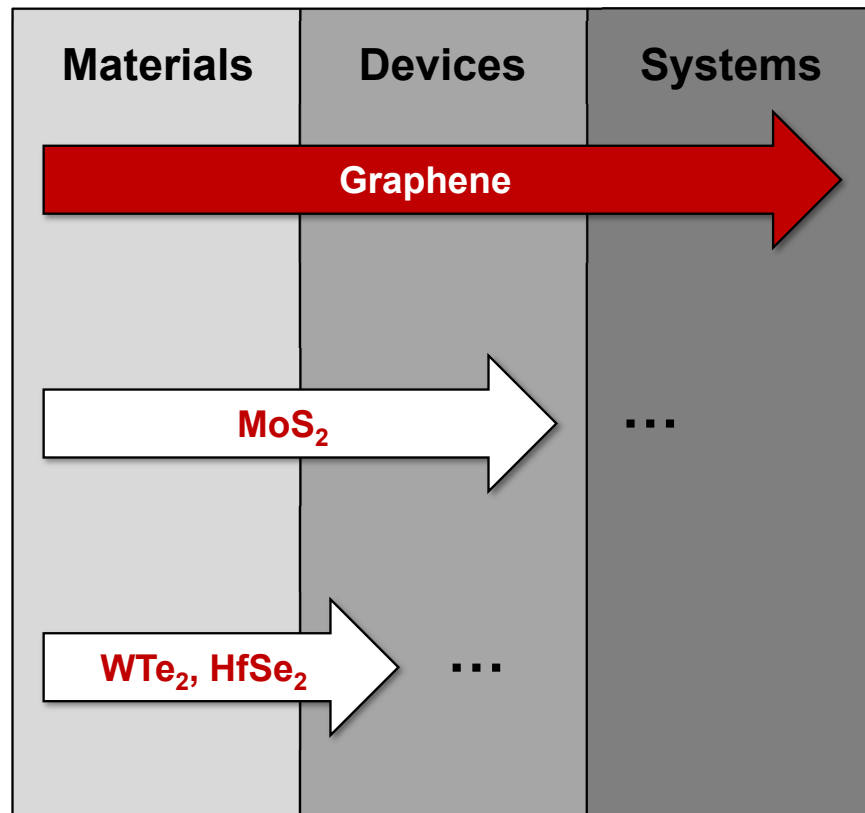
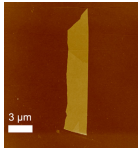
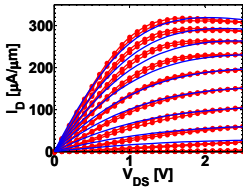
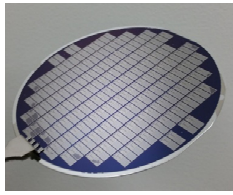


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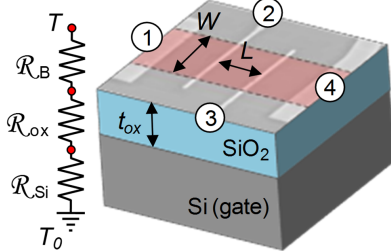
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2D Materials to Systems (Today)

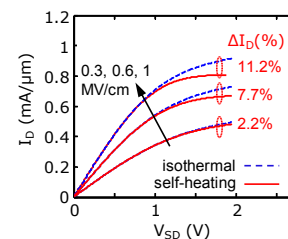
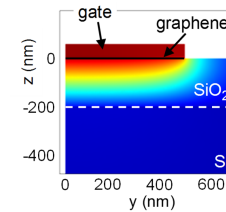
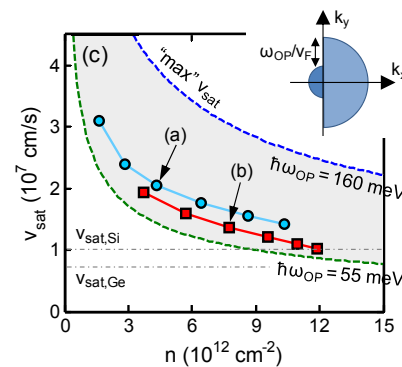


Early Work: Graphene Device Transport

V. Dorgan, M.-H. Bae, E. Pop, *Appl. Phys. Lett.* **97**, 082112 (2010)
 S. Islam, Z. Li, V.E. Dorgan, M.-H. Bae, E. Pop, *IEEE EDL* **34**, 166 (2013)



$$\Delta T = T - T_0 \approx P(R_B + R_{ox} + R_{Si})$$

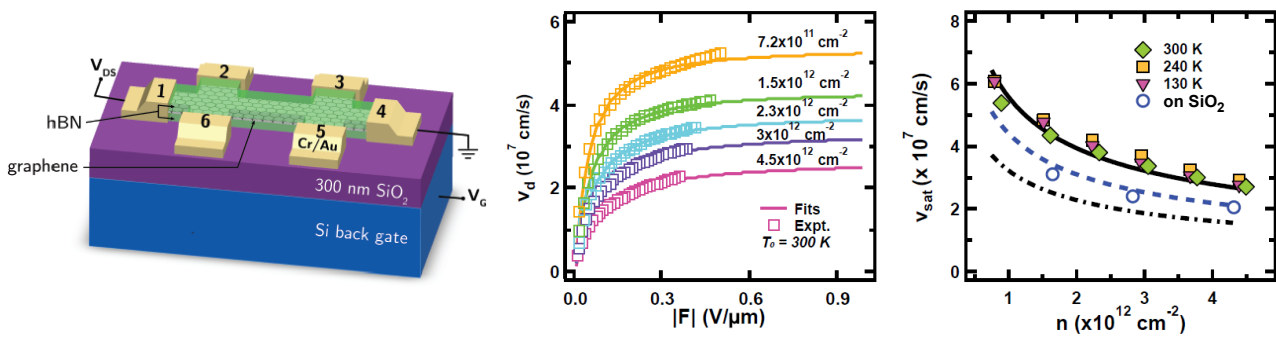


- Lack of transport studies* at $T > 300$ K and high-field $v_{sat} (>1 \text{ V}/\mu\text{m})$
- High-field **saturation velocity** (measurement needs constant field)
- Extracted practical electrical and thermal **compact models**

*at the time

Today: Record Drift Velocity in Graphene-hBN

M. Yamoah, W. Yang, E. Pop, D. Goldhaber-Gordon, *ACS Nano*, DOI:10.1021/acsnano.7b03878 (2017)



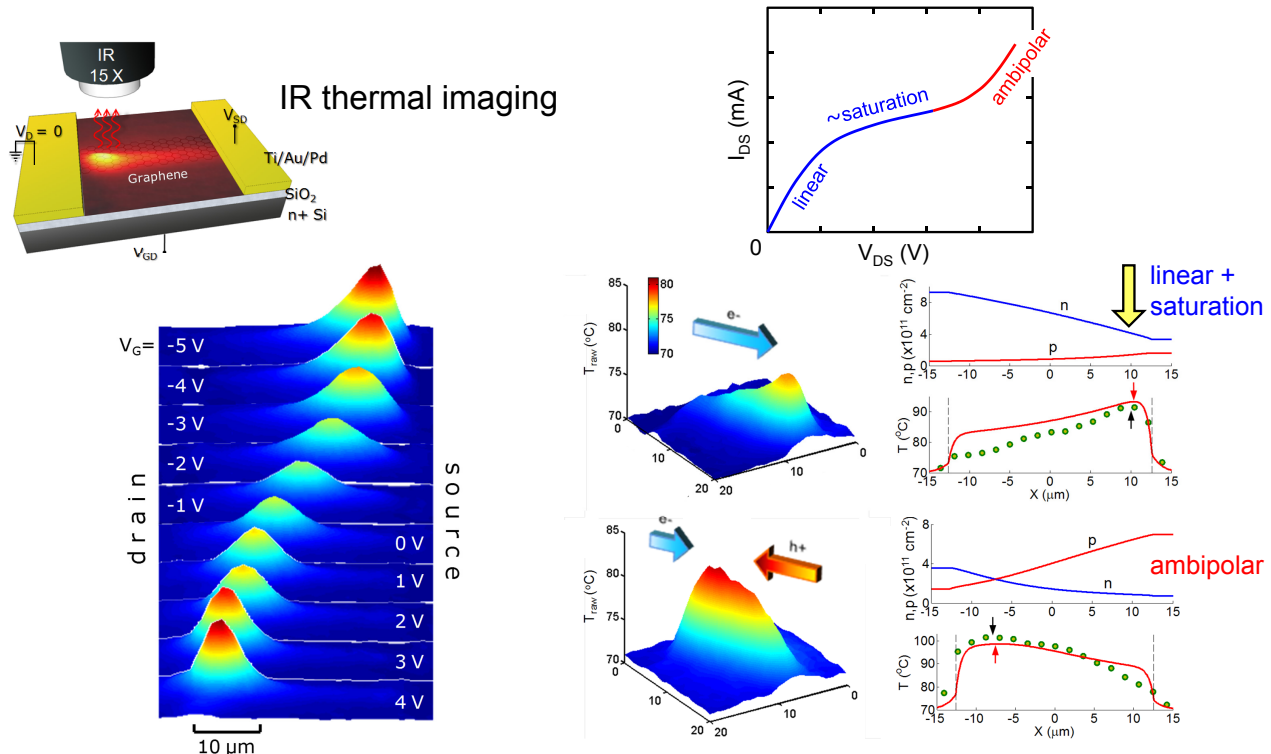
$$\Delta T = T - T_0 \approx P(\mathcal{R}_{BN} + \mathcal{R}_B + \mathcal{R}_{ox} + \mathcal{R}_{Si}) \quad v_{sat}(n, T) = \frac{2}{\pi} \frac{\omega_{OP}}{\sqrt{\pi n}} \sqrt{1 - \frac{\omega_{OP}^2}{4\pi n v_F^2} \frac{1}{N_{OP} + 1}}$$

- Ultra-high quality hBN-graphene-hBN → $\mu \sim 50$ to 100×10^3 cm²/V/s
- Velocity saturation achieved at (relatively) low fields ≥ 0.2 V/μm
- hBN surface phonons ~ 100 meV → record $v_{sat} = 3$ to 6×10^7 cm/s

Early Work: Thermal Imaging Graphene FETs

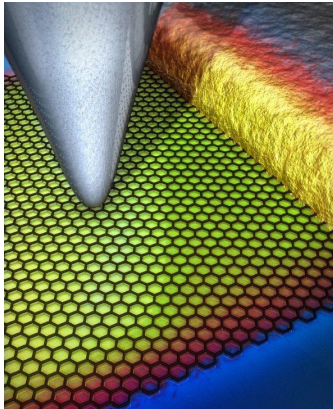
M.-H. Bae, Z.-Y. Ong, D. Estrada, E. Pop, *Nano Letters* **10**, 4787 (2010)

M.-H. Bae, S. Islam, V.E. Dorgan, E. Pop, *ACS Nano* **5**, 7936 (2011)

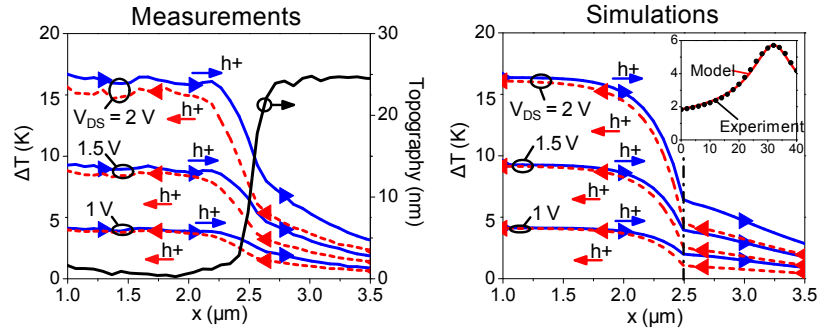
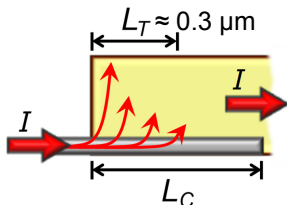


Thermoelectric Effects at Graphene Contacts

K. Grosse, M.-H. Bae, F. Lian, E. Pop, W. King, *Nature Nanotechnology* 6, 287 (2011)



scanning Joule expansion microscopy (SJEM)



- AFM-based thermometry (SJEM)
- Contact temperature due to:
 - Current crowding (CC) } 2/3
 - **Thermoelectric effect (TE)** } 1/3
- Some 2D materials have large thermopower S
 - Engineer cooling at device contacts?
 - Design built-in TE coolers?

Simulation Tools Available Online

available on <http://nanoHUB.org>

GFET Tool

GFET Tool simulates the thermal and electrical properties of a graphene field-effect transistor. The user can alter parameters and observe how the transistor behaves.

There are certain conditions where the code may not converge and an error will occur.

Please note that the nanohub version is implemented in octave and simulations will take around 1 minute to run.

Basic Settings | Advanced User Settings

- Width: **1e-06m**
- Length: **1e-06m**
- Initial Temperature: **293K**
- Gate Voltage: **0V**
- Dirac Voltage: **0V**
- Maximum Drain Current (A): **0.001**
- Drain Current Step (A): **5e-05**
- Top Gate Oxide Thickness: **1e-08m**
- Mobility [$\text{cm}^2/\text{V}\cdot\text{s}$]: **3000**

S2DS

nanoHUB.org
an NCN project

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Home > Groups > NEEDS: Nano-Engineered Electronic Device Simulation Node > Resources > Compact 1.0.0 > About

Stanford 2D Semiconductor (S2DS) Transistor Model 1.0.0

By Saurabh Vinayak Suryavanshi¹, Eric Pop¹

1. Stanford University

Download (VA)

Additional materials available (7)

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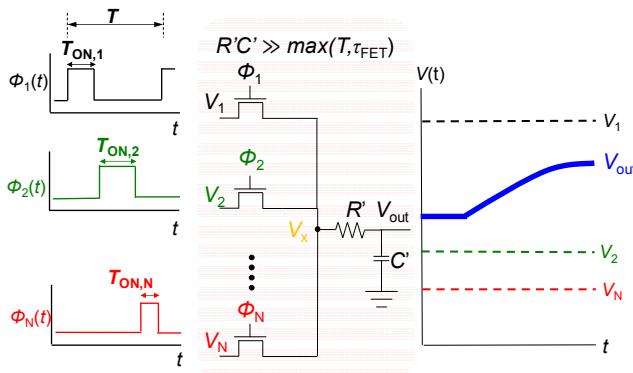
transistor models including self-heating

Today: Graphene-Based Systems

N. Wang, S. Gonugondla, I. Nahlus, N. Shanbhag, E. Pop, *VLSI Symp.* (2016)

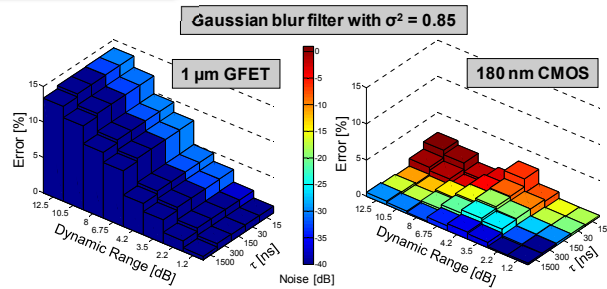
- **Dot product** nanofunction used for image processing, neural networks...
- Takes advantage of native graphene properties (**high μ** , flexible...)
- Tolerates graphene drawbacks (low I_{ON}/I_{OFF} ratio)

Idea:



switched analog circuit (SAC)
weights encoded by pulse widths $p_i T$

Simulation:

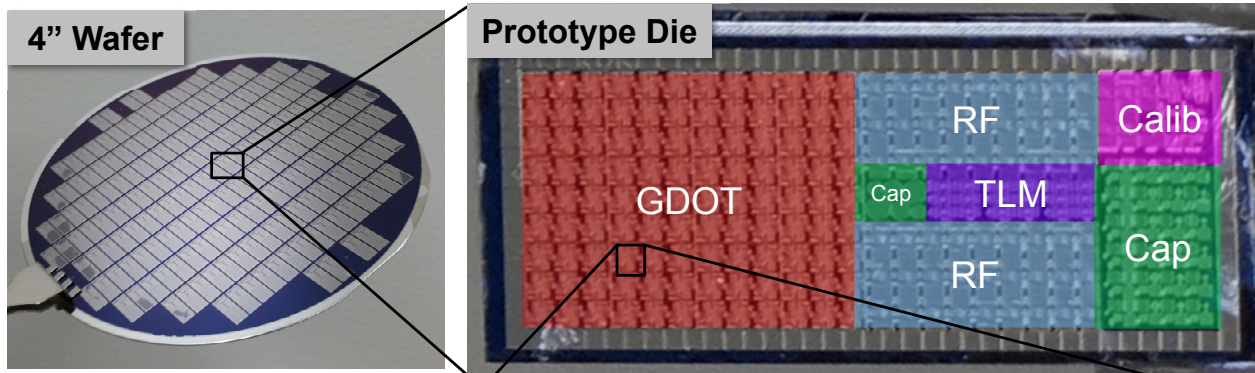


- + Fast
- + Smaller area
- + Low noise
- Narrow input range (due to low I_{ON}/I_{OFF})

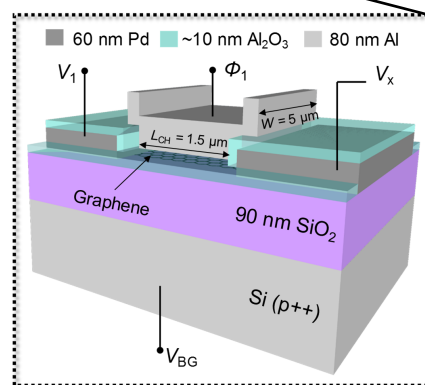
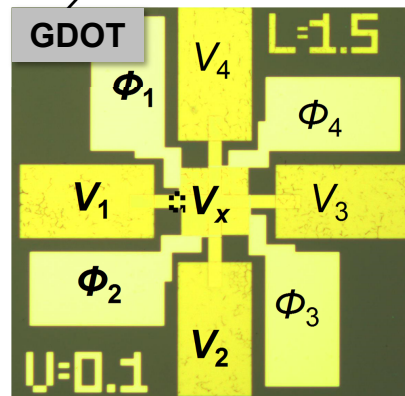
- + High accuracy
- + Wide input range
- Slow and noisy
- Larger area

... and Implementation

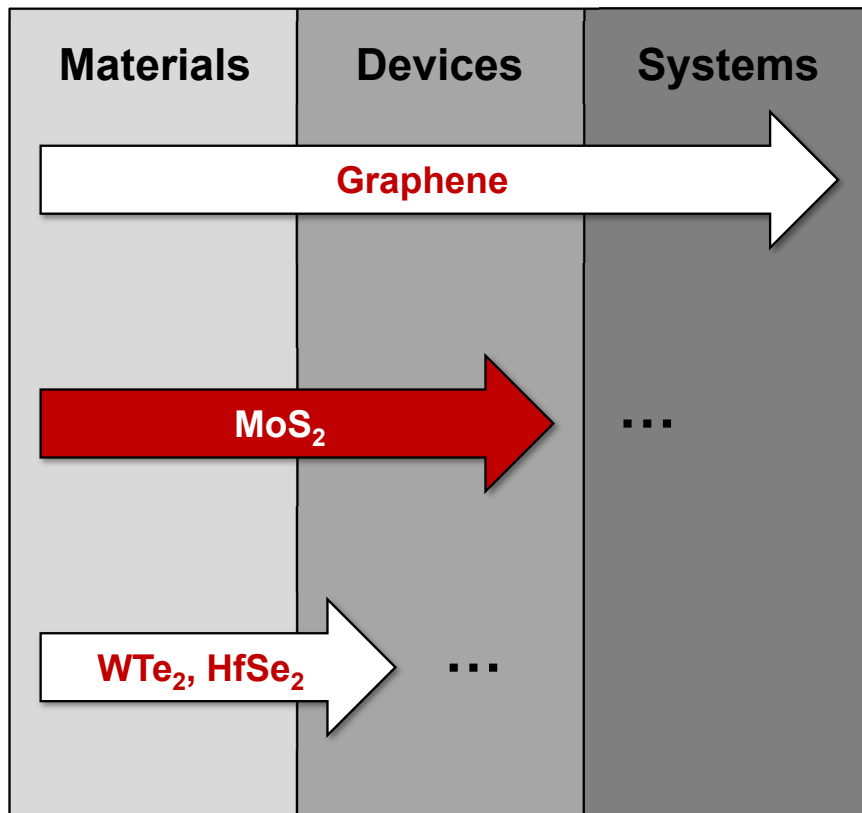
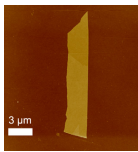
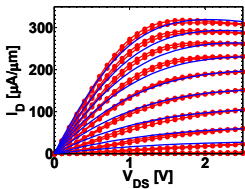
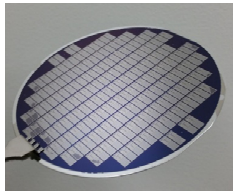
N. Wang, S. Gonugondla, I. Nahlus, N. Shanbhag, E. Pop, *VLSI Symp.* (2016)



- Wafer-scale graphene growth
- Advances in heterogeneous integration
- “Average” devices but unique function

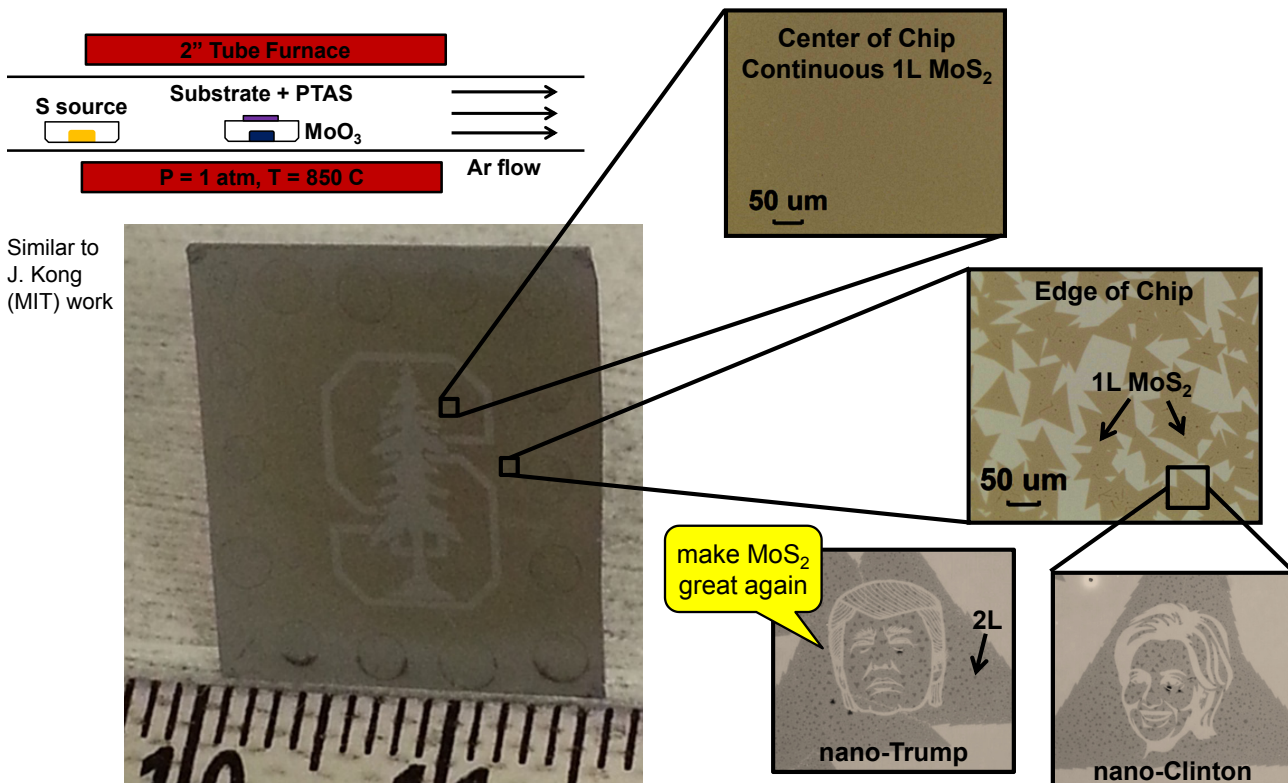


2D Materials to Systems (Today)



CVD Growth of MoS₂ Monolayers

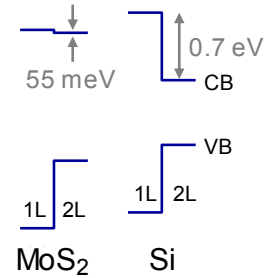
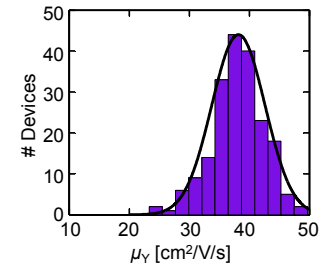
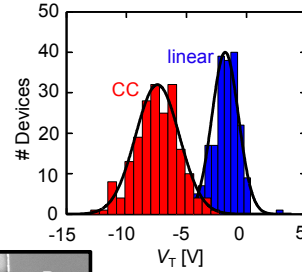
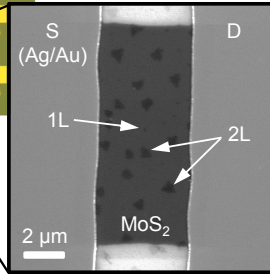
K. Smithe, C. English, S. Suryavanshi, E. Pop, *2D Materials* 4, 011009 (2017)



Electrical Properties of 1L MoS₂ Transistors

K. Smithe, S. Suryavanshi, M. Munoz Rojo, A. Tedjarati, E. Pop, *ACS Nano* 11, 8456 (2017)

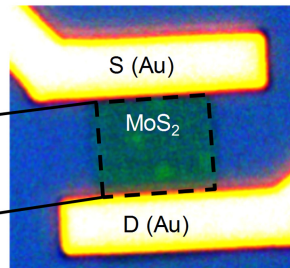
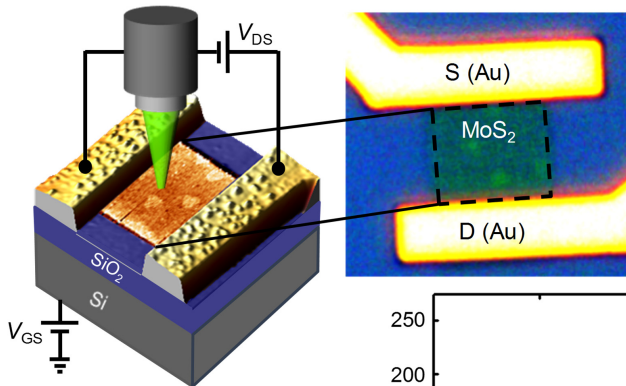
Over 300 1L MoS₂ FETs
 25/25 nm Ag/Au contacts
 30 nm SiO₂ back-gate
 Lengths from 3 – 20 μm
 Widths from 5 – 20 μm



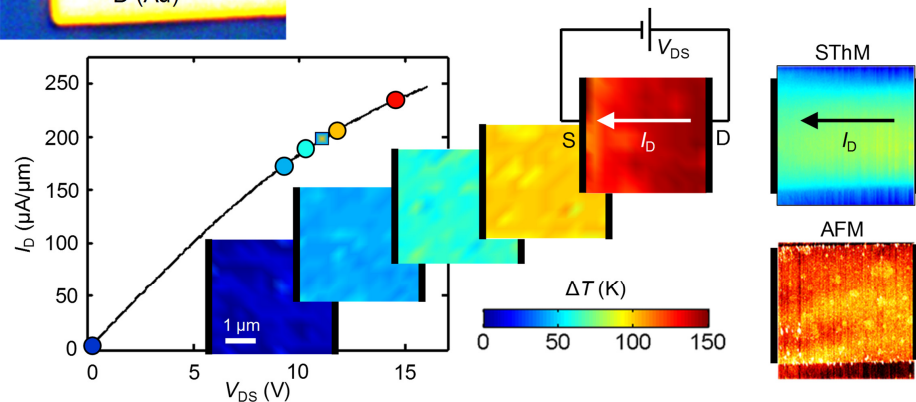
- Large area monolayer (1L) MoS₂ devices
- Mobility $\mu = 30$ to 50 cm²/V/s and $R_C \sim 1$ k Ω - μ m
- Surprise: **less** variability due to “patches” of 2L than ultra-thin silicon!
- Why? Because 1L-2L conduction band offset is small (~ 55 meV)

Energy Dissipation in MoS₂ Transistors

E. Yalon, C. McClellan, K. Smithe, R.L. Xu, M. Munoz-Rojo, S. Suryavanshi [...] E. Pop, *Nano Letters* 17, 3429 (2017)



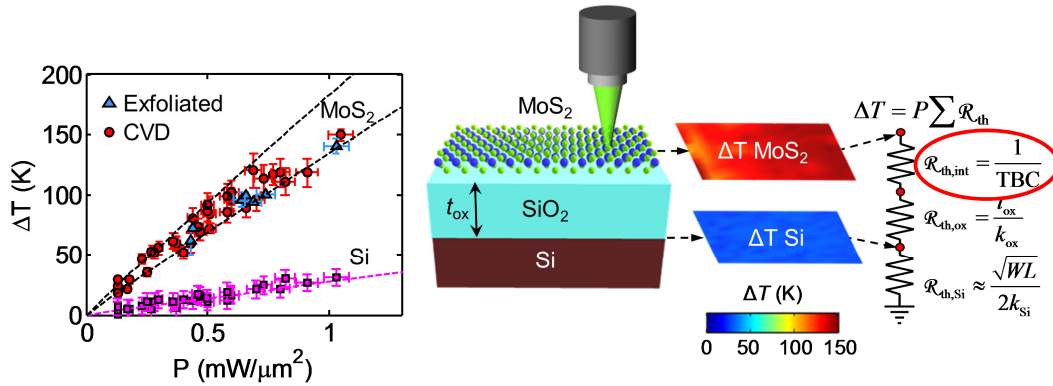
- Raman thermal imaging of functioning MoS₂ transistors
- Bilayer (2L) regions do not heat or cool differently



- Surprise: **less** variability due to “patches” of 2L than ultra-thin silicon!
- Why? Because 1L-2L conduction band offset is small (~ 55 meV)

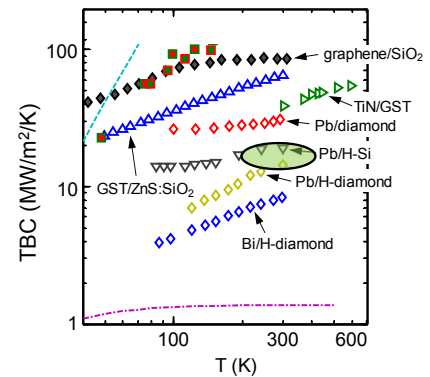
Energy Dissipation in MoS₂ Transistors

E. Yalon, C. McClellan, K. Smithe, R.L. Xu, M. Munoz-Rojo, S. Suryavanshi [...] E. Pop, *Nano Letters* **17**, 3429 (2017)



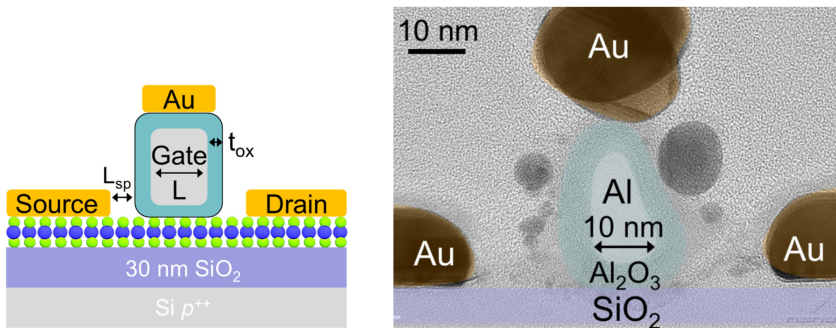
Simultaneously get ΔT of MoS₂ and substrate

- Accurate thermal boundary conductance (TBC) of MoS₂-SiO₂ = 14 ± 4 MW/m²/K
- Kapitza length is ~ 90 nm of SiO₂ (!)
- Very low TBC, comparable to Pb-diamond

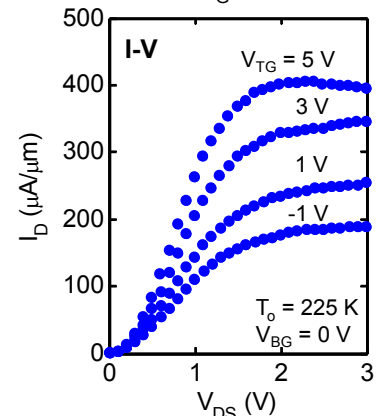
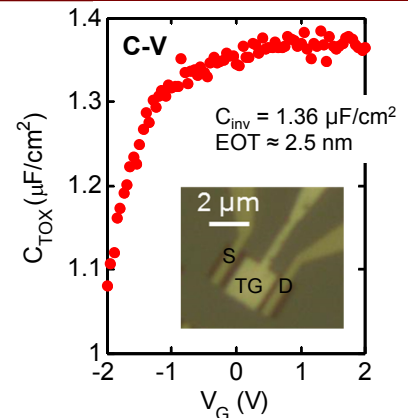


Nanoscale MoS₂ Channel (~ 10 nm)

C. English, K. Smithe, R.L. Xu, E. Pop, *IEDM* (2016)

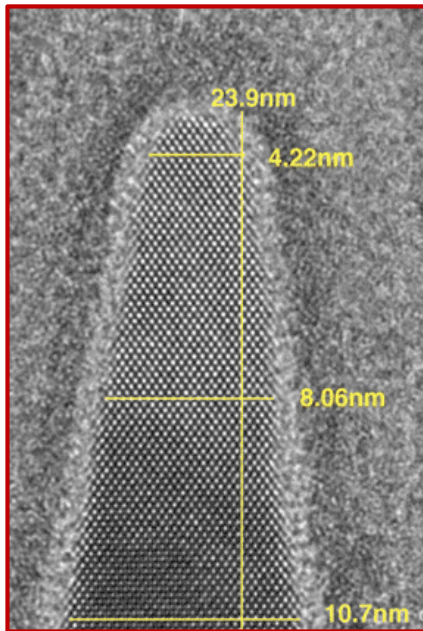


- Self-aligned top-gated monolayer CVD MoS₂
- Similar to SOI, but with 6.15 Å “thick” channel
- **Record $I_{Dsat} > 400 \mu\text{A}/\mu\text{m}$ for monolayer MoS₂**
- Simulations suggest devices are $\sim 20\%$ ballistic
- Must improve contacts, long-channel μ , EOT...

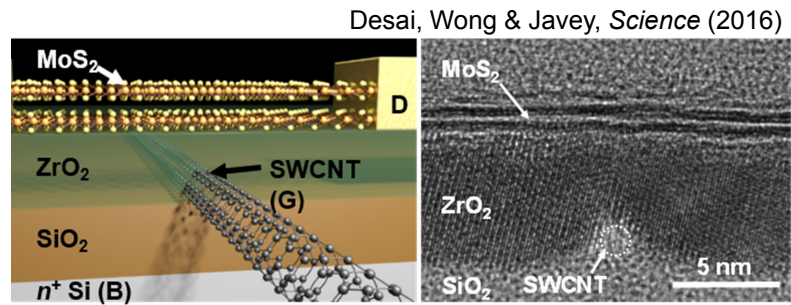


Modern FinFET vs. Atomically Thin MoS₂ FETs

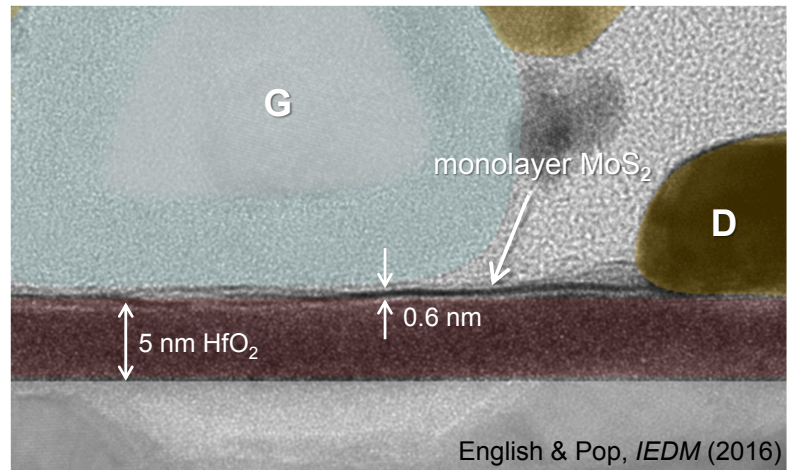
(note same scale)



Intel "14 nm" FinFET



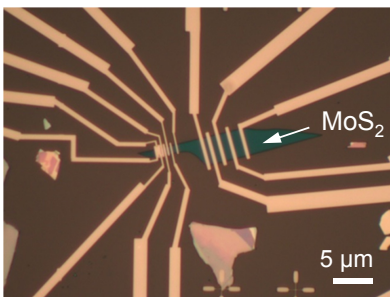
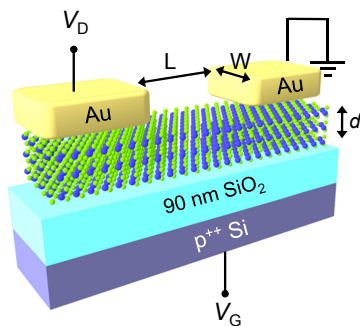
Desai, Wong & Javey, *Science* (2016)



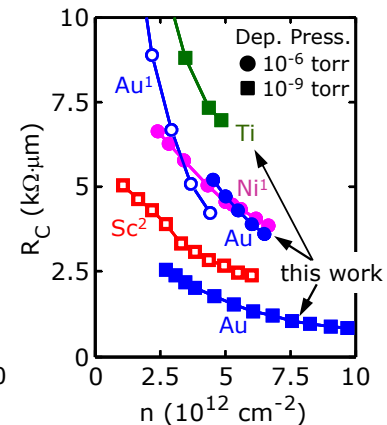
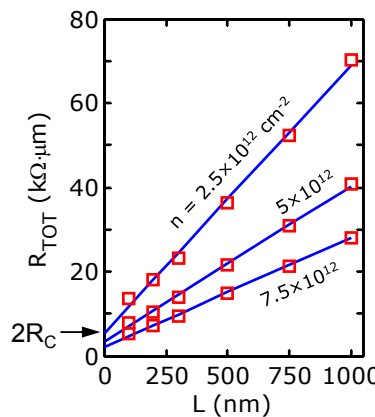
English & Pop, *IEDM* (2016)

Metal Contacts to MoS₂ (Clean but Undoped)

C. English, G. Shine, V. Dorgan, K. Saraswat, E. Pop, *Nano Lett.* **16**, 3824 (2016)



Transfer Length Method (TLM)



- Contacting 2D materials is **difficult**
- Careful TLMs are important
- **Cleaner Au deposition (~10⁻⁹ torr) leads to improved contacts**

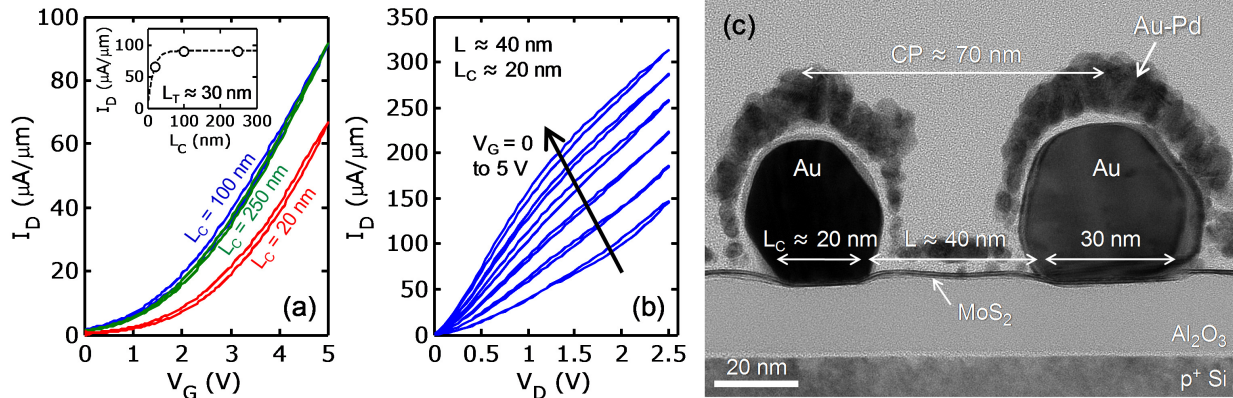
– $R_C \sim 740 \Omega \cdot \mu\text{m}$ and $\rho_C \approx 4 \times 10^{-7} \Omega \cdot \text{cm}^2$

¹H.Liu & P. Ye (2013), ²S. Das & J. Appenzeller (2013)

Nanoscale MoS₂ Contacts

C. English, G. Shine, V. Dorgan, K. Saraswat, E. Pop, *Nano Lett.* **16**, 3824 (2016)

Goal: scale both channel length and contacts of MoS₂ FETs → what happens?

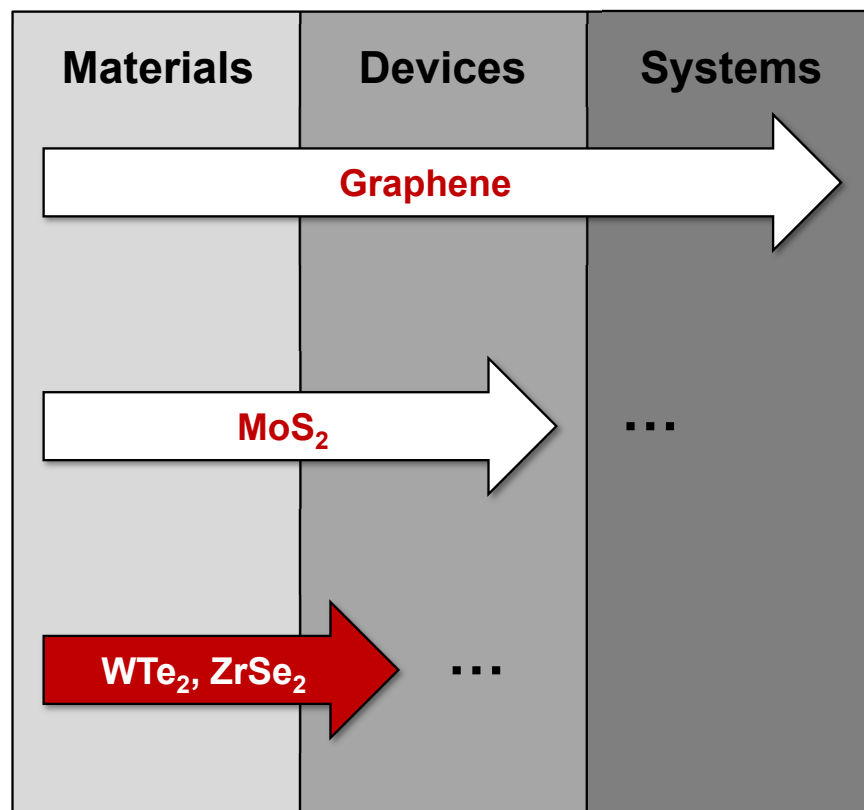
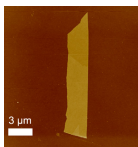
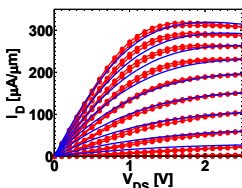
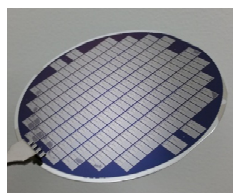


- **Smallest MoS₂ contacts to date**

- L = 40 nm and variable contacts ($L_C = 20$ to 100 nm)
- Smallest contact pitch CP ~ 70 nm, **equivalent to “14 nm” tech. node**

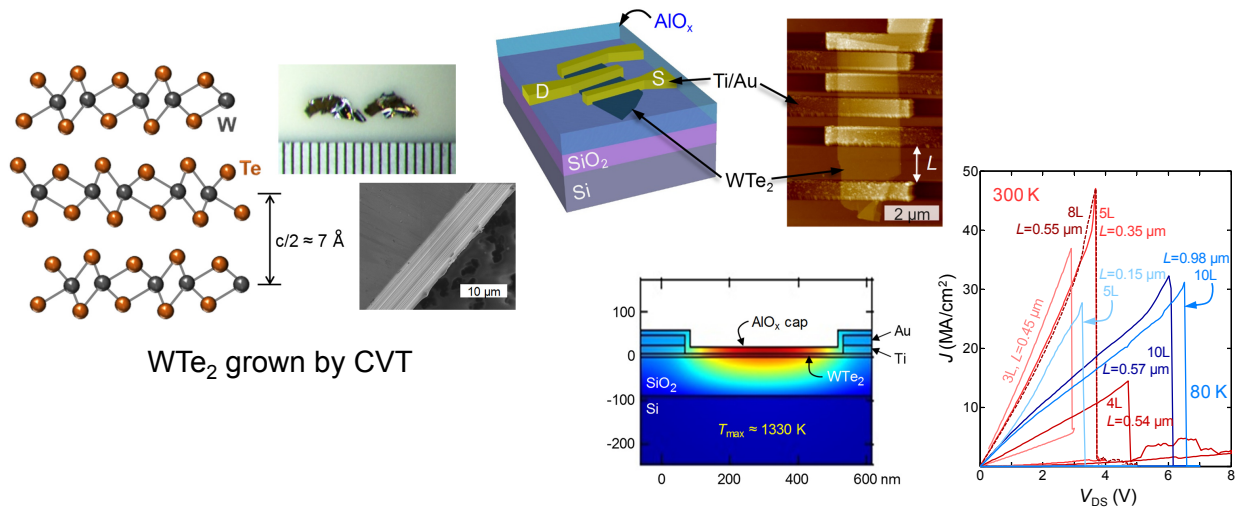
- **Contacts are limiting** the performance of small MoS₂ transistors

2D Materials to Systems (Today)



2D Semi-Metal: WTe_2

M. Mleczko, R. Xu, K. Okabe, H.-H. Kuo, I.R. Fisher, H.-S.P. Wong, Y. Nishi, E. Pop, *ACS Nano* **10**, 7507 (2016)

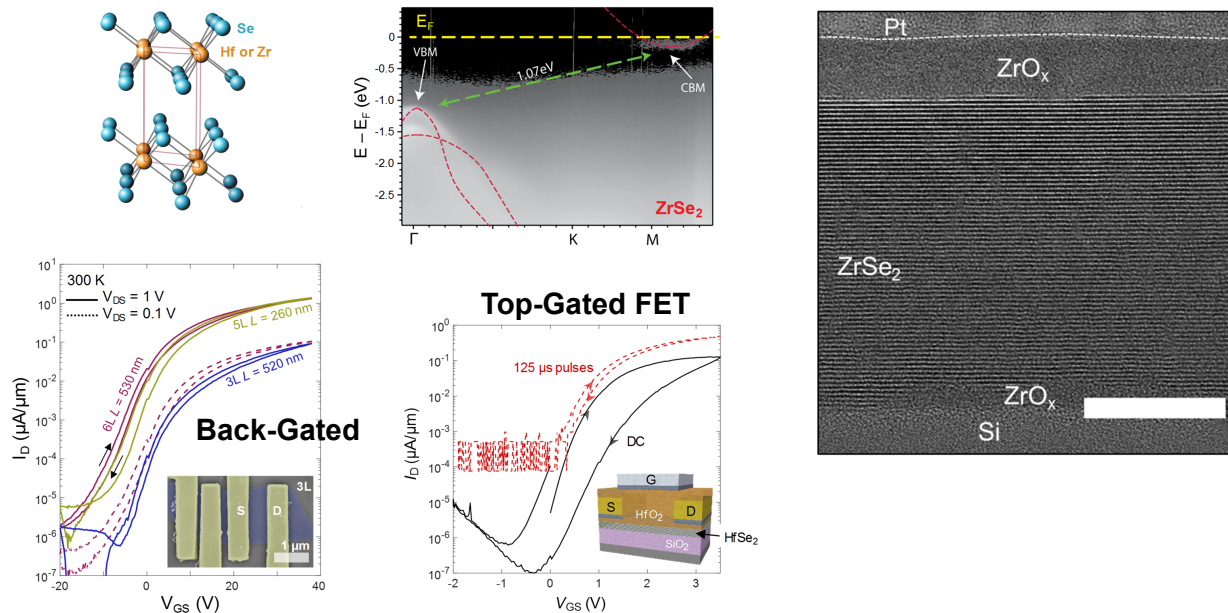


WTe_2 grown by CVT

- Thin (<6 layer) WTe_2 unstable in air, but **stable after capping** with AlO_x
- **High-current density** (40-50 MA/cm²) and low thermal conductivity (3-5 W/m/K)
- Potential applications as electrode in low-power phase-change memory

2D Semiconductors with Native High-K Oxides

M. Mleczko, C. Zhang, [...], I. Fisher, Y. Nishi, E. Pop, *Science Advances* **3**, e1700481 (2017)

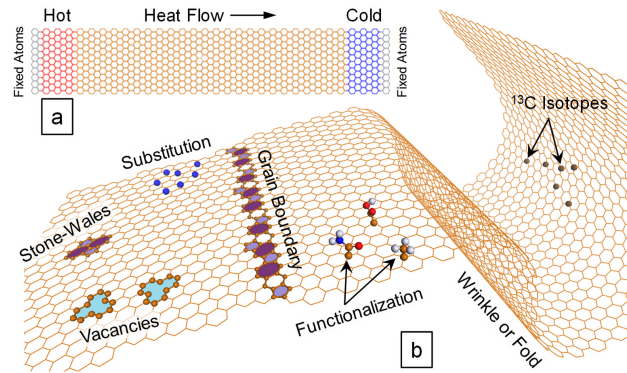


- $HfSe_2$ and $ZrSe_2$ have band gaps around 1 eV
 - ... and native HfO_2 and ZrO_2
- } similar to silicon but in 2D form!

2D Material Thermal Properties

- **Large in-plane** thermal conductivity of graphene, BN (>500 W/m/K)
- **Ultra-low cross-plane** thermal conductivity of layered WSe_2 (<0.1 W/m/K)
 - Lower than plastics and **comparable to air**
- Huge thermal anisotropy in all layered 2D materials (>10-100x)
- MRS Bulletin review with AFRL:

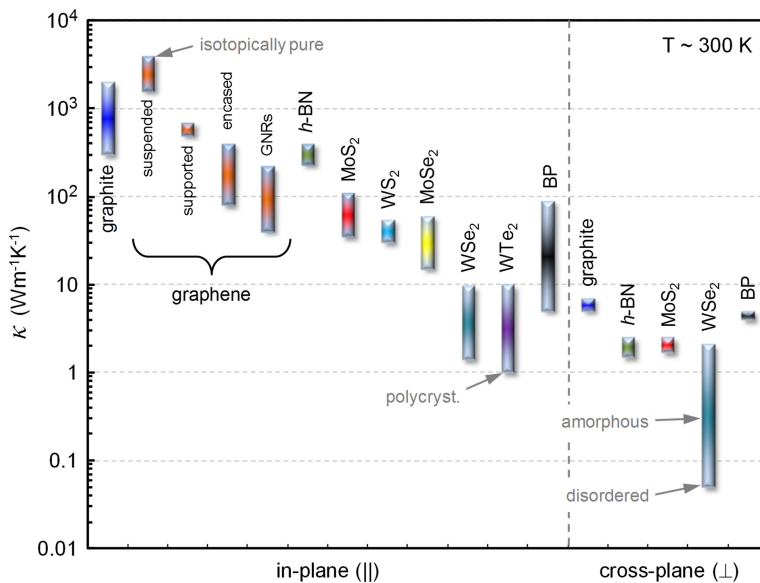
E. Pop, V. Varshney, A.K. Roy, "Thermal Properties of Graphene: Fundamentals and Applications," *MRS Bulletin* **37**, 1273 (2012)



- **Large thermopower** in TMDs ($S \sim 0.5$ mV/K) \rightarrow Thermoelectrics?

$$ZT = \frac{S^2 \sigma T}{k}$$

Thermal Conductivity of 2D Materials



$$Q'' = -k \nabla T$$

heat flux \uparrow thermal conductivity \uparrow T gradient \uparrow

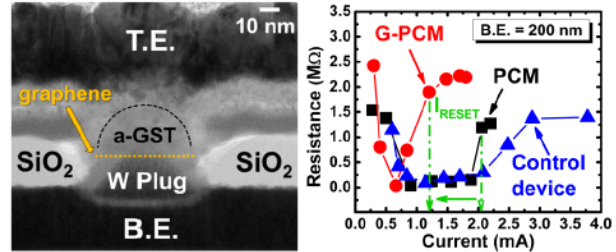
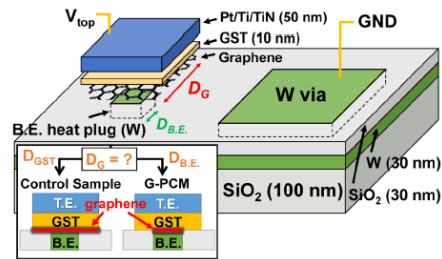
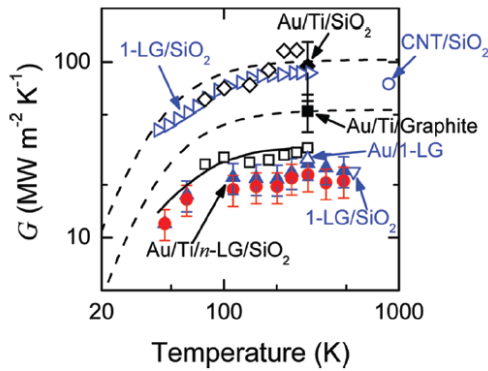
- **Huge thermal anisotropy** of 2D materials: in-plane $\kappa_{||} \gg$ cross-plane κ_{\perp}
- Note: must use "**correct thickness**" of monolayers from XRD or TEM, e.g. 3.35 Å for graphene and 6.15 Å for MoS_2 (**not** thickness from AFM)

Unusual: Graphene as Thermal Barrier for PCM

Y.K. Koh, M.-H. Bae, D.G. Cahill, E. Pop, *Nano Lett.* **10**, 4363 (2010)

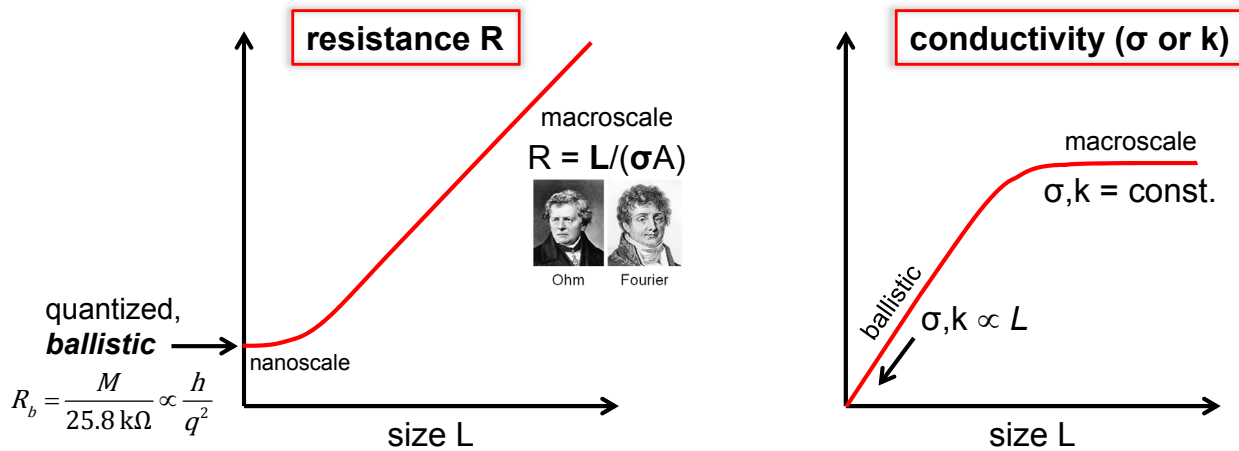
C. Ahn, S.W. Fong, Y. Kim, S. Lee, A. Sood, C. Neumann, K. Goodson, E. Pop, H.-S.P. Wong, *Nano Lett.* **15**, 6809 (2015)

- Phase-change memory (PCM) needs good thermal insulation

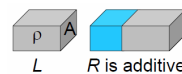


- Exploiting graphene thermal boundary resistance (TBR) ~ 30 nm SiO₂
- Ultra-thin **thermal barrier** limits PCM heat loss \rightarrow 40% lower current

Heat (and Current) Flow in Nanoscale Samples



- Macroscale, R is additive: $1 + 1 = 2$

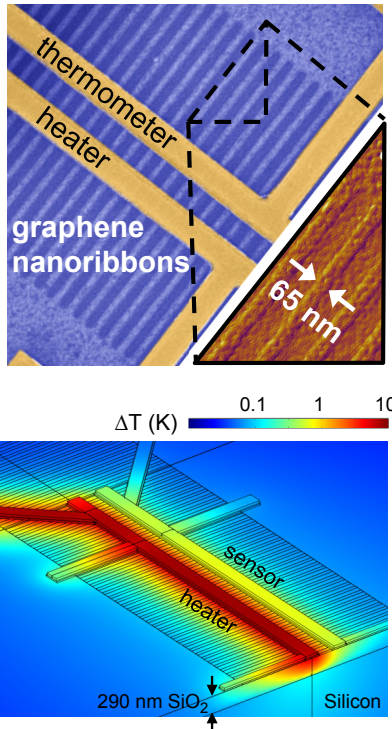


- Nanoscale**, R is quantized: $1 + 1 = 1$

- Occurs when system size is comparable to electron or phonon (heat) wavelengths and mean free path (10-100 nm)
- Both electrical and thermal resistance can be **quasi-ballistic**

Thermal Conductivity of Nanoscale Graphene

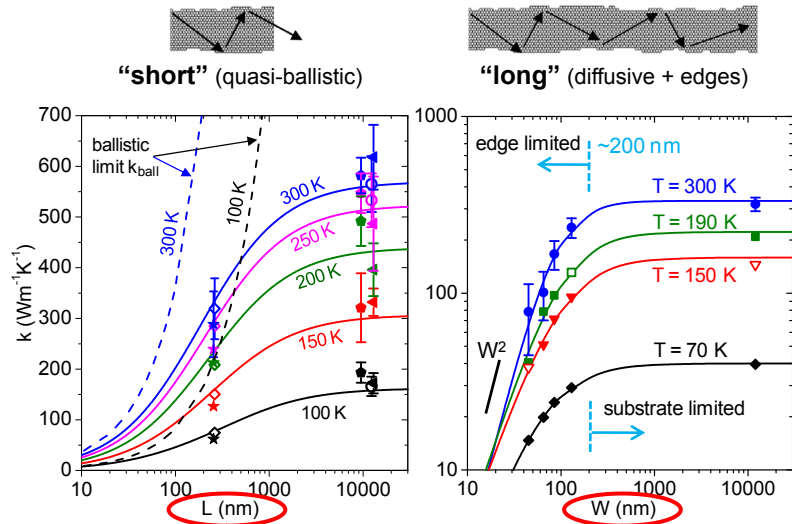
M.-H. Bae, Z. Li, Z. Aksamija, P. Martin, F. Xiong, Z.-Y. Ong, I. Knezevic, E. Pop, *Nature Comm.* 4, 1734 (2013)



Bulk thermal properties do not apply at $\le 1 \mu\text{m}$!

Thermal conductivity $k(T) = f(W, L)$ even at room T

- 35% (quasi-)ballistic heat flow in short devices ($\lambda \sim 100 \text{ nm}$)
- Strong edge scattering in narrow devices



E. Pop

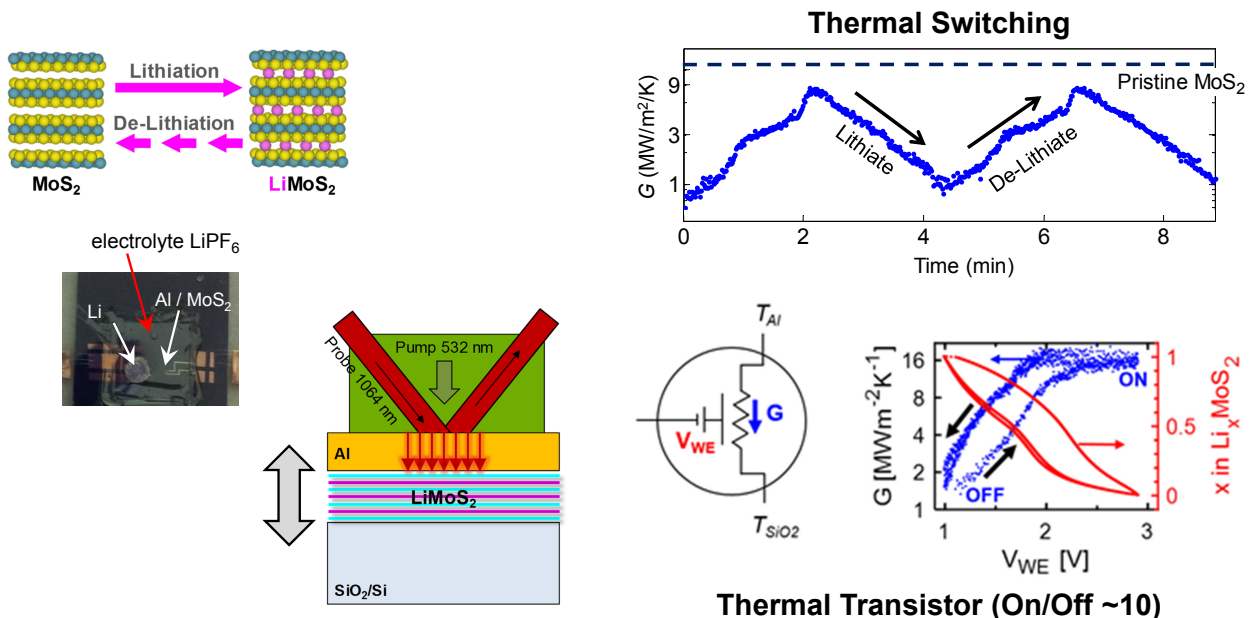
Stanford ENGINEERING

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Unusual Application: Thermal Transistors

A. Sood, F. Xiong, [...], Y. Cui, E. Pop, K Goodson, *submitted* (2017)

- Could we... manipulate & **switch heat flow?** (e.g. thermal circuits)
- Ex: using reversible Li intercalation in MoS_2



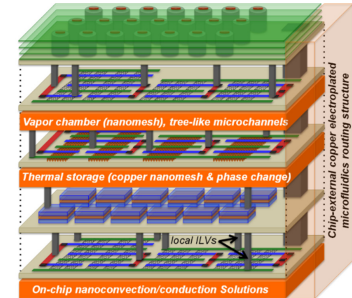
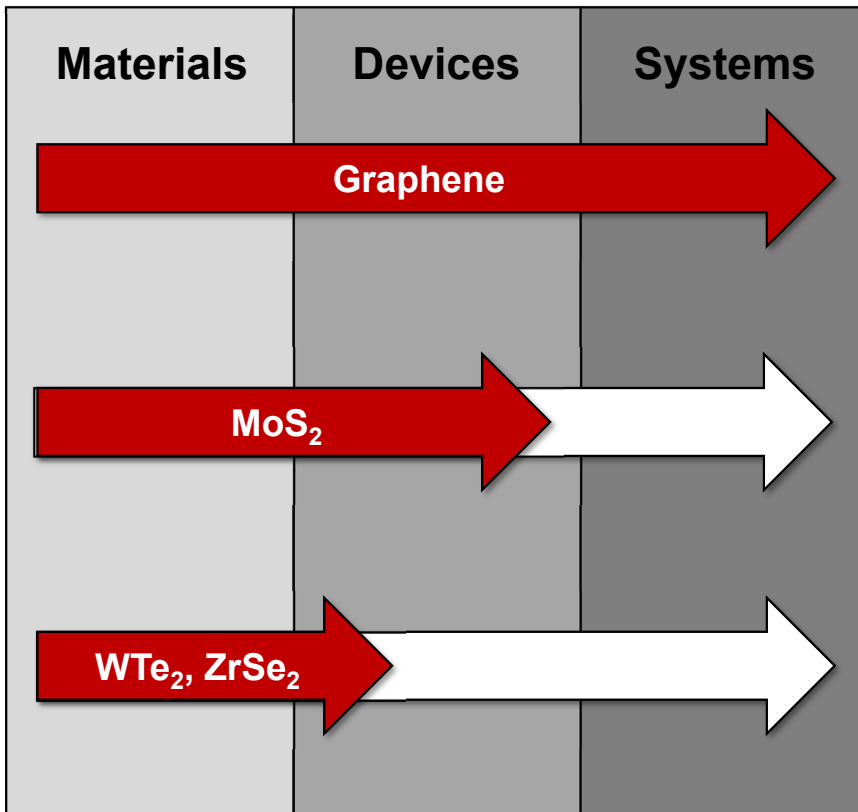
Thermal Transistor (On/Off ~ 10)

E. Pop

Stanford ENGINEERING

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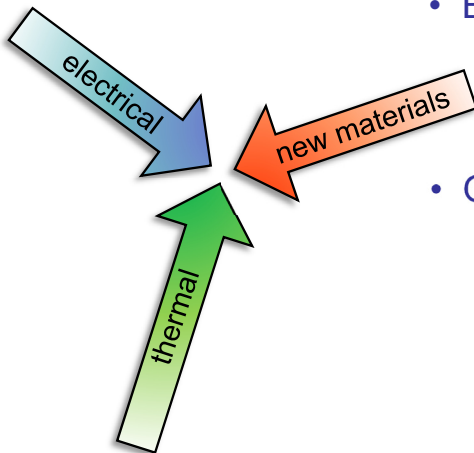
2D Materials to Systems – Future (?)



M. Aly et al., "Energy-Efficient Abundant-Data Computing: The N3XT 1,000X," *IEEE Computer* 48, 24 (2015)

Summary

- Moore's Law ~10x → slowing down
- Energy scaling & harvesting ~10⁴x → exciting



- Opportunity for convergence of:
 - Novel 2D nanomaterials
 - Anisotropic electrical & thermal properties
 - Heterogeneous integration
- From fundamentals to systems
- Collaborations with industry & academia