

Two-Dimensional (2D) Electronics and the SystemX Alliance at Stanford

Eric Pop

Electrical Engineering (EE)

SystemX Alliance and Precourt Institute for Energy (PIE)

Stanford University

<http://poplab.stanford.edu>



Acknowledgements

<http://poplab.stanford.edu>

- **Alumni:**

- Prof. D. Estrada, Drs. Z.-Y. Ong, A. Liao, J. Wood, Z. Li, V. Dorgan, F. Xiong, Z. Li, E. Carrion, S. Islam, K. Grosse
- 8 M.S. and 10 B.S. theses

- **Post-docs:**

- Feng Xiong, Yong Cheol Shin, Eilam Yalon, Miguel Munoz

- **Grad students:**

- C. English, F. Lian, S. Deshmukh, S. Bohaichuk
- M. Mleczek, C. Neumann, I. Datye, M. Chen, A. Gabourie
- K. Smithe, S. Suryavanshi, N. Wang, R.L. Xu, C. McClellan

- **Undergrads:**

- Andrew, Tim, Job, Justin, Yesnar, Erin, Anika, Aria, Stephone

- **Sponsors:**

- National Science Foundation (NSF), Army Research Office (ARO)
- Air Force (AFOSR), Intel, STARnet-SONIC, **SystemX Alliance**

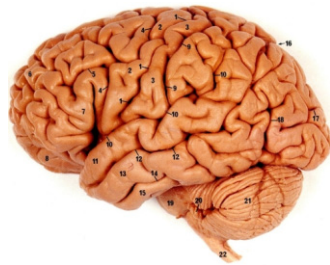
- **Collaborators:**

- Z. Bao, K. Goodson, S. Mitra, Y. Nishi, E. Reed, K. Saraswat, H.-S.P. Wong (Stanford), D. Cahill, W. King, J. Lyding, J. Rogers, M. Shim (UIUC), M. Rudan (Bologna), C. Jacoboni (Modena), M. Hersam (NWU), I. Knezevic (Wisc.), D. Jena (Cornell), D. Ielmini, R. Sordan (Milano), J. Shiomi (Tokyo)



What Motivates Us

(IBM Watson, *Jeopardy!* champion)



20 Watts



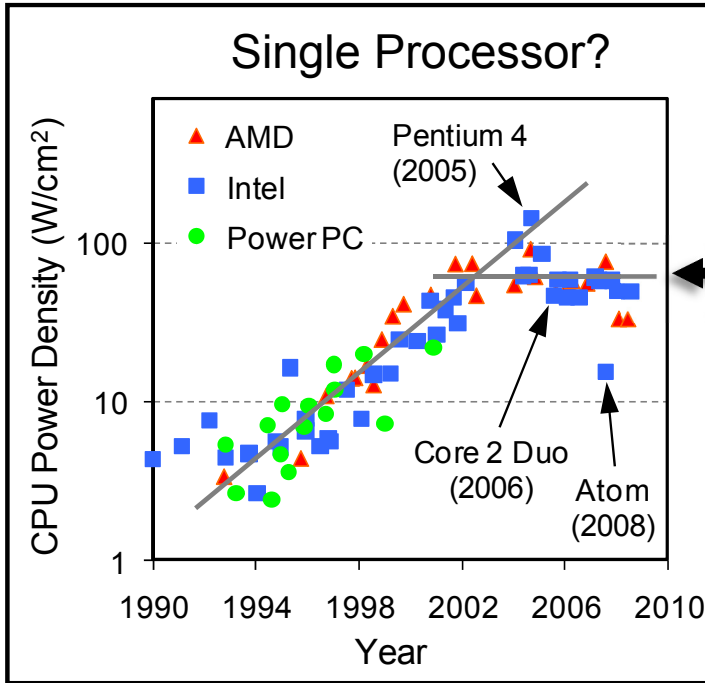
200 kiloWatts

10,000x

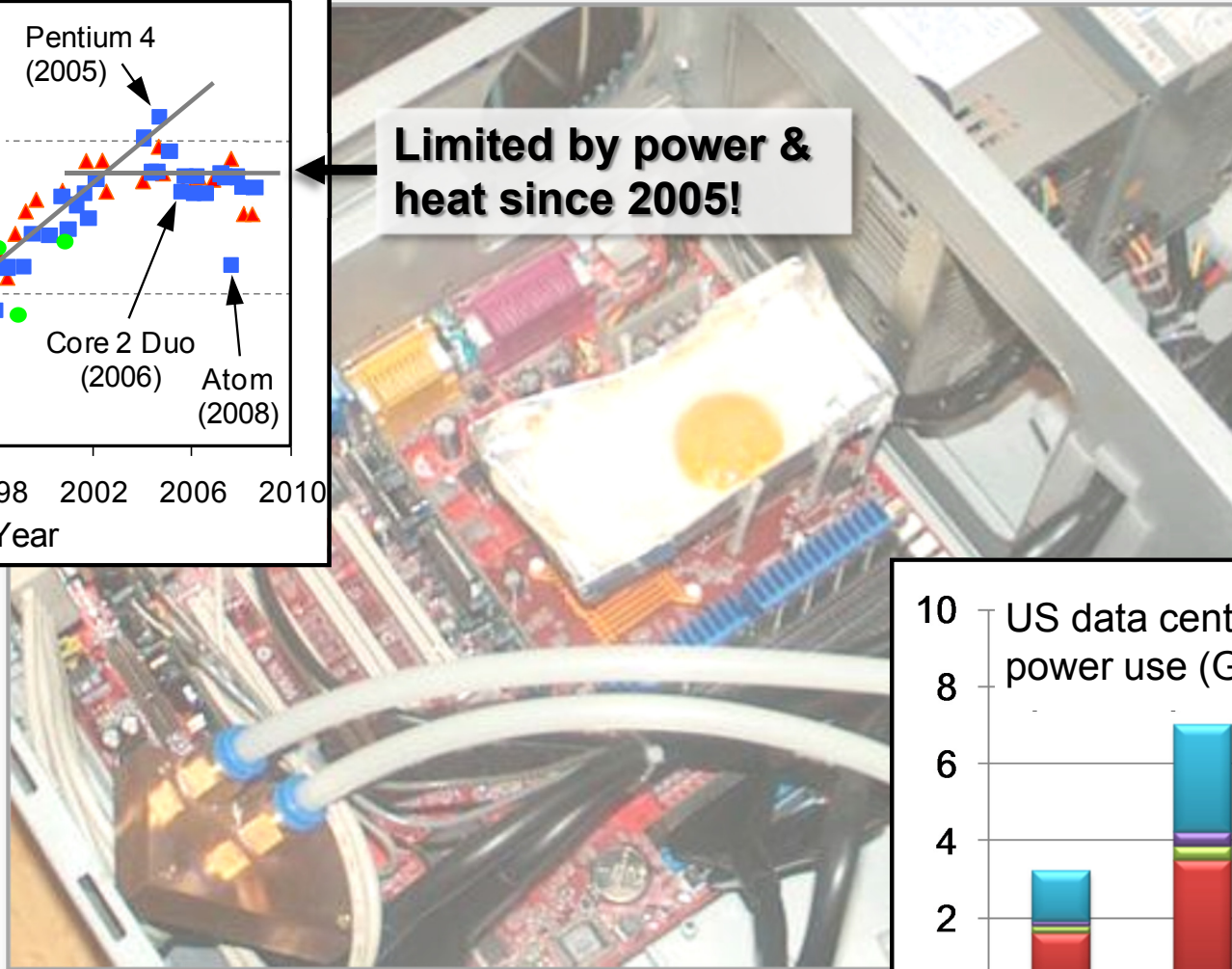
(conventional Moore's Law size scaling can get us ~10x)

Electronics Use (and Waste) Much Power

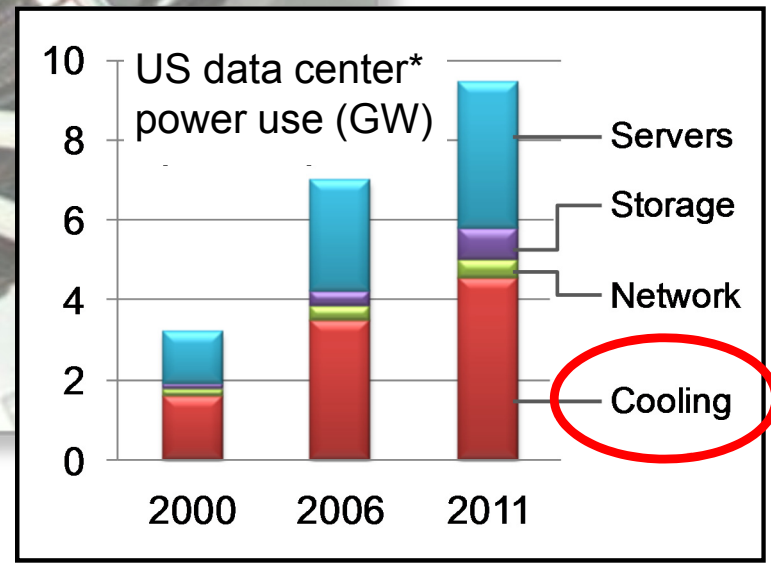
E. Pop, *Nano Research* 3, 147 (2010)
 new course: Energy in Electronics, EE 323 (Fall 2014)



Limited by power & heat since 2005!



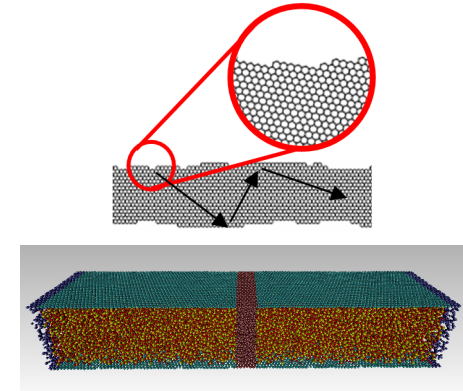
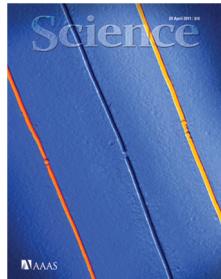
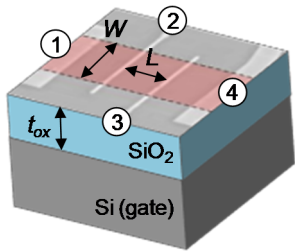
J. Koomey (Stanford)



Calibrating: 1 GW ~ 1 nuclear power plant
 12 GW ~ all electricity used by Argentina

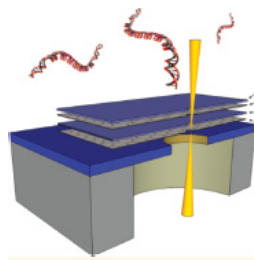
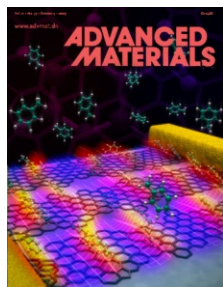
*World-Wide about 30 GW

Our Work: Two Sides of the Same Coin



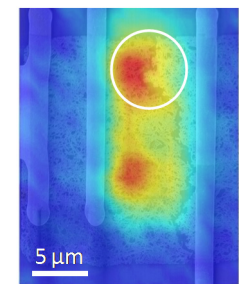
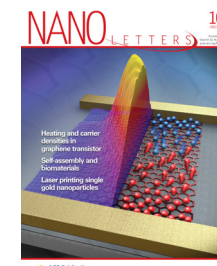
Lower power at its source

(devices, sensors, circuits)



Harvest and manage heat

(energy, thermoelectrics)



fundamental understanding
practical applications

Outline of Talk

- **The SystemX Alliance at Stanford**

- **2D Materials**

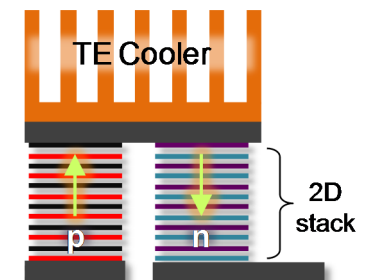
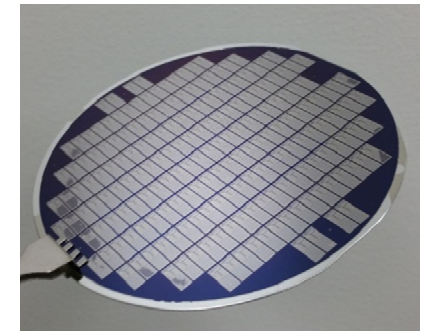
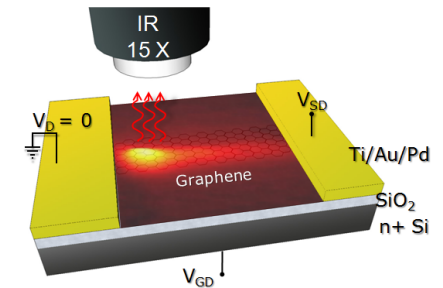
- Structure and energy bands

- **Devices to Systems**

- Transport properties and integration

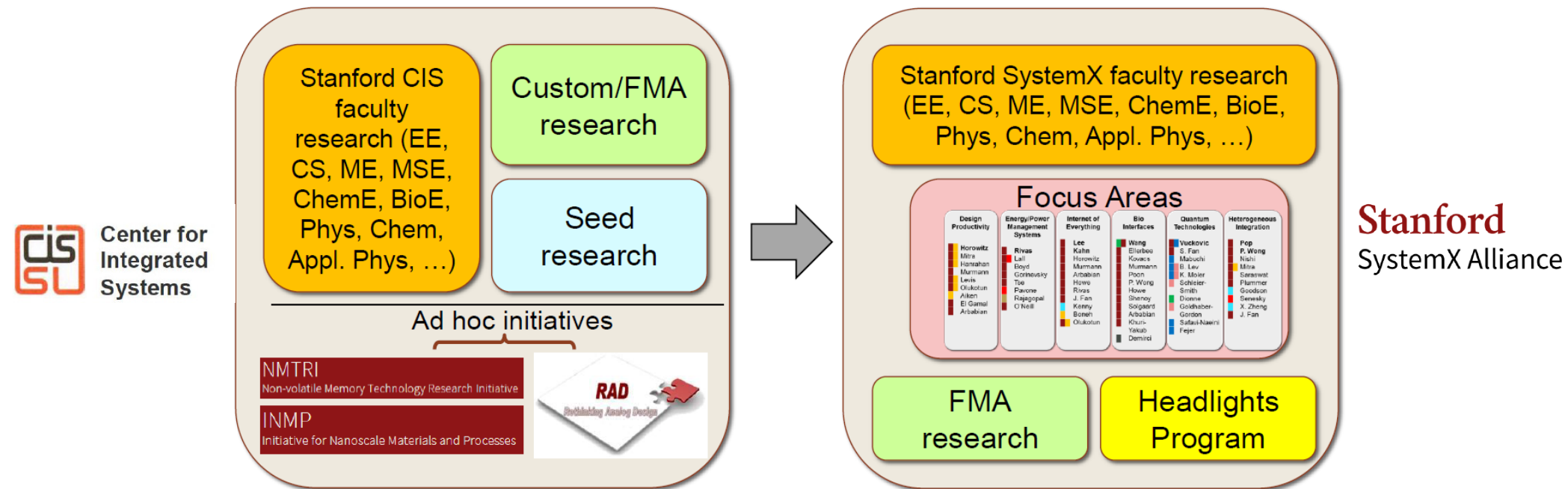
- **Thermal Energy at Nanoscale**

- Fundamental limits & looking ahead



What Is the SystemX Alliance at Stanford?

- Center for Integrated Systems (CIS) → SystemX Alliance
 - Industry-academic Alliance to repositioned for 21st century research
 - Become “the” hub for electronic research at Stanford



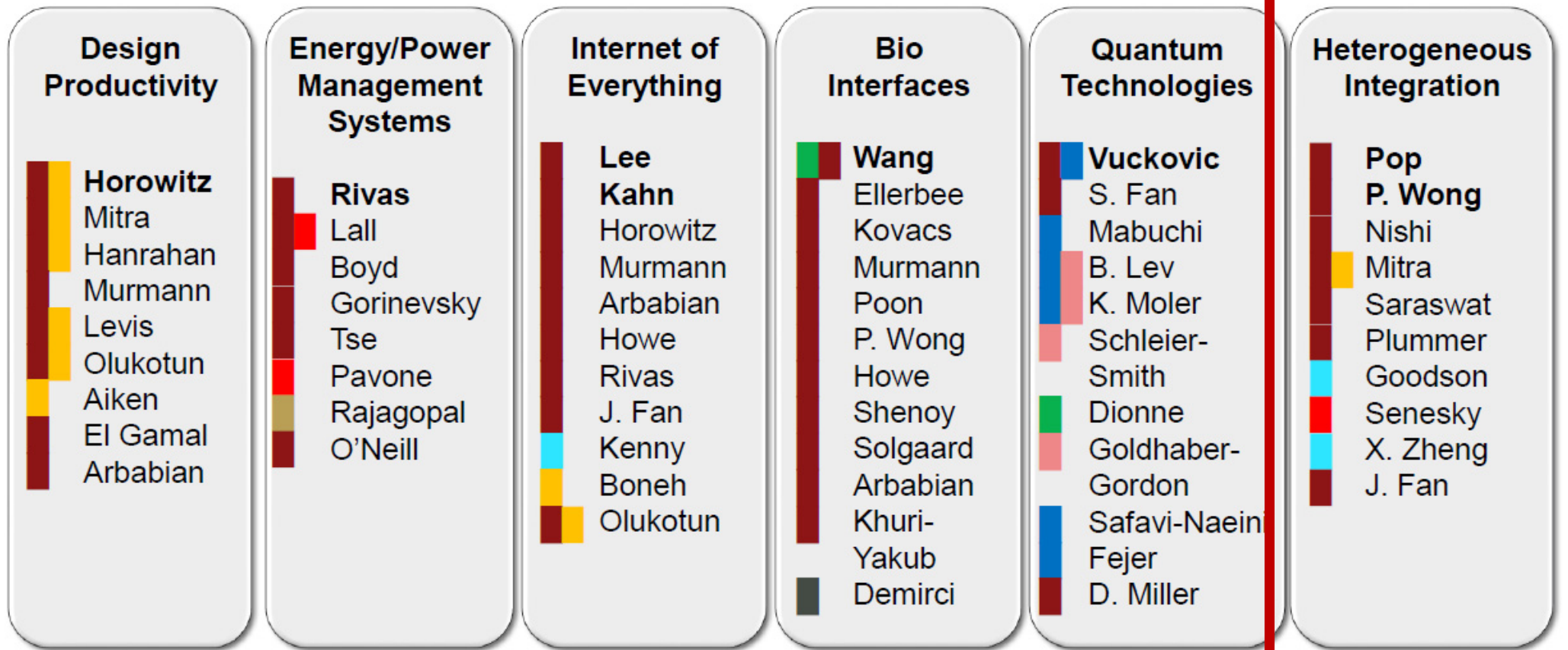
- What's New?
 - Stronger emphasis of top-down, **systems research**
 - Introduce **focus areas** to create coherent thrusts
 - Additional **sponsor benefits** including workshops, E-Seminars

Value Proposition for Industry Sponsors

- See **everything** that is going on at Stanford
 - Real-time **view of all faculty research**, including NSF, DARPA, etc. activities
 - **Student** recruiting, internships, and networking
- Participation in Focus Area research
 - Invitation-only attendance to **bi-annual workshop** & discussion
- Customized Fellow-Mentor-Advisor (FMA) projects
 - **Company-specific research** performed by student & advisor with industry mentor
- Faculty liaisons, company visits, and weekly **E-Seminars**



SystemX Focus Areas

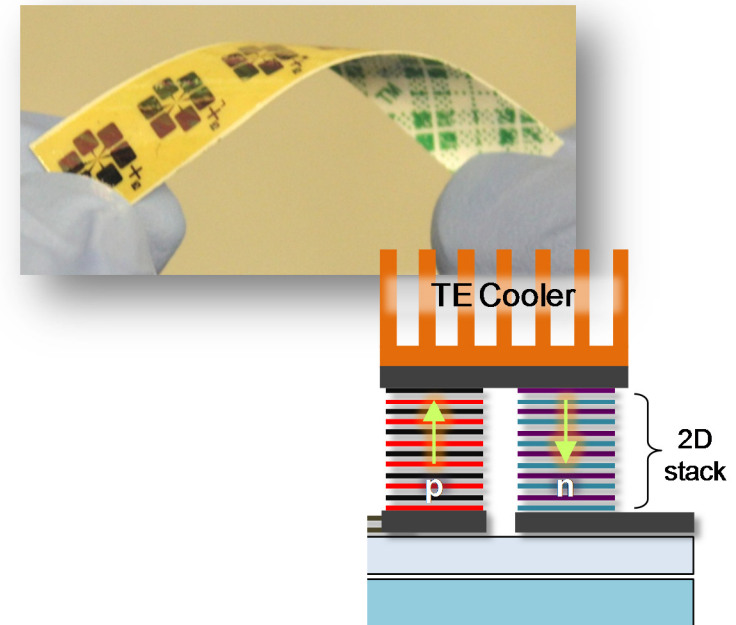
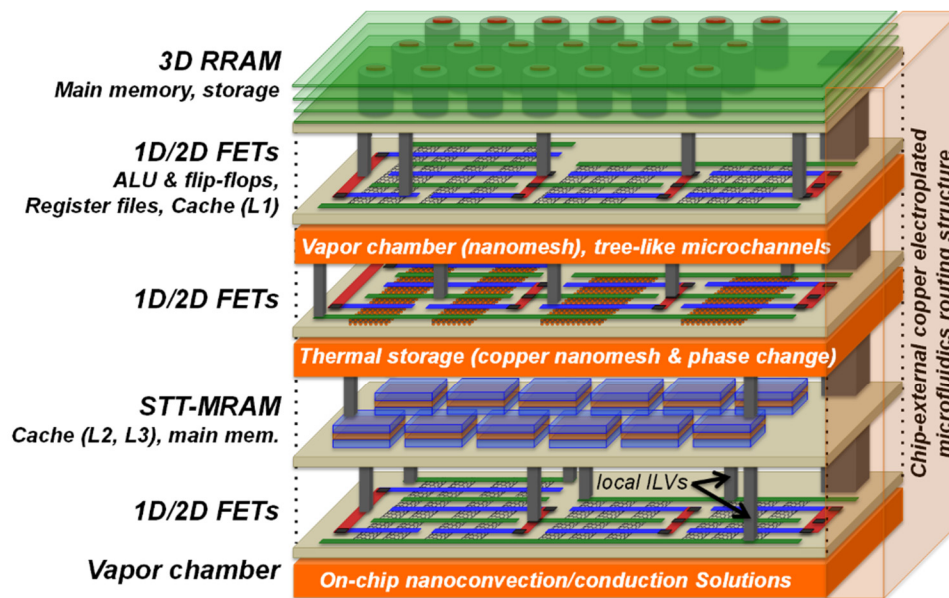


■ = EE ■ = ME ■ = AP ■ = CEE ■ = Radiology
■ = CS ■ = MSE ■ = PHY ■ = AA

- Focus areas change dynamically and have finite life-cycle (~3-5 years)

Heterogeneous Integration Focus Area

- Heterogeneous Integration (HI)
- Integration of “beyond-Si” platforms for “beyond Moore” applications
 - Monolithic integration of logic, memory, sensors, thermal management, flexible substrates
 - Energy-efficient and energy-harvesting design opportunities



- Core faculty: E. Pop, H.-S.P. Wong (co-leads), J. Fan, K. Goodson, S. Mitra, Y. Nishi, J. Plummer, K. Saraswat, D. Senesky, X. Zheng

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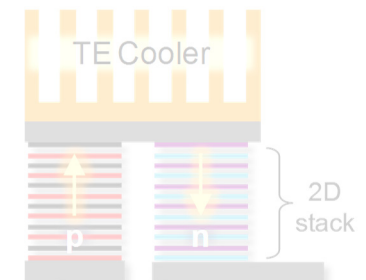
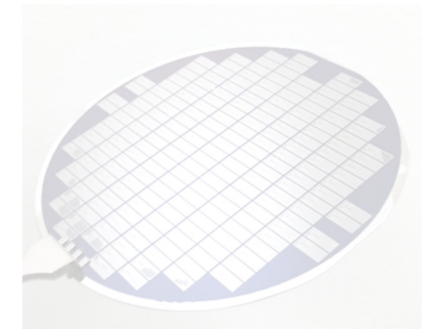
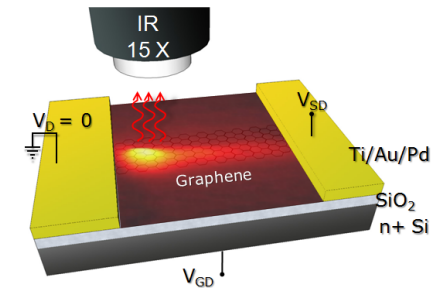
- Structure and energy bands

- Devices to Systems

- Transport properties and integration

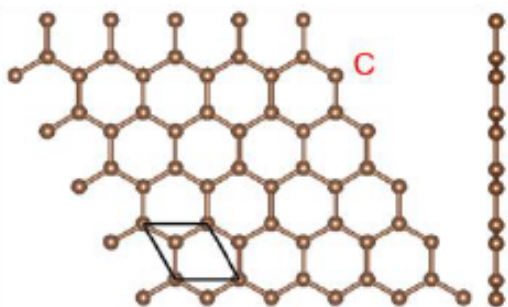
- Thermal Energy at Nanoscale

- Fundamental limits & looking ahead

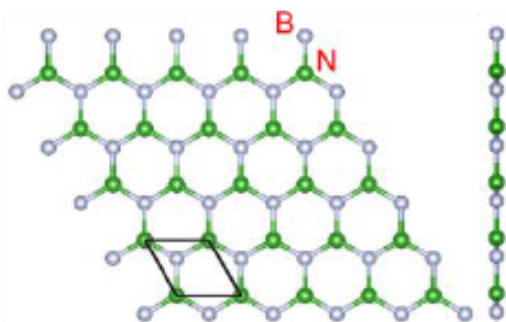


Atomic Structure of Some 2D Materials

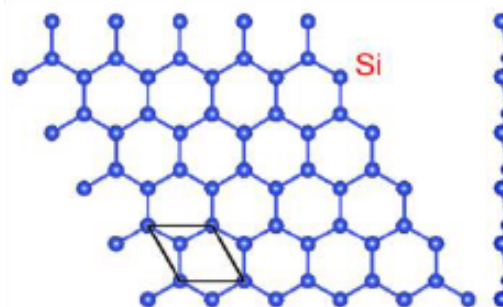
(a) graphene



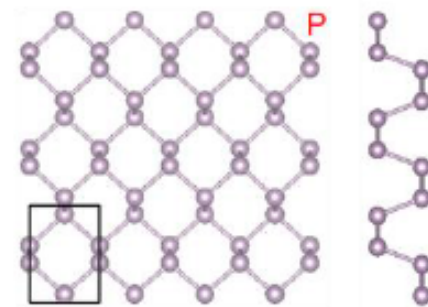
(b) Boron nitride



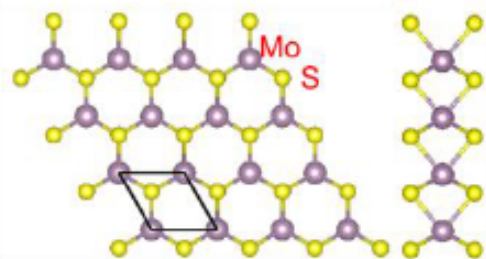
(c) silicene



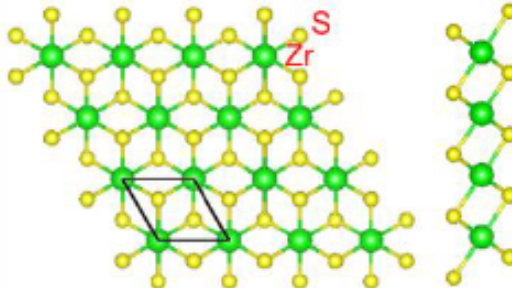
(d) Black phosphorus



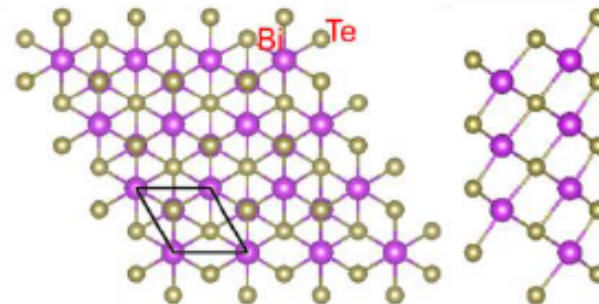
(e) 2H transition metal dichalcogenides: MoS₂



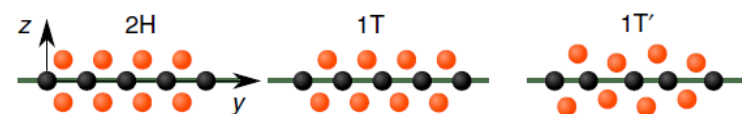
(f) 1T transition metal dichalcogenides: ZrS₂



(g) Bismuth telluride



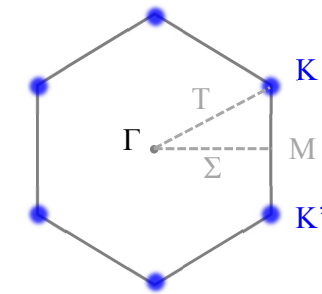
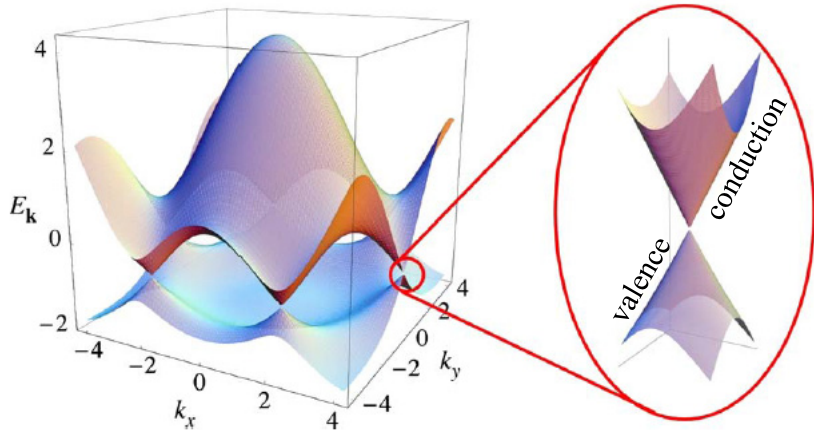
- 2D lattices can be planar (graphene, BN), buckled (Xenes), 1T, 2H, 3R
- Transition metal dichalcogenides (TMDs) are 2H or 1T(')
- Phase change 2H (semic.) to 1T or 1T' (metallic) by ΔT , strain or Li intercalation.



M. Chhowalla et al., *Nat. Chem.* **5**, 263 (2013)
 Duerloo et al., *Nat. Comm.* **5**, 4214 (2014)

Electronic Band Structure of 2D Materials

graphene: semimetal



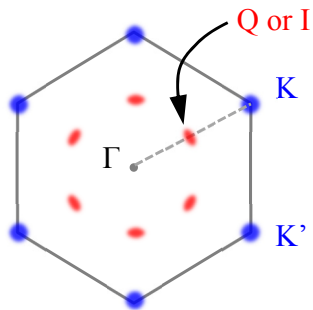
$$E = \hbar v_F k$$

$$v_F \approx 10^6 \text{ m/s}$$

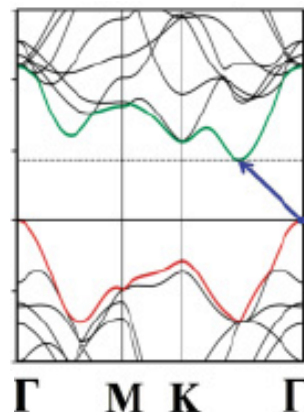
$K = K'$ degeneracy

Castro-Neto, Rev. Mod. Phys. (2009)

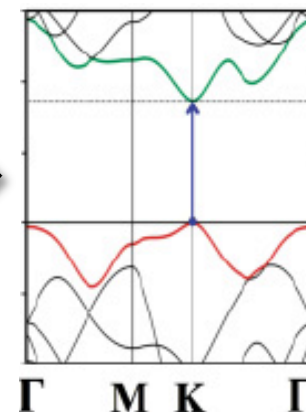
MX₂ TMDs



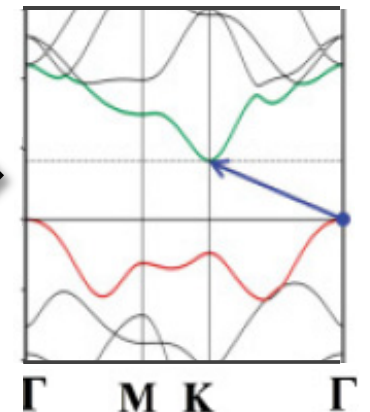
**Bulk MoS₂
(indirect gap)**



**1L MoS₂
(direct gap)**



**1L MoS₂
(tensile strain*)**



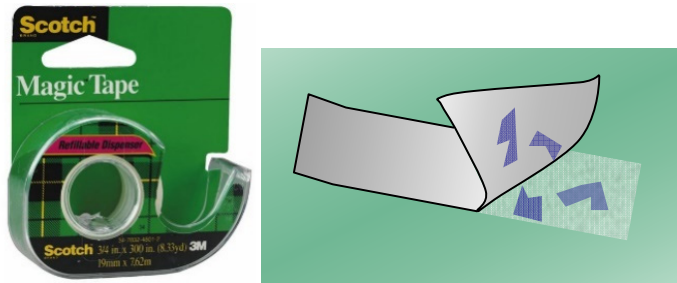
$K = 2x$ degenerate

$Q = 6x$ degenerate (along T line, sometimes mislabeled Σ)

(*little is known about strain)

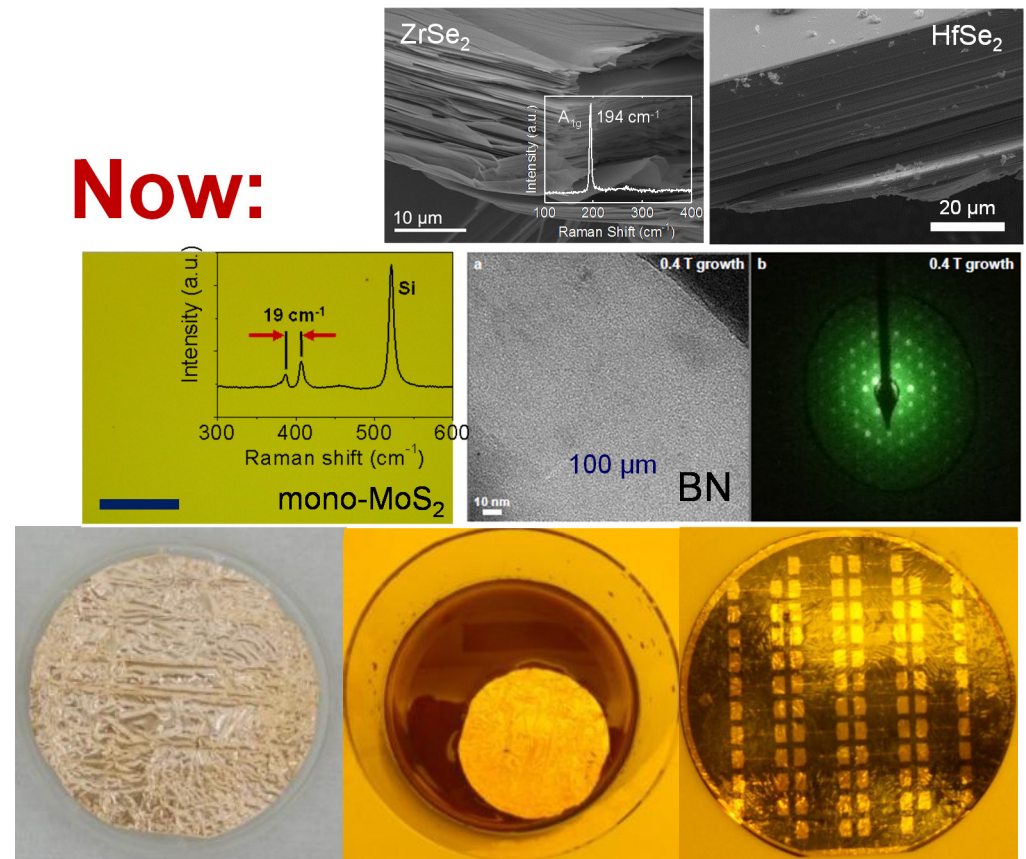
Huge Advances in Synthesis

Then:



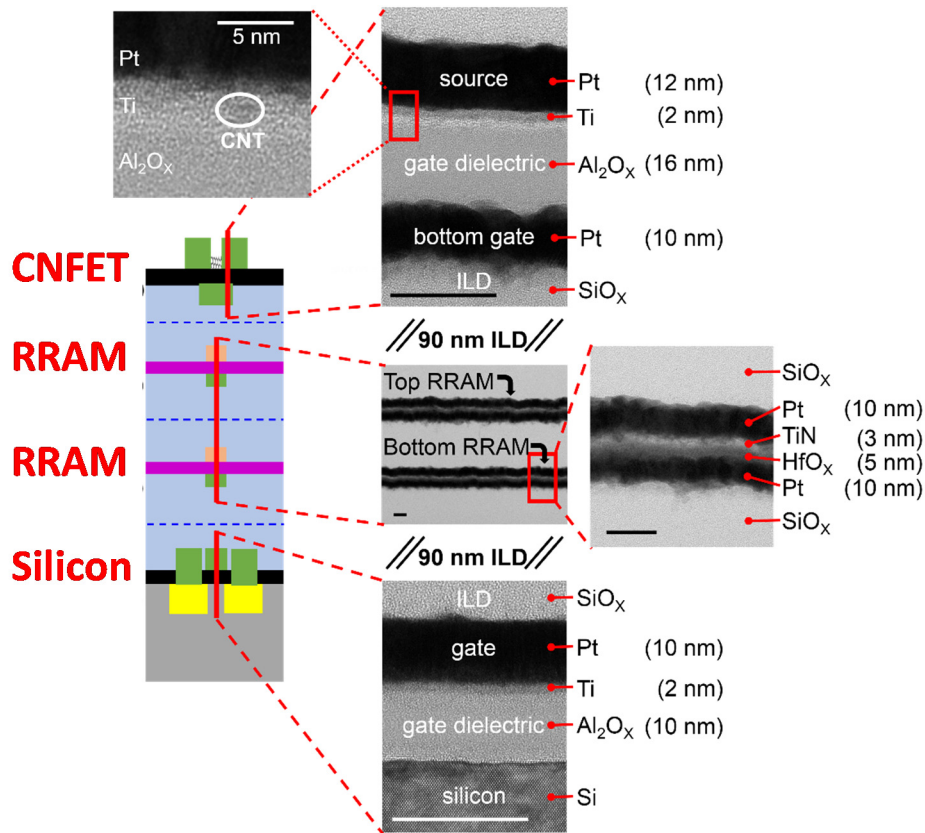
random $\sim 10 \mu\text{m}$ pieces

Now:



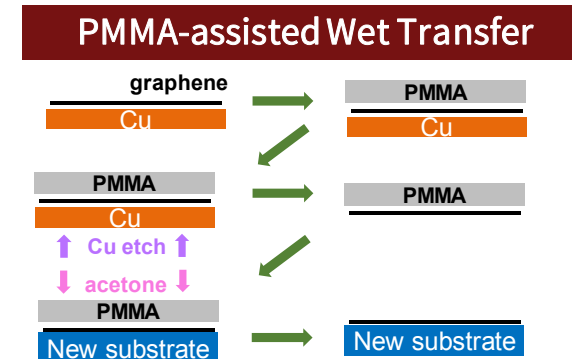
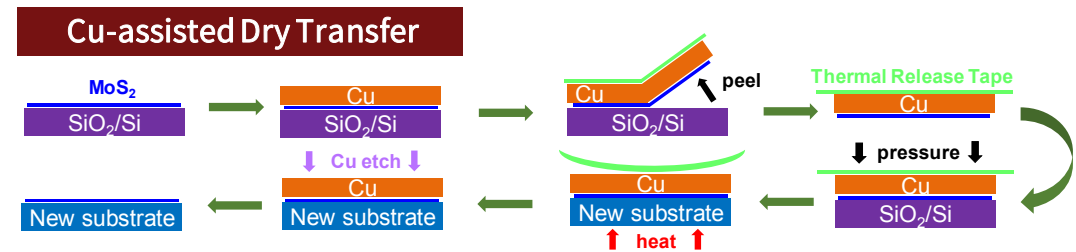
wafer-scale chemical vapor deposition (CVD)

Huge Advances in Heterogeneous Integration



Monolithic 3D: low-temperature 3D integration of CNT logic and RRAM memory on CMOS substrate

source: Shulaker, Wong, Mitra (IEDM-2014)

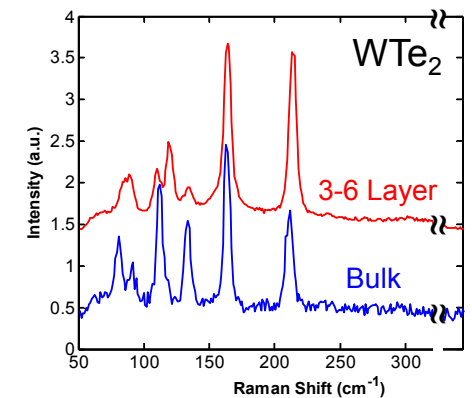
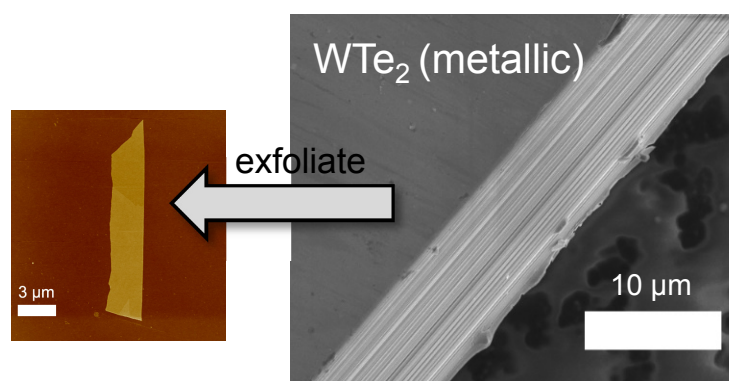
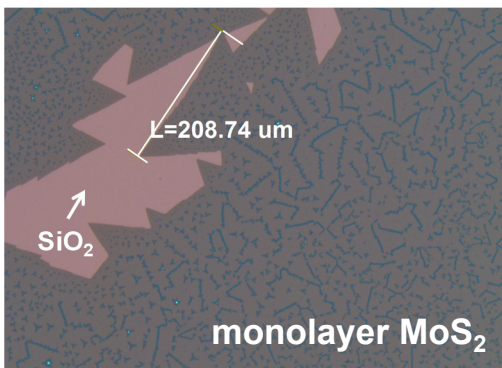
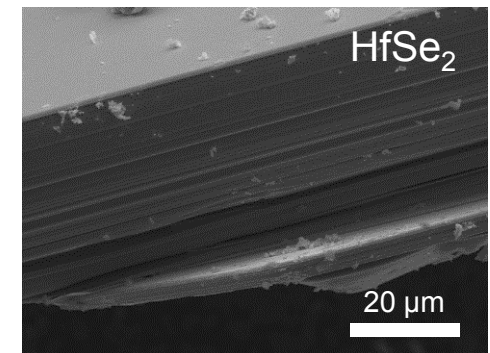
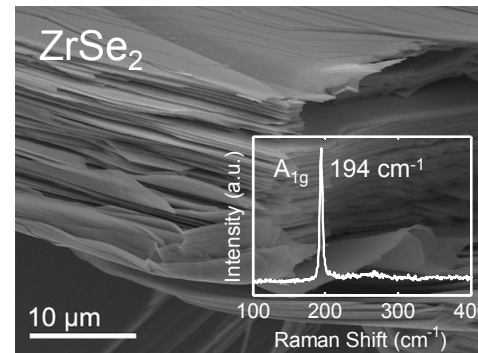
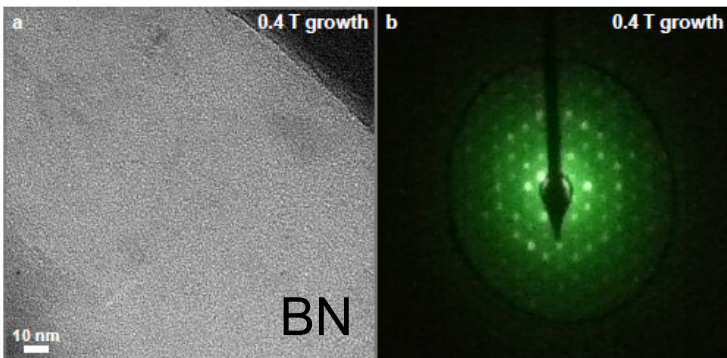
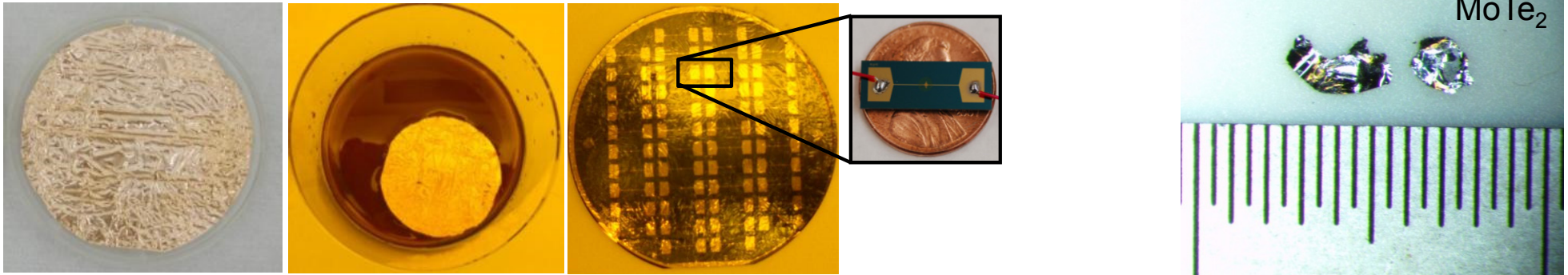


Wet or Dry Transfer: layer transfer of 2D monolayers onto insulators while preserving the electronic properties

source: K. Smithe (Pop Lab, 2015)

2D Materials at Stanford

CVD growth of monolayer graphene, BN and MoS₂



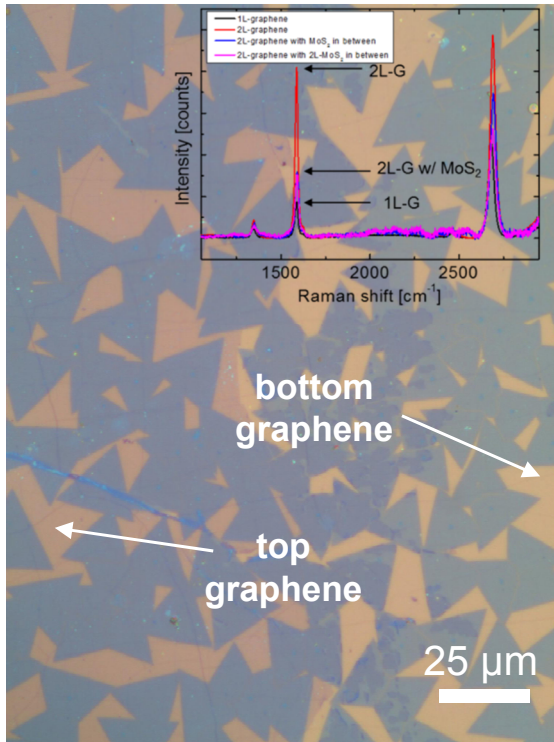
E. Pop, H.-S.P. Wong, Y. Nishi, I. Fisher

CVT growth of MoTe₂, WTe₂, ZrSe₂, HfSe₂

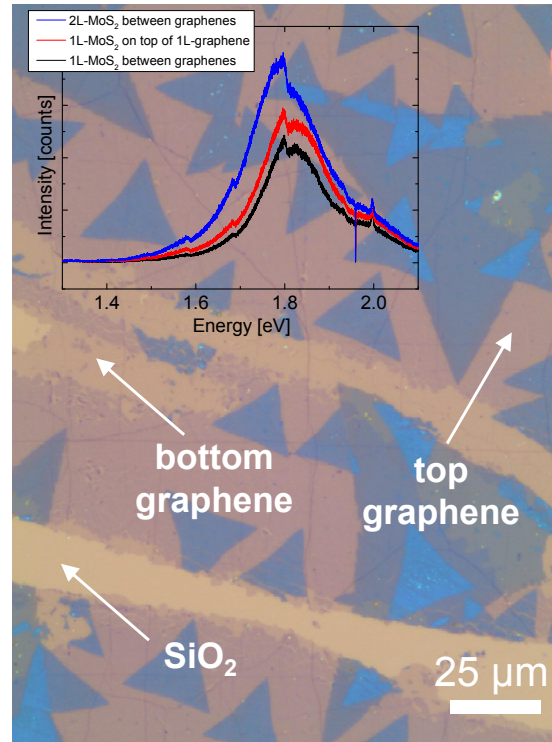
Heterostructures from 2D Monolayers

work of Y.C. Shin (Pop Lab)

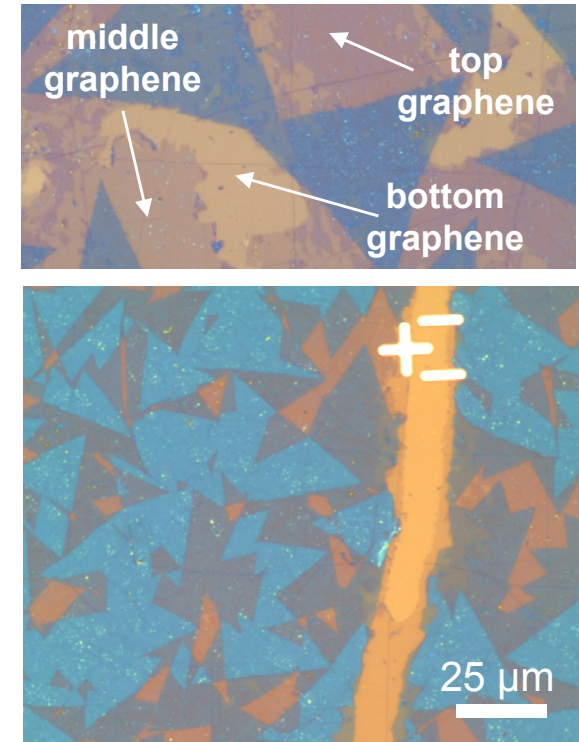
Graphene/MoS₂/Graphene



Graphene/MoS₂/MoS₂/Graphene



Graphene/MoS₂/Graphene/MoS₂/Graphene



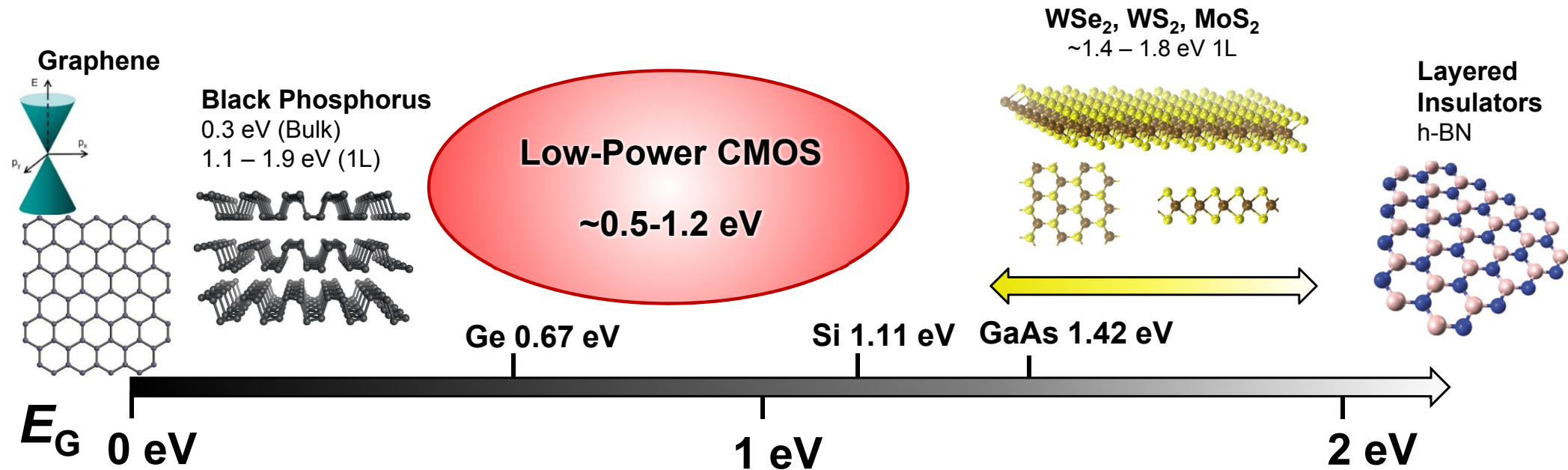
- Unusual out-of-plane thermal and electrical properties
- Thermal characterization underway (with Ken Goodson group)
- Electrical and thermoelectric characterization under development

Band Gaps (E_G) of Several 2D Materials

courtesy of M. Mleczko (Pop Lab)

High-Speed / RF

Power Devices



- Low- E_G but high mobility \rightarrow high-speed and RF applications
- Medium- E_G (0.3 to 1.1 eV) \rightarrow low-power CMOS
- High- E_G \rightarrow power devices

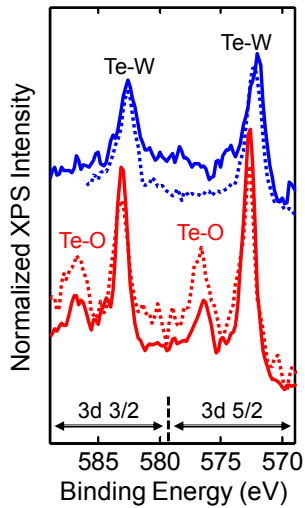
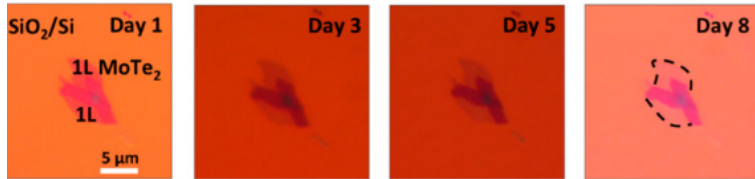
Ambient Stability of 2D Materials*

courtesy of M. Mleczko (Pop Lab)

*monolayers will be least stable

MoTe₂

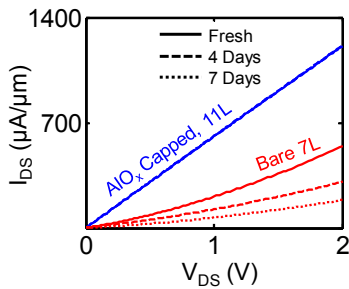
B. Chen et al., *ACS Nano* 9, 5326 (2015)



— Capped Fresh
 Capped 7 Days
 — Bare Fresh
 Bare 7 Days

WTe₂

M. Mleczko et al. (2016)



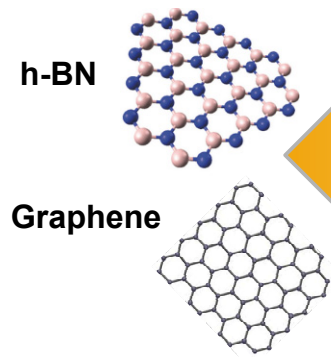
	-S ₂	-Se ₂	-Te ₂
Mo			
W			
Nb, Sn			
Hf, Zr Ta, Ti			



Black Phosphorus

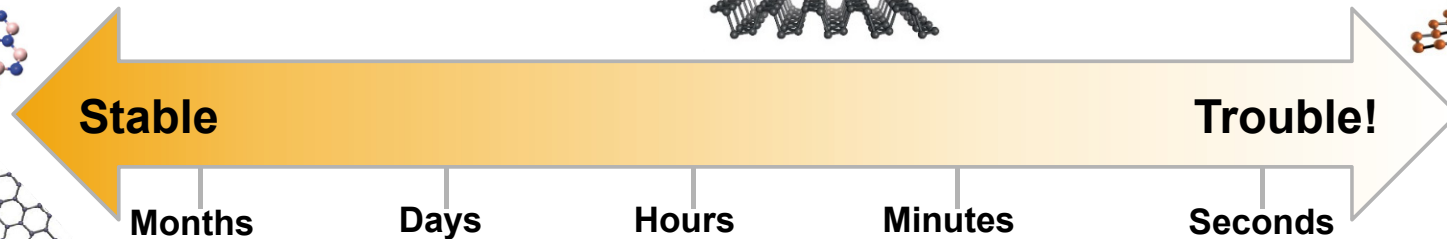


Silicene, Stanene...



h-BN

Graphene

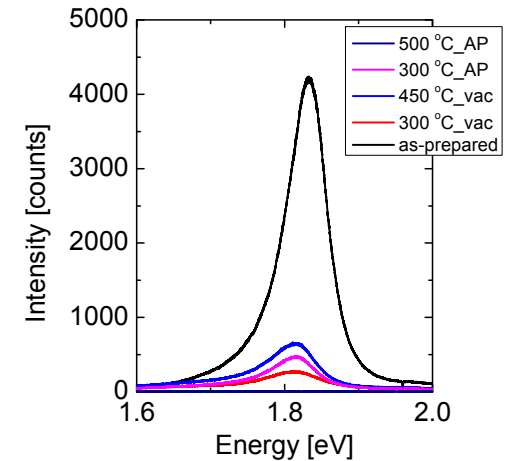
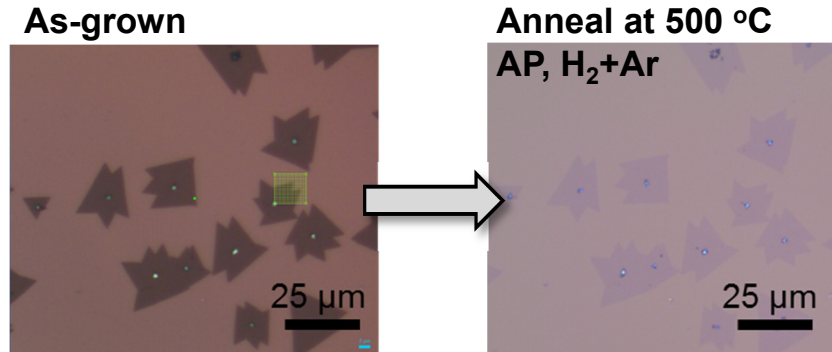
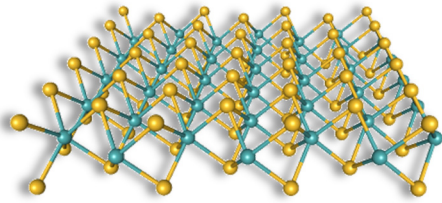


Time Scale of Degradation

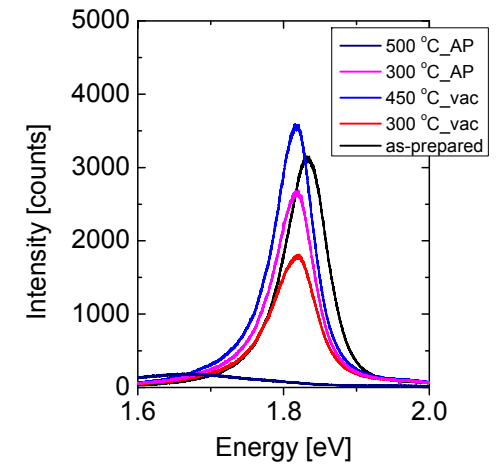
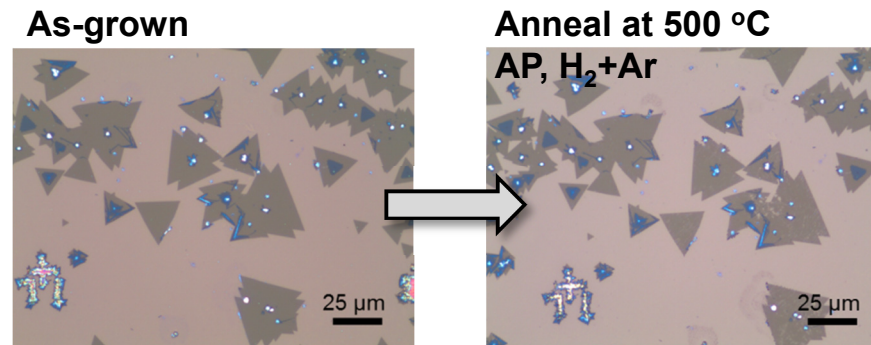
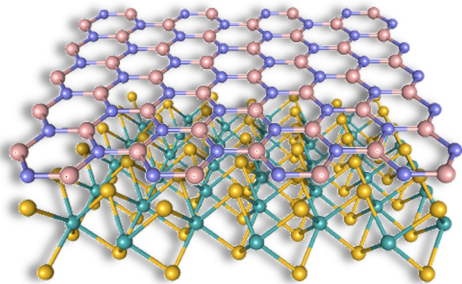
Enhanced Stability by Capping with h-BN

work of Y.C. Shin (Pop Lab)

Unprotected MoS₂



h-BN capped MoS₂



- Monolayer h-BN protects monolayer MoS₂ up to ~500 °C
- AlO_x (by ALD) can also be used as encapsulation layer (but can dope)

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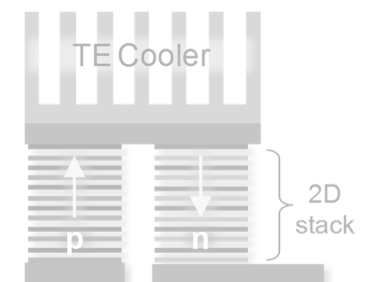
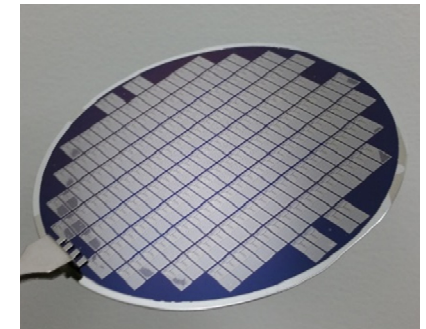
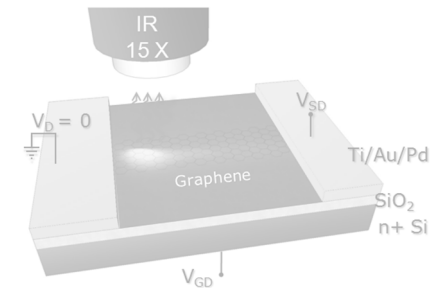
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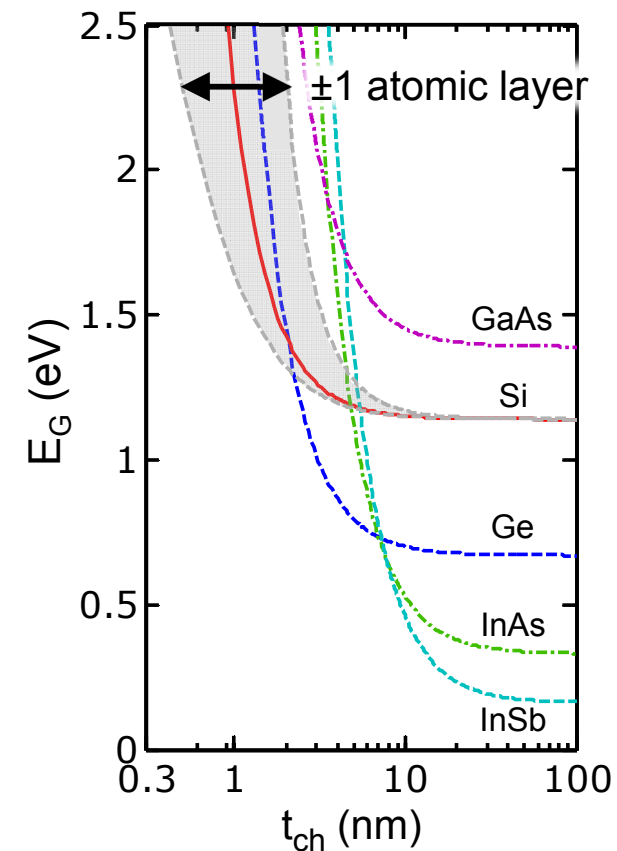
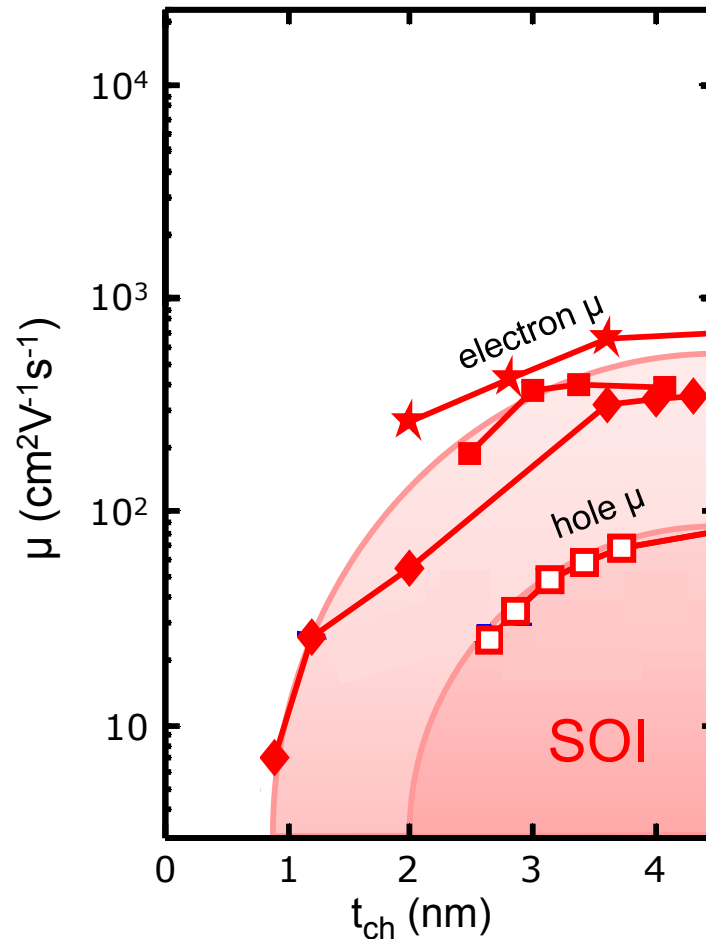
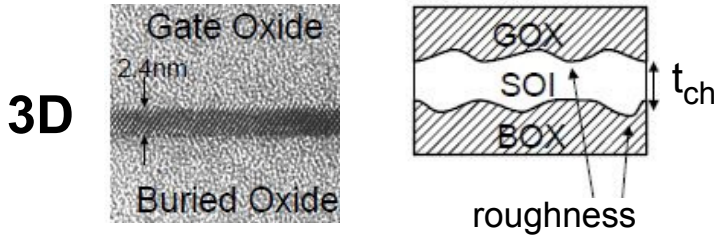
- Thermal Energy at Nanoscale

- Fundamental limits & looking ahead



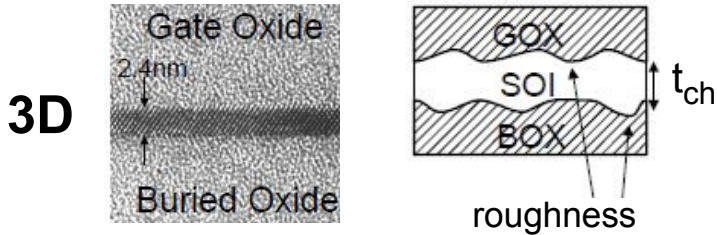
Transistors Beyond Silicon?

- Problem:** 20th century transistors “carved” out of **3D** materials (Si) → surface roughness restricts mobility, band gap, variability



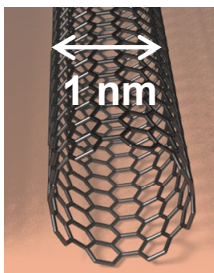
Transistors Beyond Silicon?

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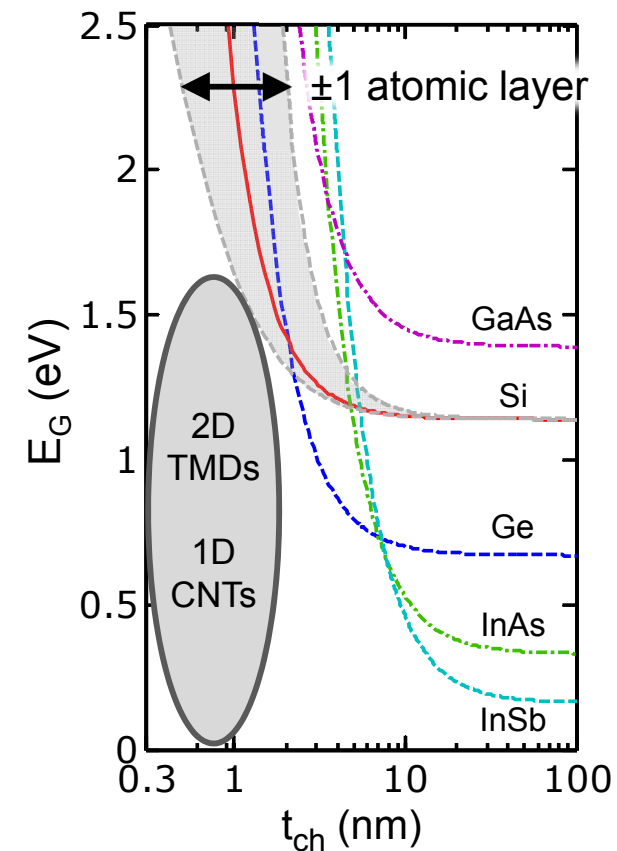
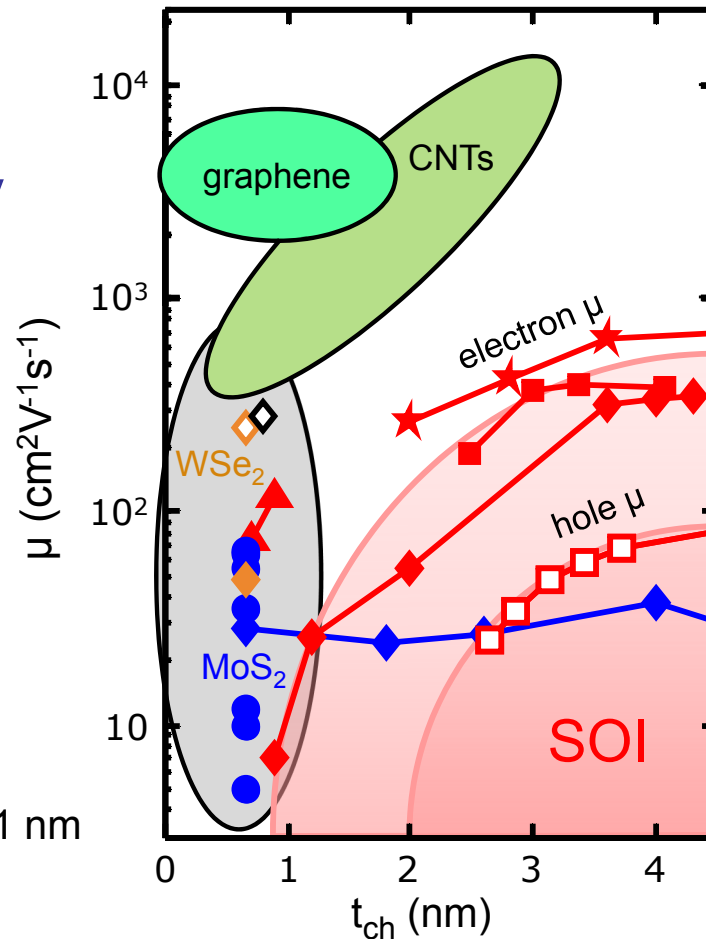
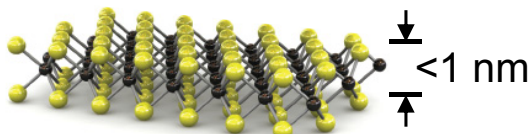


- Solution?** 21st century atomically thin materials

1D carbon nanotube (CNT)

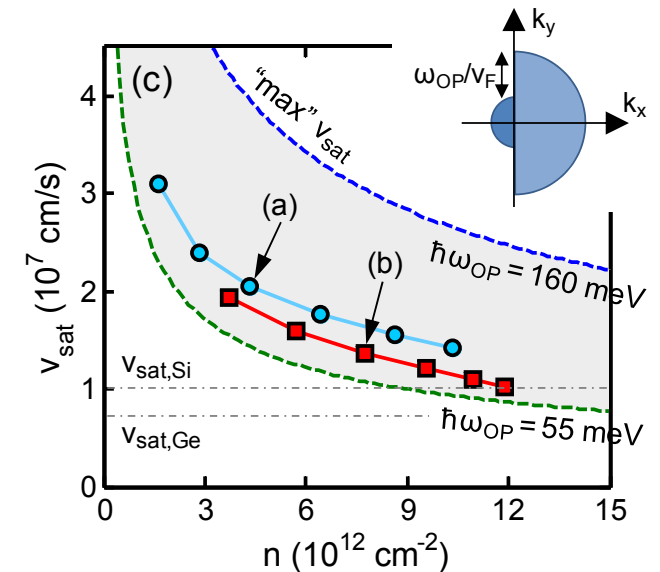
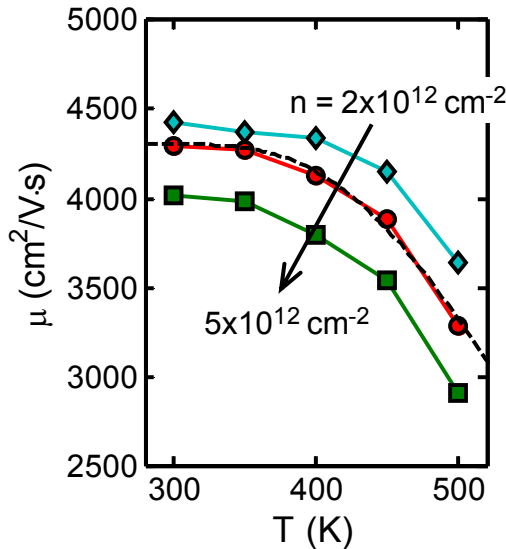
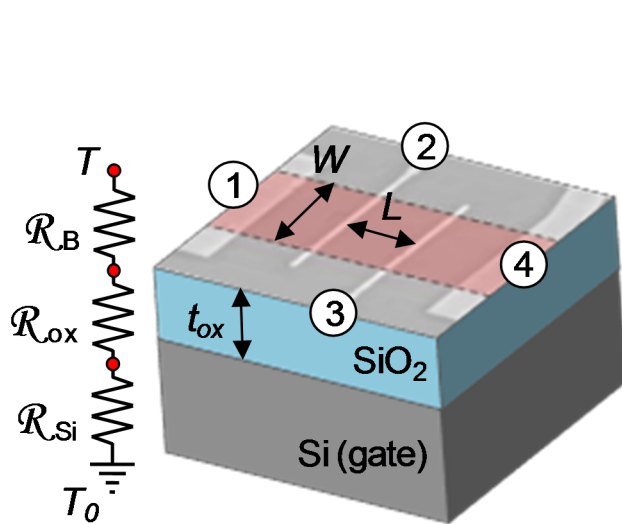


2D TMD (MoS₂, WTe₂, ZrSe₂)



Early Work: Graphene Transport Parameters

V. Dorgan, M.-H. Bae, E. Pop, *Appl. Phys. Lett.* 97, 082112 (2010)



$$\Delta T = T - T_0 \approx P(\mathcal{R}_B + \mathcal{R}_{ox} + \mathcal{R}_{Si})$$

$$\mu(n, T) = \frac{\mu_0}{1 + (n/n_{ref})^\alpha} \times \frac{1}{1 + (T/T_{ref} - 1)^\beta}$$

$$v_{sat}(n, T) = \frac{2}{\pi} \frac{\omega_{OP}}{\sqrt{\pi n}} \sqrt{1 - \frac{\omega_{OP}^2}{4\pi n v_F^2} \frac{1}{N_{OP} + 1}}$$

- Lack of transport data* at $T > 300$ K and high-field $v_{sat} (>1$ V/ μ m)
- High-field v_{sat} measurement is tricky, needs constant field
- Also extracted practical electrical and thermal compact models

*J.-H. Chen, *Nature Nano* (2008); W. Zhu, *PRB* (2009); I. Meric, *Nature Nano* (2008)

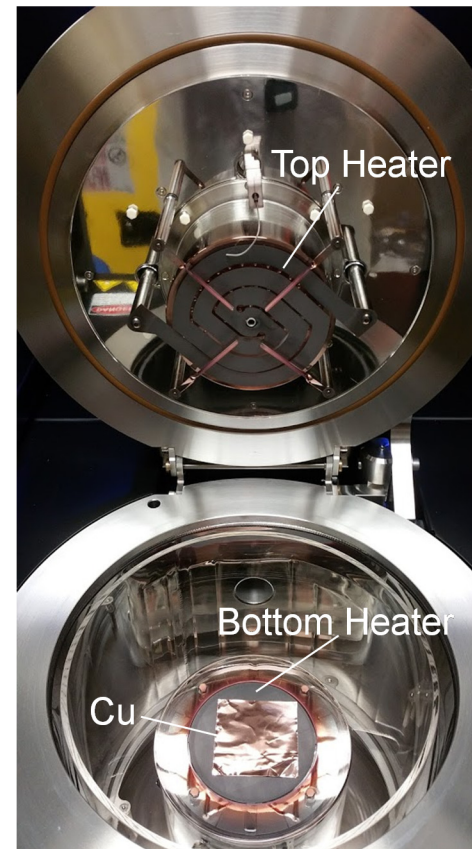
Today: Graphene-Based Functions and Systems

- Goal: graphene switched analog circuit (SAC). Why?
- Graphene = nanofabrics with high mobility ($\sim 10\times > \text{Si}$), flexible...
- SAC tolerates low $I_{\text{on}}/I_{\text{off}}$ ratio ($\sim 5\times$) of graphene (no band gap)
- Breakthroughs in heterogeneous integration of graphene & CMOS

4" Aixtron
Black Magic
System



Growth
Chamber

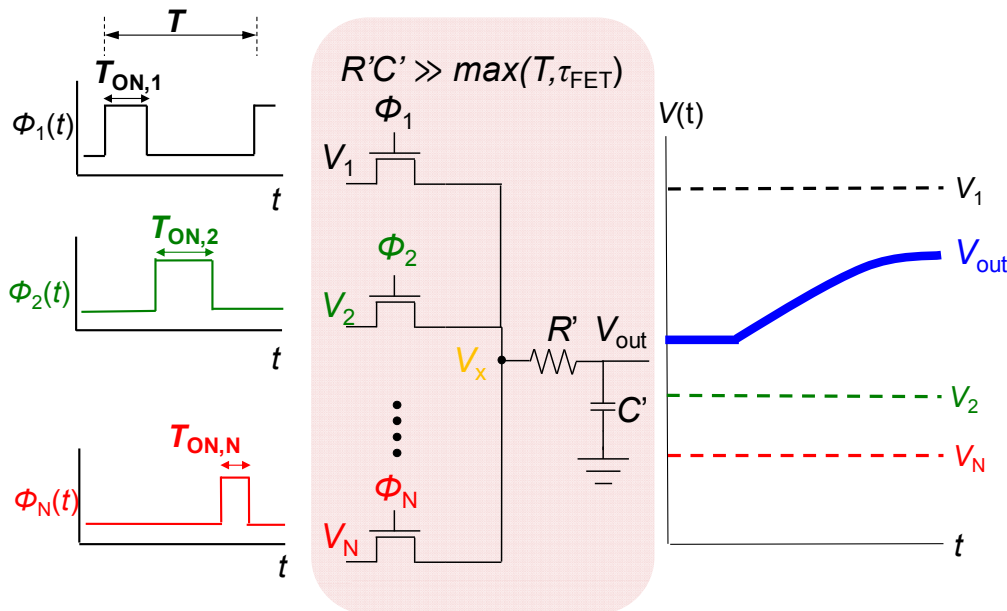


Graphene Dot Product (GDOT) Nanofunction

N. Wang, S. Gonugondla, I. Nahlus, N. Shanbhag, E. Pop, *VLSI Symp.* (2016)

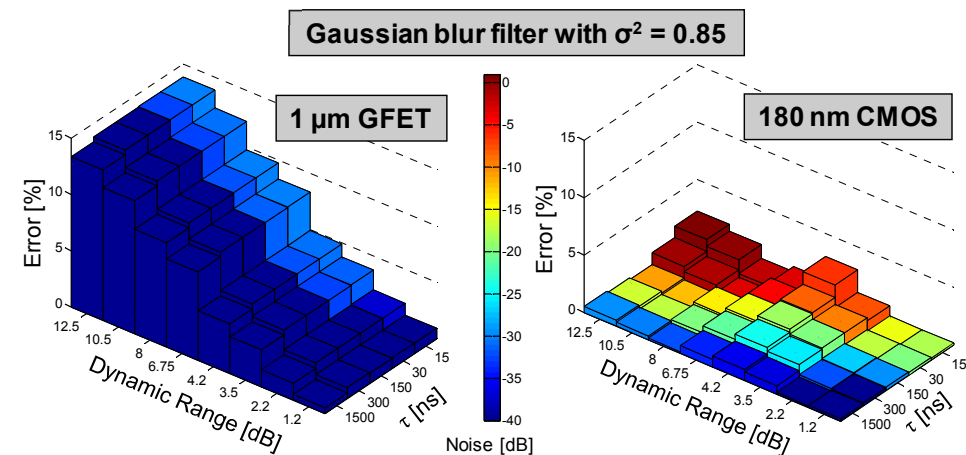
- Dot product nanofunction used for image processing, neural networks...
- Takes advantage of native graphene properties, tolerates drawbacks

Idea:



weights encoded by pulse widths $p_i T$

Simulation:

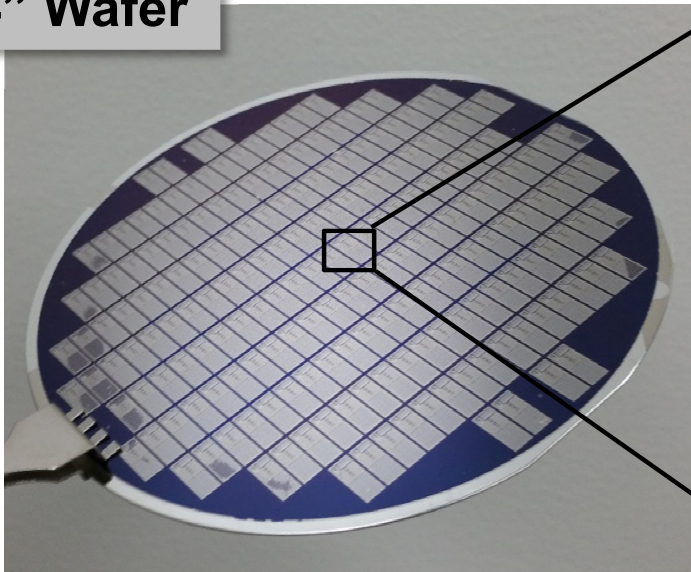


- + Fast
- + Smaller area
- + Low noise
- Narrow input range

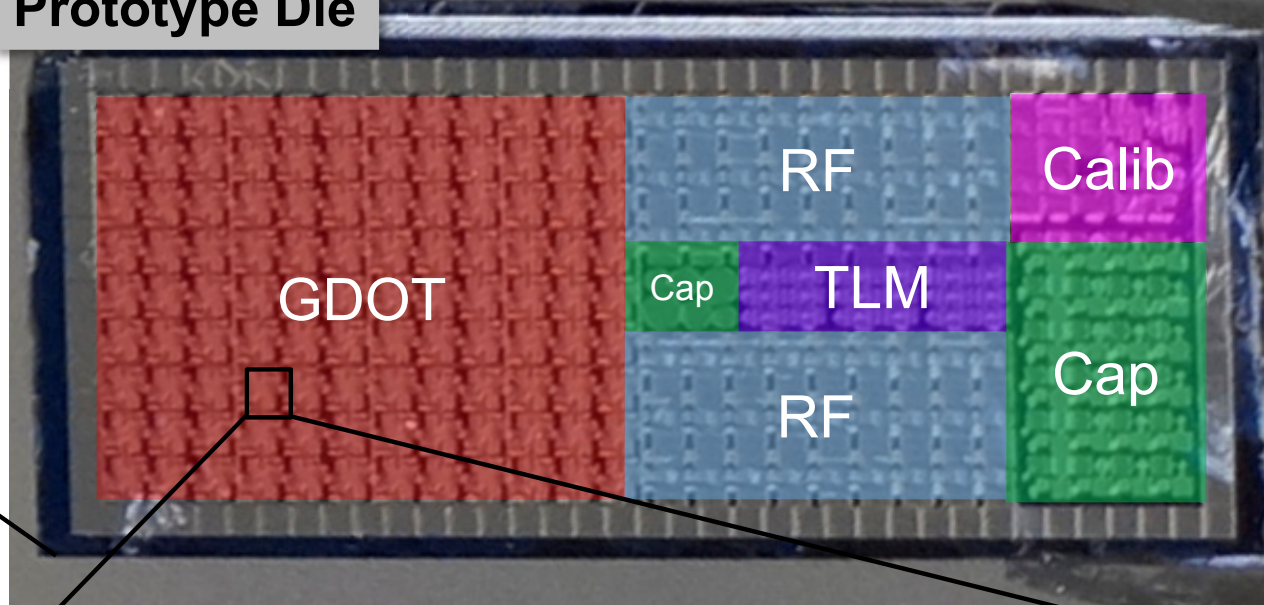
- + High accuracy
- + Wide input range
- Slow and noisy
- Larger area

... and Implementation

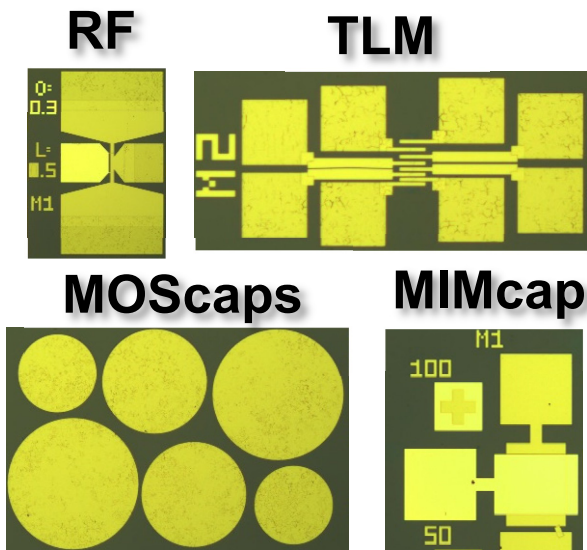
4" Wafer



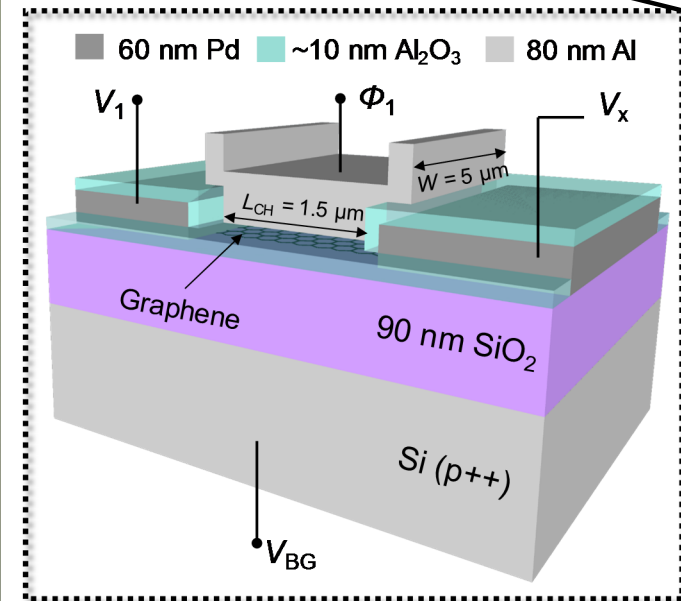
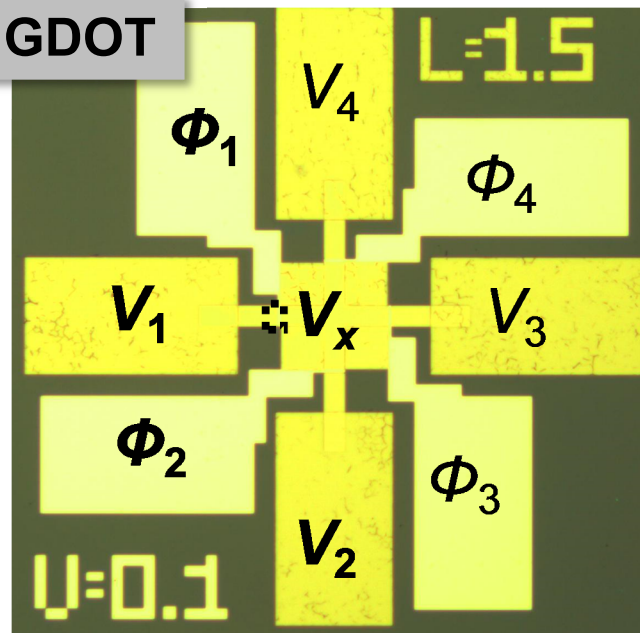
Prototype Die



Test Structures

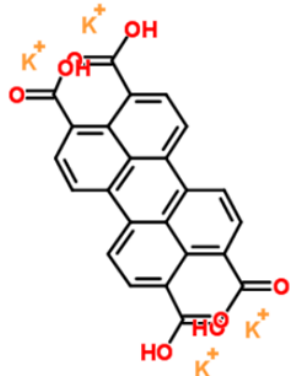


GDOT

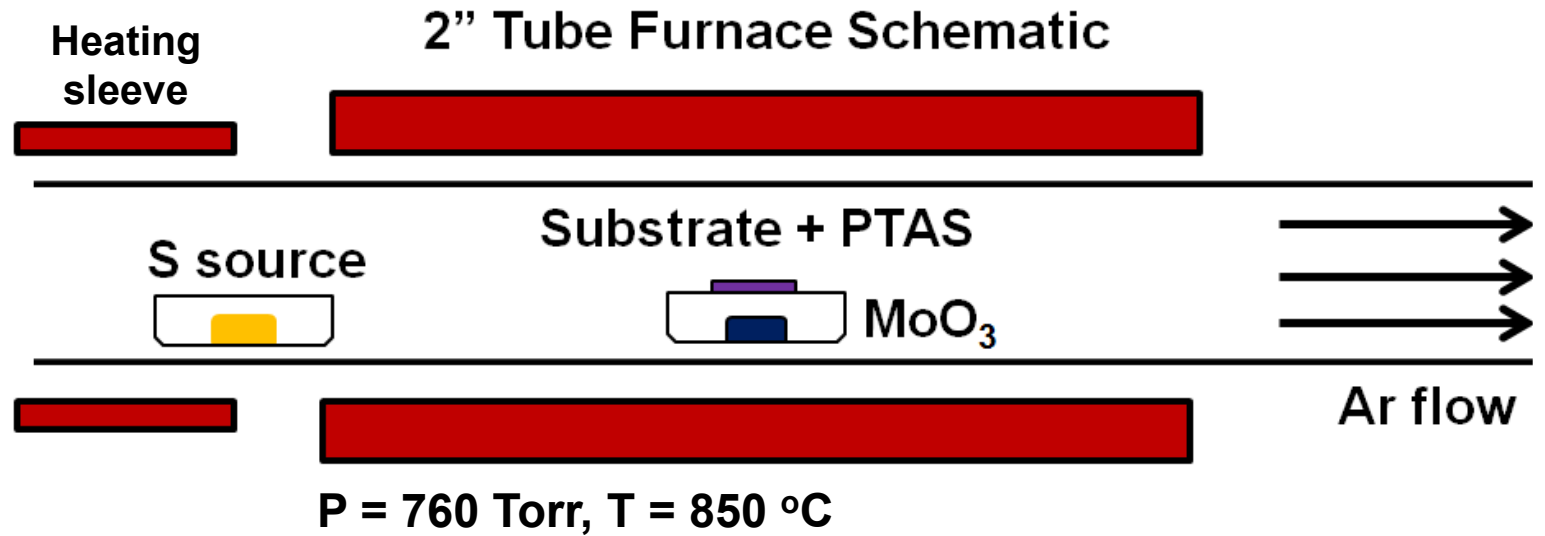


CVD Growth of Monolayer MoS₂

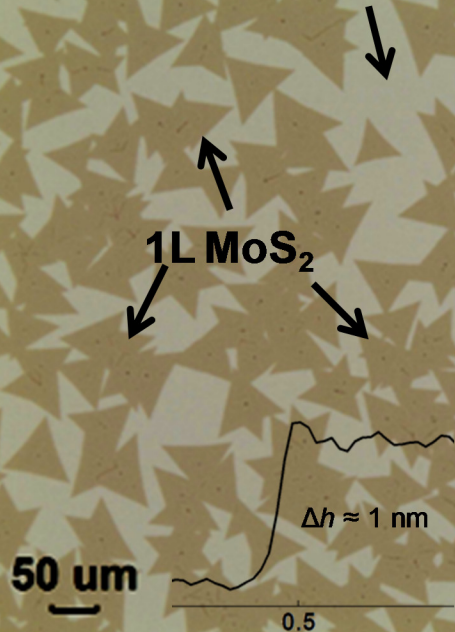
Kirby Smithe (Pop Lab)



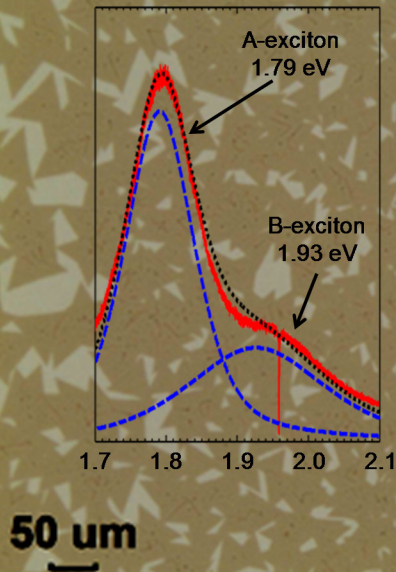
PTAS: perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt



(a) SiO₂/Si substrate



(b)



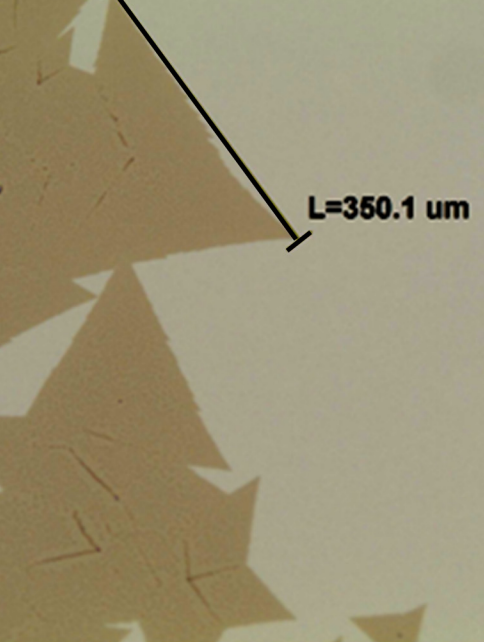
(c)

Continuous 1L MoS₂

Speck of dirt

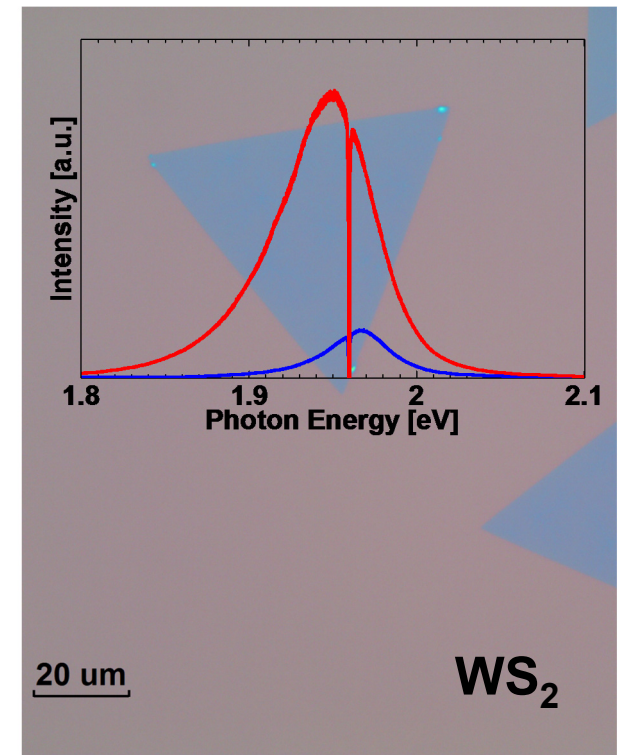
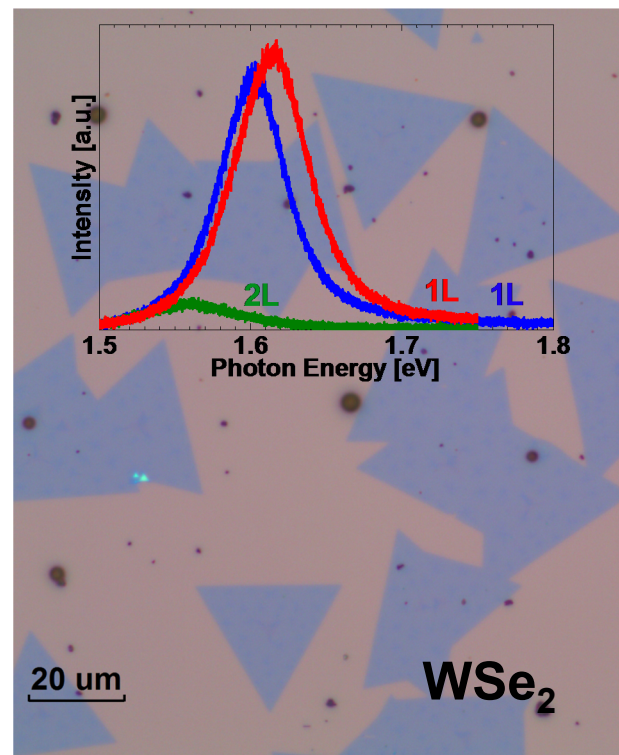
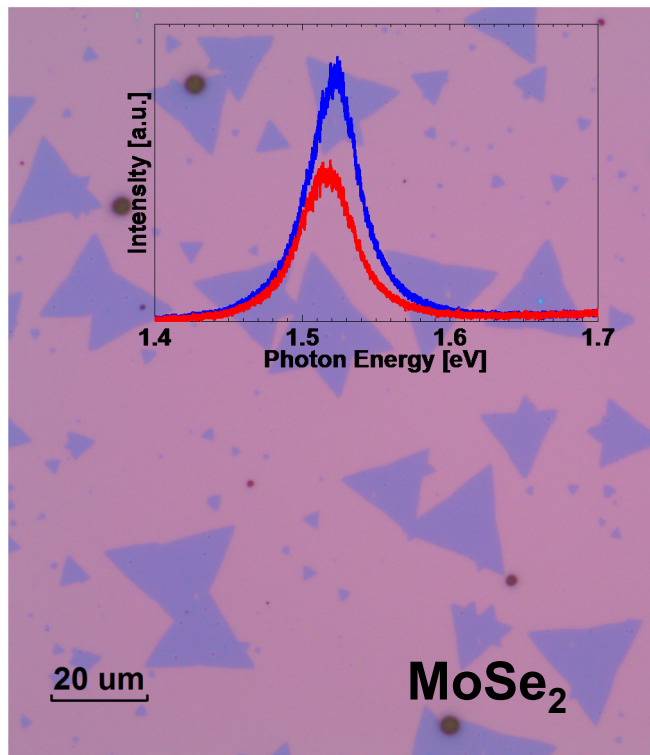
50 μm

(d)



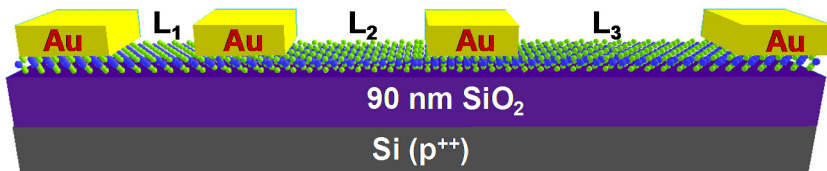
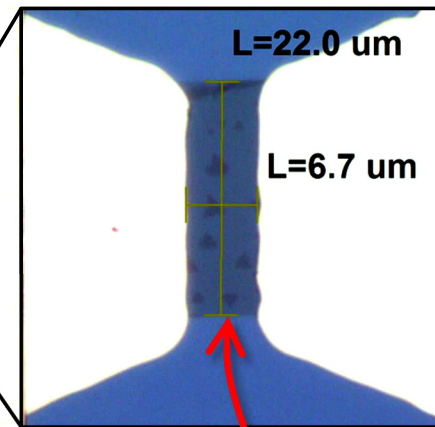
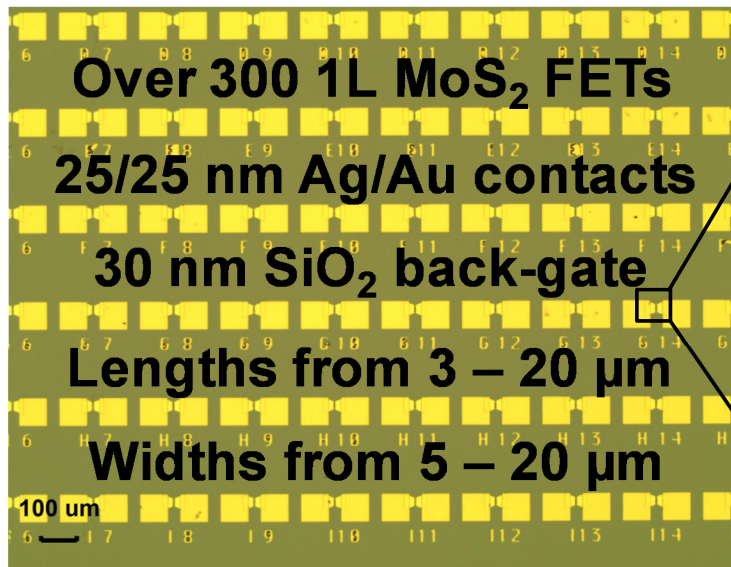
Other Monolayer Semiconductors

Kirby Smithe (Pop Lab)

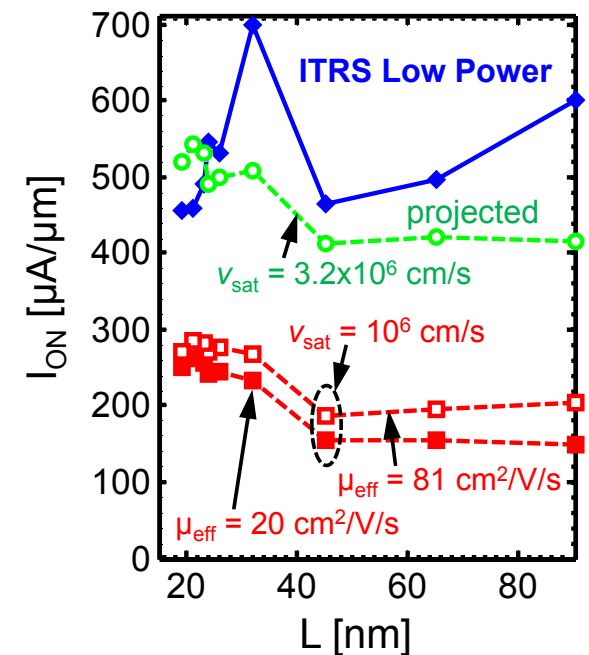
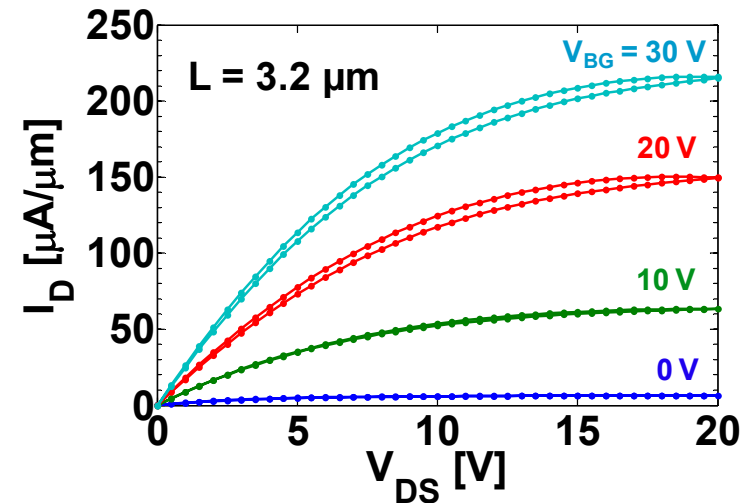


- Goal → Large-area **monolayers**, direct band gaps 1.5-2.0 eV
- Wish to scale up devices for low-power **digital** electronics
- Most experience with MoS₂, other TMDs just becoming available

MoS₂ Transistors with Good I_{DSat}



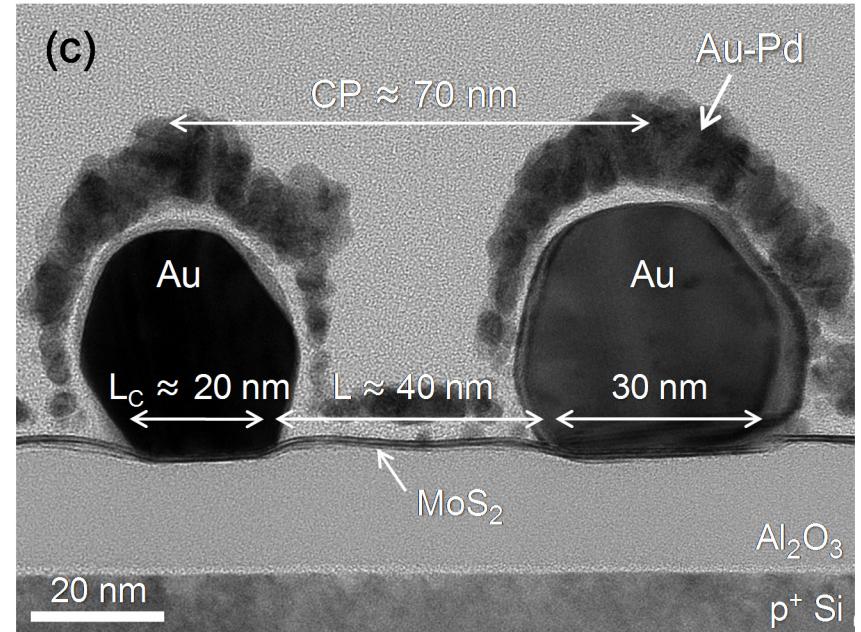
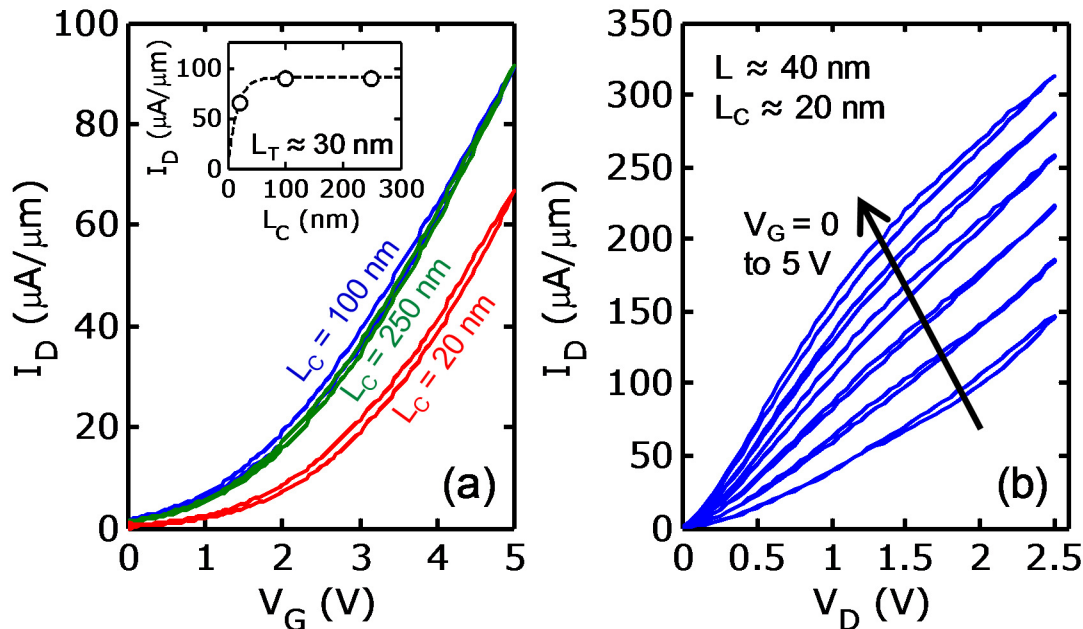
- Large area monolayer MoS₂ devices
- Some variability due to “patches” of 2L
- TLM: $\mu \sim 35 \text{ cm}^2/\text{V}/\text{s}$ and $R_C \sim 1.7 \text{ k}\Omega\text{-}\mu\text{m}$
- I_{DSat} close to ITRS “low power” needs



Highly Scaled MoS₂ Transistors

C. English, G. Shine, V. Dorgan, K. Saraswat, E. Pop, *Nano Lett.* 16, 3824 (2016)

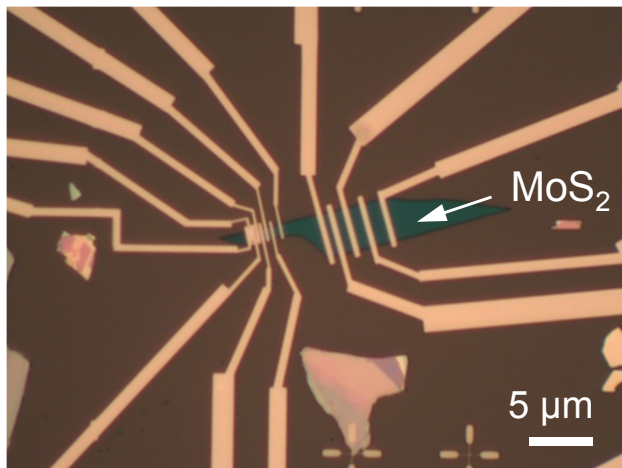
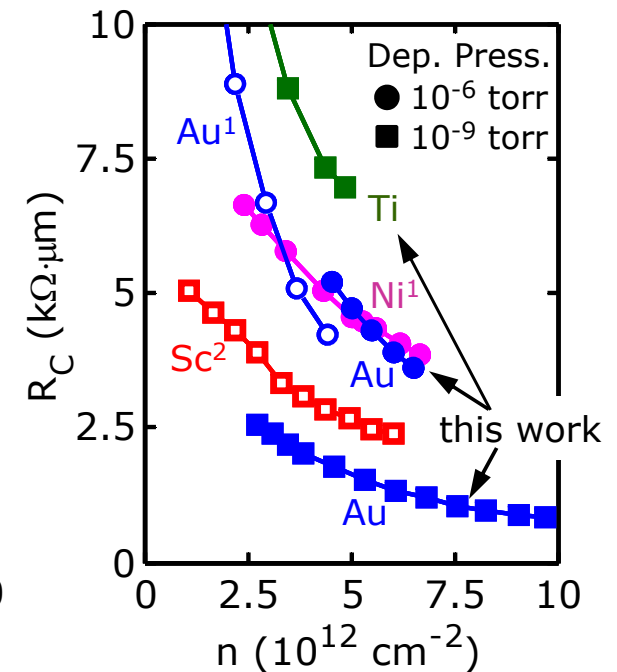
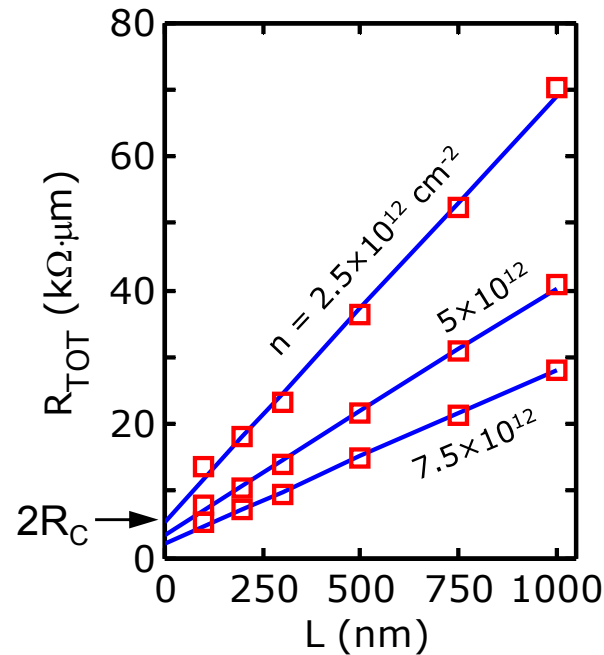
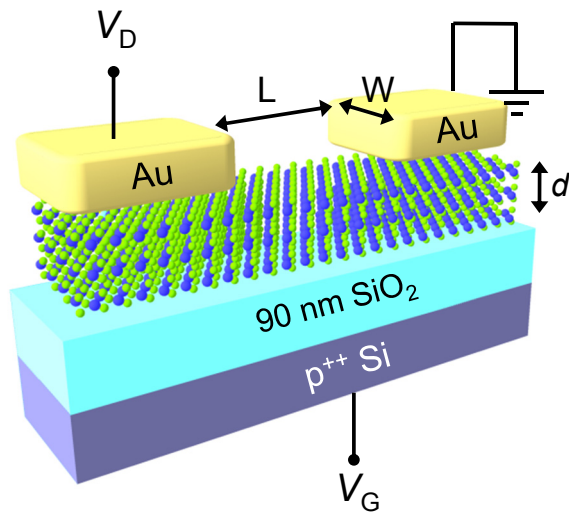
Goal: scale both channel length and contacts of MoS₂ FETs → what happens?



- **Smallest MoS₂ transistor with smallest contacts to date**
 - $L = 40$ nm and variable contacts ($L_C = 20$ to 100 nm)
 - Smallest contact pitch $CP \sim 70$ nm, equivalent to “14 nm” technology node
- **Contacts are limiting** the performance of small MoS₂ transistors

Metal Contacts to MoS₂ (Clean but Undoped)

C. English, G. Shine, V. Dorgan, K. Saraswat, E. Pop, *Nano Lett.* 16, 3824 (2016)



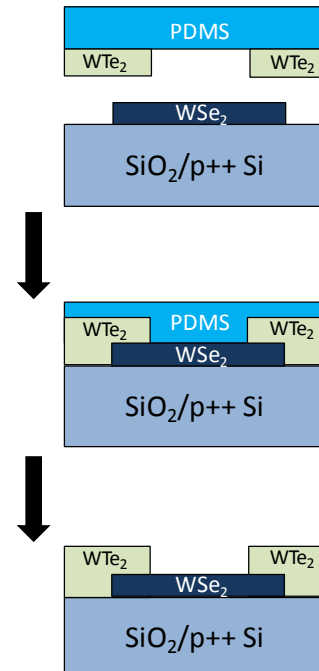
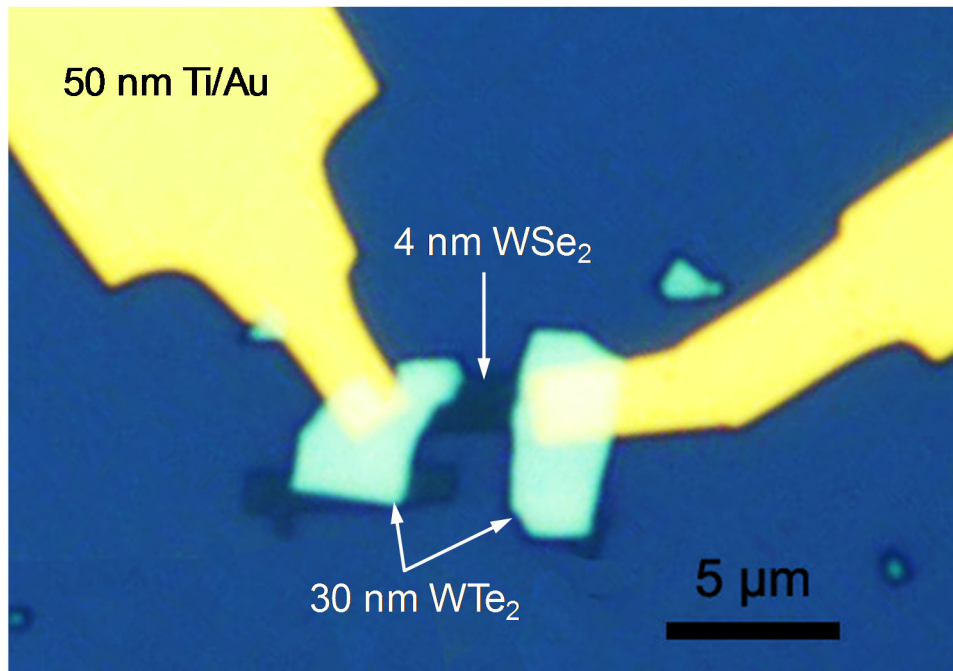
Transfer Length Method (TLM)

- Contacting 2D materials is **difficult**
- Cleaner Au deposition ($\sim 10^{-9}$ torr) leads to improved contact resistance
 - $R_C \sim 740 \Omega \cdot \mu\text{m}$ and $\rho_C \approx 4 \times 10^{-7} \Omega \cdot \text{cm}^2$

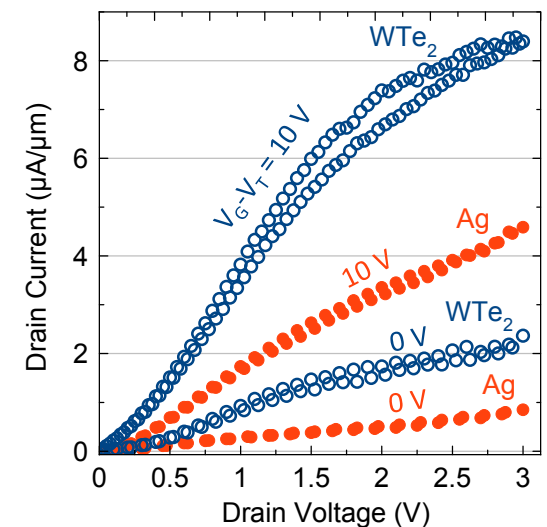
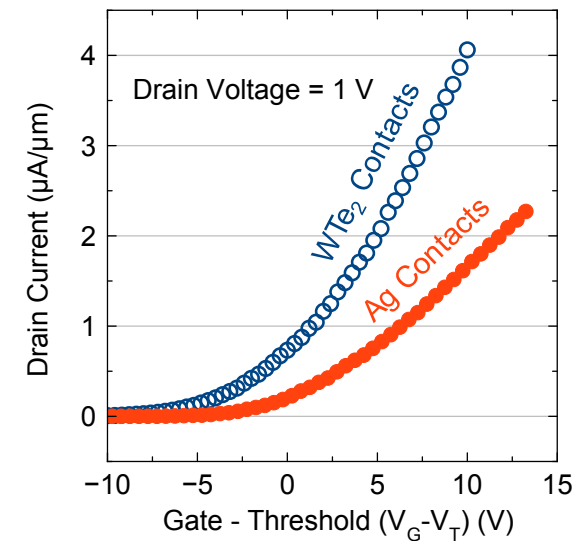
¹H.Liu & P. Ye (2013), ²S. Das & J. Appenzeller (2013)

2D Contacts to 2D Transistors?

C. McClellan, M. Mleczko, Y. Nishi, E. Pop, *Device Research Conf.* (2016)

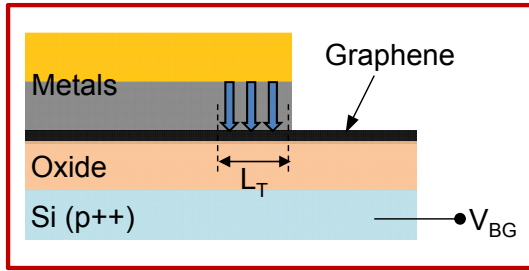


- WTe₂ (2D metal) contacts to WSe₂ (semic.)
- Residue-free transfer process
- 2x improvement over Ag contacts (“best known”)
- Observed current saturation

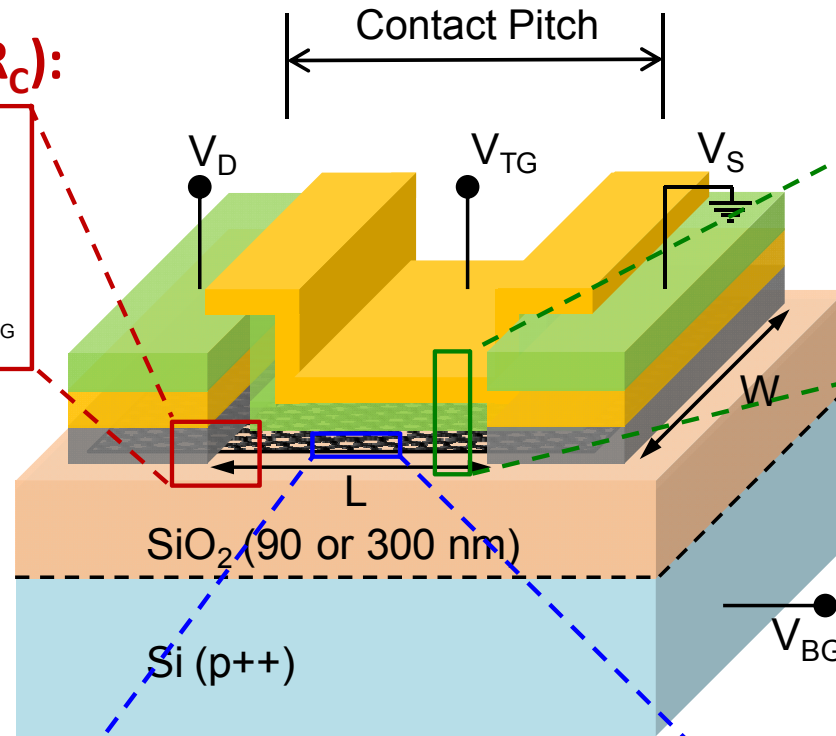


Summary of Challenges in 2D Devices

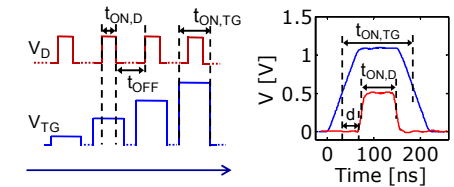
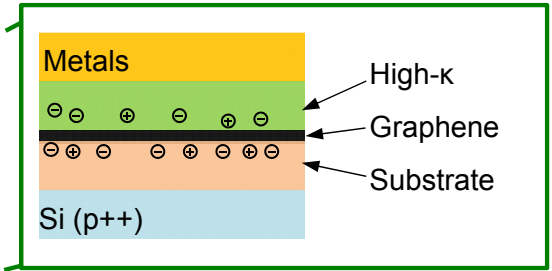
Contact Resistance (R_C):



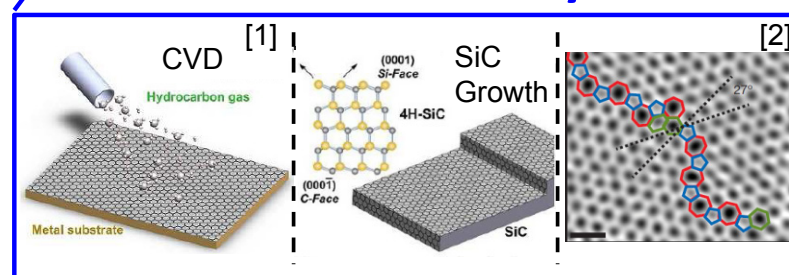
Must scale pitch =
channel & contacts



Interfaces:



Material Quality:



+Variability!

E. Carrion, E. Pop et al, *IEEE TED*, 61, 1583 (2014)

Outline of Talk

- The SystemX Alliance at Stanford

- 2D Materials

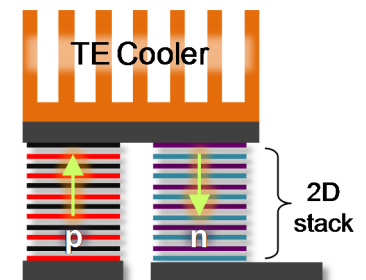
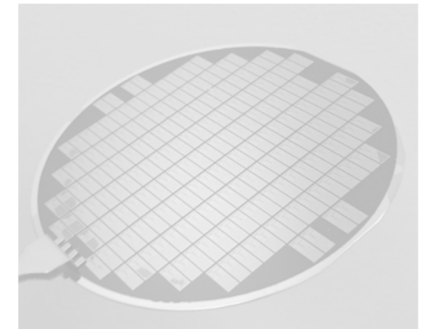
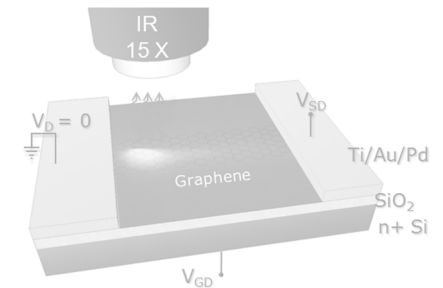
- Structure and energy bands

- Devices to Systems

- Transport properties and integration

- Thermal Energy at Nanoscale

- Fundamental limits & looking ahead

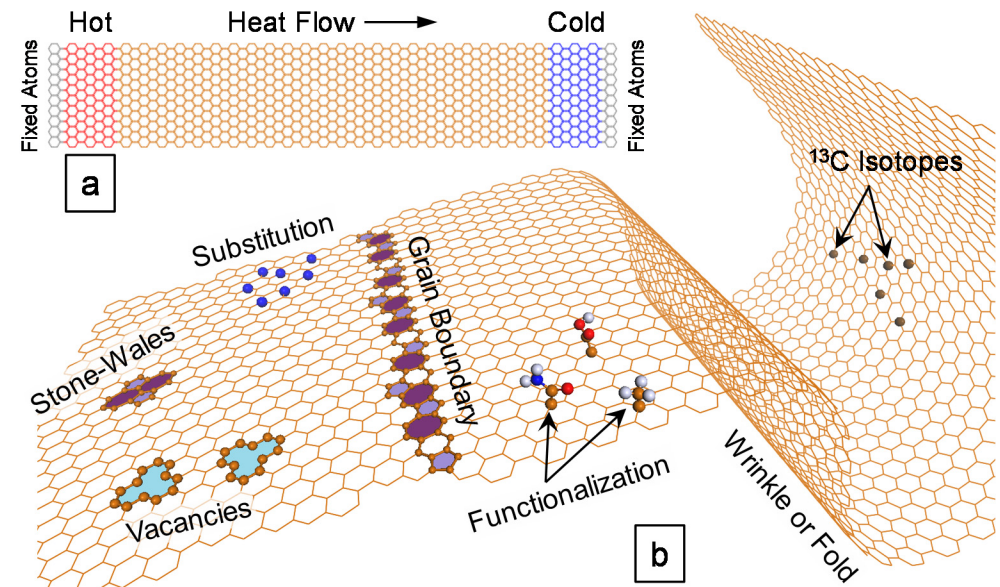


2D Material Thermal Properties

- **Large in-plane** thermal conductivity of graphene, BN (>500 W/m/K)
- **Ultra-low cross-plane** thermal conductivity of layered WSe₂ (<0.1 W/m/K)
 - Lower than plastics and **comparable to air**
- Huge thermal anisotropy in all layered 2D materials (>10-100x)

- MRS Bulletin review with AFRL:

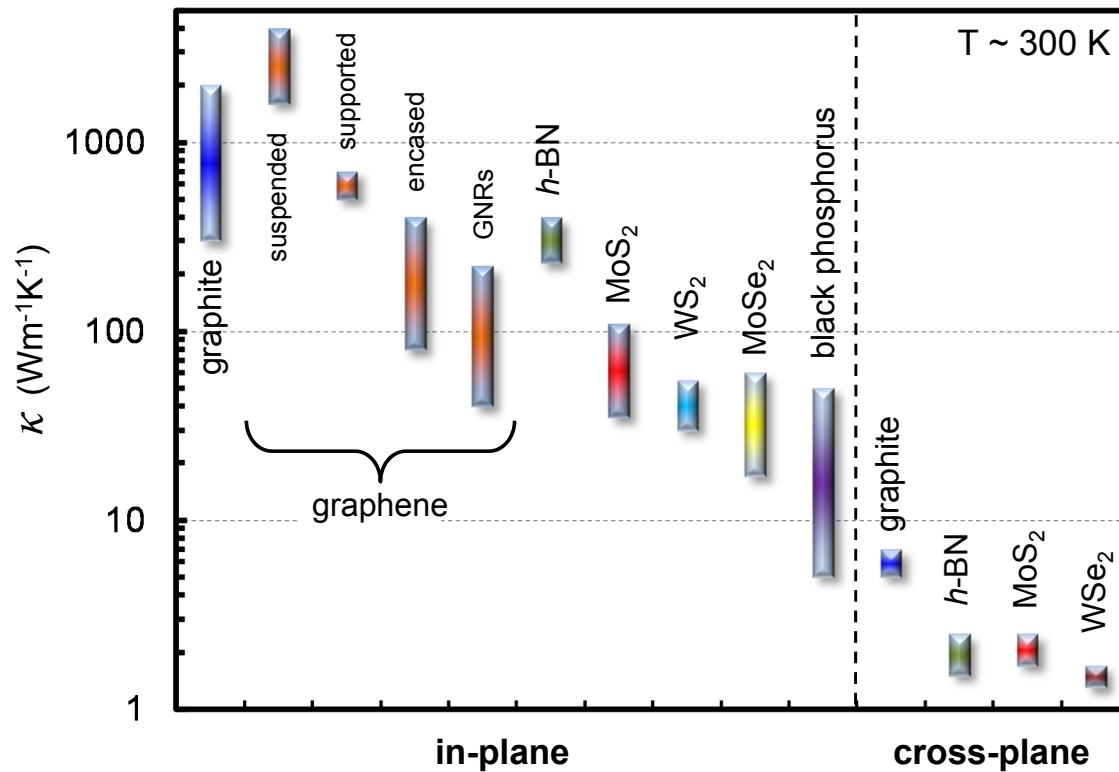
E. Pop, V. Varshney, A.K. Roy, "Thermal Properties of Graphene: Fundamentals and Applications," *MRS Bulletin* **37**, 1273 (2012)



- **Large thermopower** in TMDs ($S \sim 0.5$ mV/K) → Thermoelectrics?

$$ZT = \frac{S^2 \sigma T}{k}$$

Thermal Conductivity (κ) of 2D Materials



$$Q'' = -\kappa \nabla T$$

heat flux

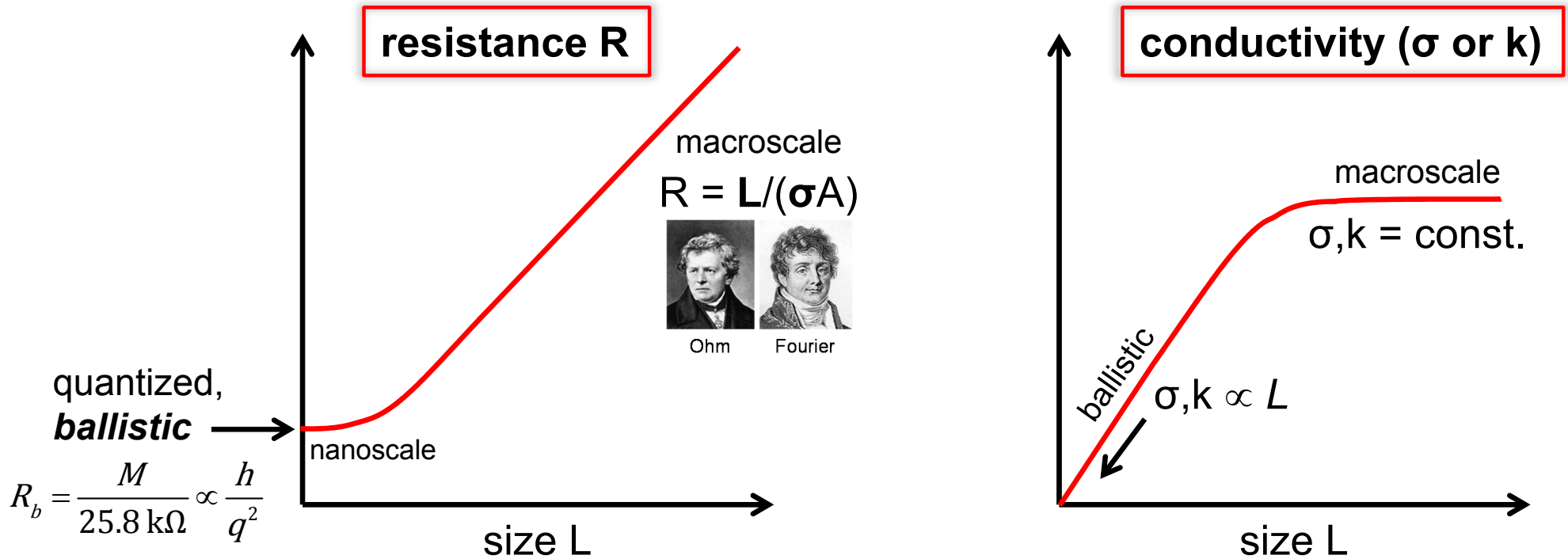
thermal conductivity

T gradient

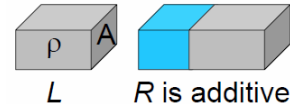
- Flexural phonon modes play important role in 2D materials
- **Anisotropy:** κ_{\parallel} from $\sim 6 \text{ Wm}^{-1}\text{K}^{-1}$ (WTe_2) to $\sim 2000 \text{ Wm}^{-1}\text{K}^{-1}$ (graphene)
 - Cross-plane κ_{\perp} is typically very small, e.g. 1 to 6 $\text{Wm}^{-1}\text{K}^{-1}$

E. Pop, V. Varshney, A. Roy, *MRS Bull.* 37, 1273 (2012); Table courtesy of Z. Li (Pop Lab)

Heat (and Current) Flow in Nanoscale Samples



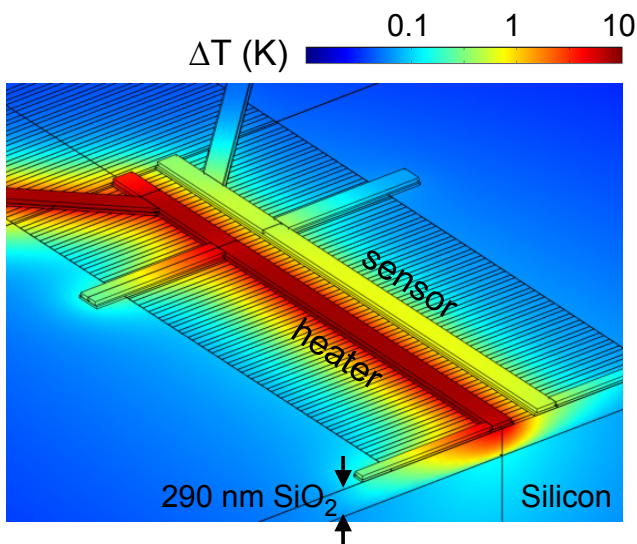
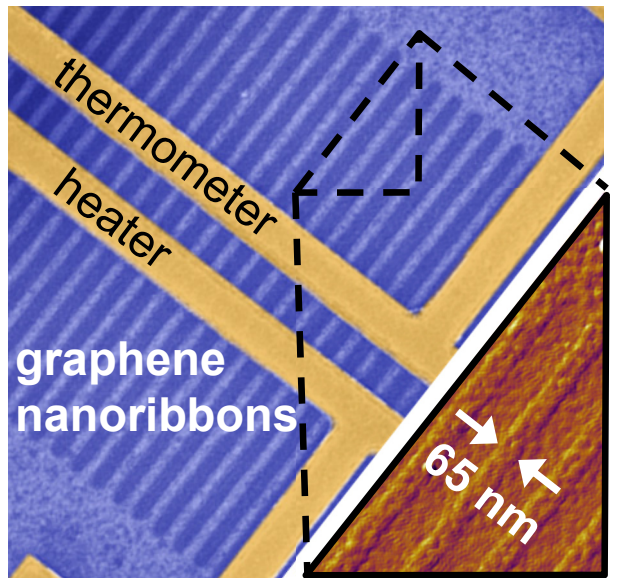
- Macroscale, R is additive: $1 + 1 = 2$
- **Nanoscale**, R is quantized: $1 + 1 = 1$



- Occurs when system size is comparable to electron or phonon (heat) wavelengths and mean free path (10-100 nm)
- Both electrical and thermal resistance can be **quasi-ballistic**

Heat Flow in Nanoscale Graphene

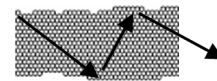
M.-H. Bae, Z. Li, Z. Aksamija, P. Martin, F. Xiong, Z.-Y. Ong, I. Knezevic, E. Pop, *Nature Comm.* 4, 1734 (2013)



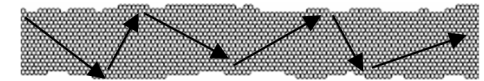
Bulk thermal properties do not apply at $<1 \mu\text{m}$!

Thermal conductivity $k(T) = f(W, L)$ even at room T

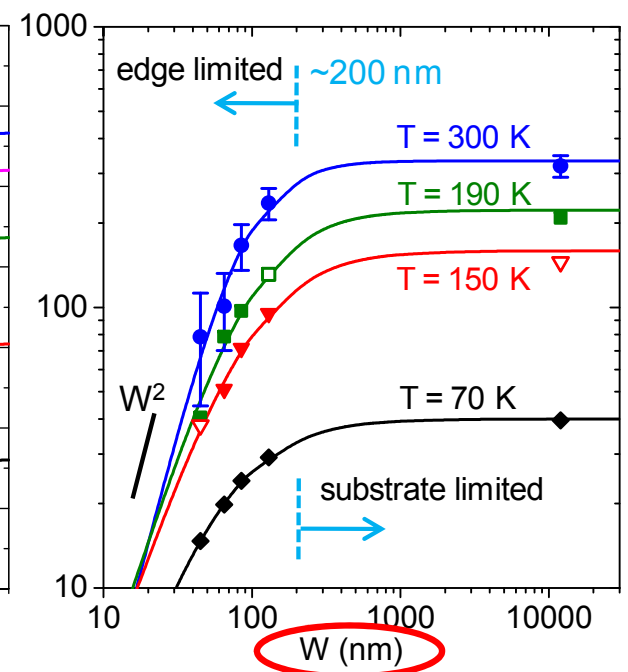
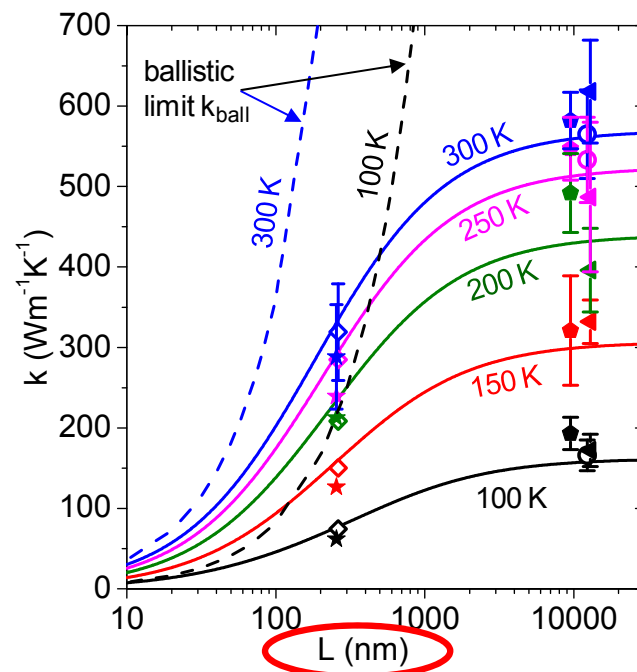
- 35% (quasi-)ballistic heat flow in short devices ($\lambda \sim 100 \text{ nm}$)
- Strong edge scattering in narrow devices



“short” (quasi-ballistic)



“long” (diffusive + edges)

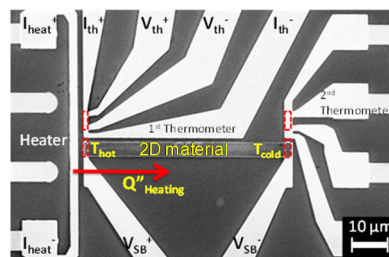
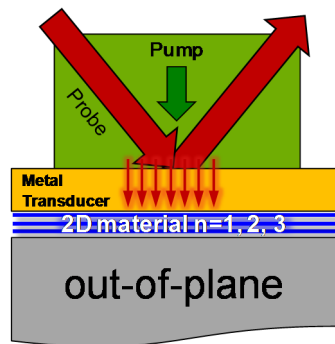


Looking Ahead: Future Opportunities

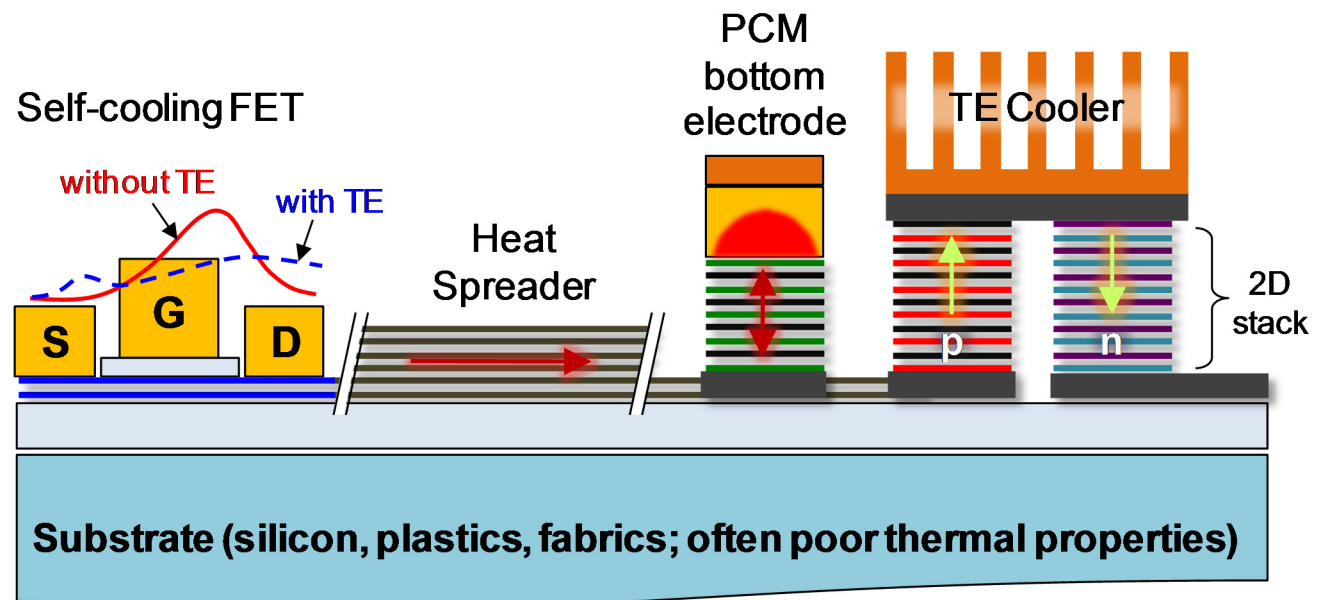
collab: E. Reed, K. Goodson, K. Saraswat, H.-S.P. Wong, Y. Cui

Could we:

- Exploit **anisotropy** for routing heat? (thermal diode)
- Separate thermal and electrical flow? (thermal transistor)
- Design electronics with **built-in thermoelectric cooling**?
- Achieve transparent heat spreaders and flexible thermoelectrics?



in-plane

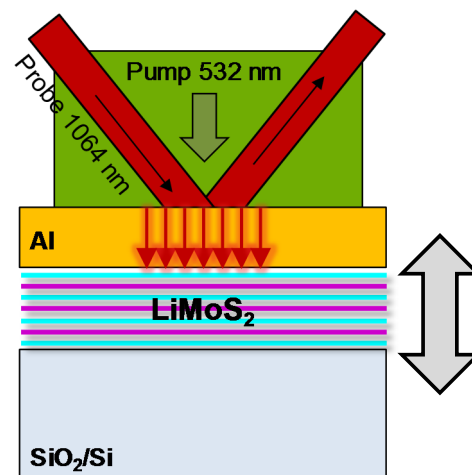
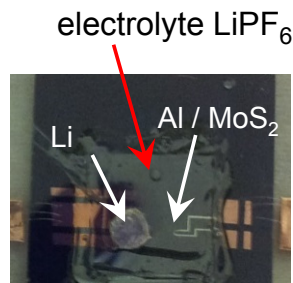
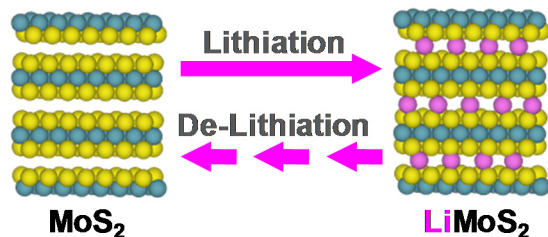


Looking Ahead: Future Opportunities

collab: E. Reed, K. Goodson, K. Saraswat, H.-S.P. Wong, Y. Cui

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- Design electronics with **built-in thermoelectric cooling**?
- Achieve transparent heat spreaders and flexible thermoelectrics?



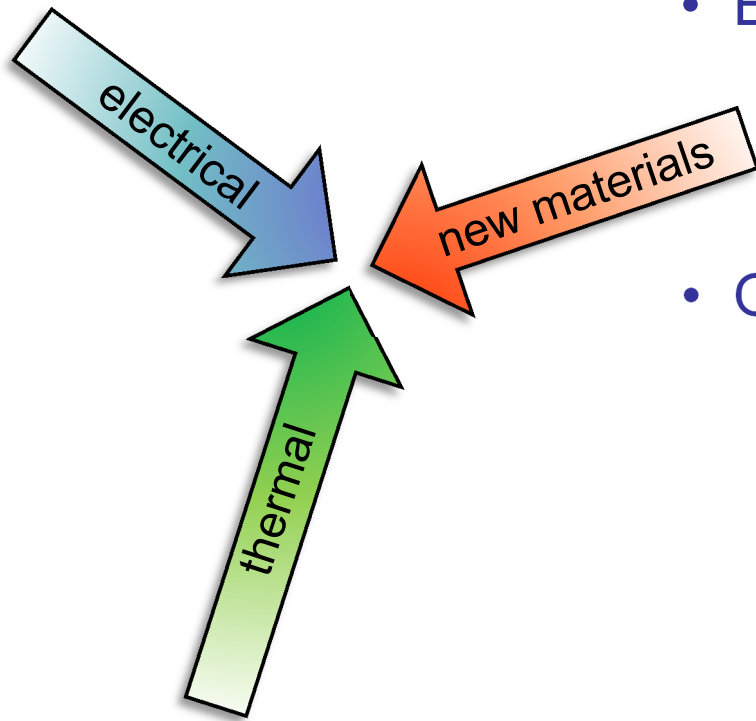
Thermal Switching



A. Sood, F. Xiong, [...], E. Pop, *Spring MRS* (2015)

Summary

- Moore's Law $\sim 10x$ → slowing down
- Energy scaling & harvesting $\sim 10^4x$ → exciting



- Opportunity for convergence of:
 - Novel 2D nanomaterials
 - Anisotropic electrical & thermal properties
 - Heterogeneous integration
- Understand fundamental limits
- Future opportunities

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