Power Dissipation in Nanoscale CMOS and Carbon Nanotubes

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Power and Heat: The Big Picture

Sun surface? 6000 W/cm²

http://phys.ncku.edu.tw/~htsu/humor/fry_egg.html
Thermal Management Challenges

350-V bulk power subassembly (under cover)

- IBM S/390 refrigeration
- Grid computing:

Power and Heat: The Tiny Picture

Carbon nanotubes burn at high enough applied voltage (they also emit light when they get this hot)
Power, Thermal Management Methods

Is there a bottom-up approach?
From the device and materials level?

Chip-Level Thermal Network

Top view
Hottest spots > 300 W/cm²

Cross-section
8 metal levels + ILD

Transistor < 100 nm
**Thermal and Electrical Resistance**

\[ P = I^2 \times R \]
\[ \Delta V = I \times R \]
\[ \Delta T = P \times R_{TH} \]
\[ R = f(\Delta T) \]

Fourier’s Law (1822)  
Ohm’s Law (1827)

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**Device-Level Thermal Challenges**

- **Small geometry**
  - High power density (device-level hot spot)
  - Higher surface-to-volume ratio, i.e., higher role of thermal interfaces between materials
- **Lower thermal conductivity**
- **Lowering power** (but can it ever be low enough?!)
- **Device-level thermal design** (phonon engineering)

<table>
<thead>
<tr>
<th>Material</th>
<th>( k ) (W/m/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>148</td>
</tr>
<tr>
<td>Ge</td>
<td>60</td>
</tr>
<tr>
<td>Silicides</td>
<td>40</td>
</tr>
<tr>
<td>Si (10 nm)</td>
<td>13</td>
</tr>
<tr>
<td>SiO(_2)</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Thermal Resistance of a Single Device

High thermal resistances:
- SWNT due to small thermal conductance (very small \( d \sim 2 \) nm)
- Others due to low thermal conductivity, decreasing dimensions, increased role of interfaces

Power input also matters:
- SWNT \( \sim 0.01-0.1 \) mW
- Others \( \sim 0.1-1 \) mW


Modeling Device Thermal Resistance

- Steady-state models
  - Finite-Element models

\[
R_{TH} = \frac{1}{2k_v D} \approx \frac{1}{4k_v \sqrt{LW}}
\]

\[
R_{TH} \approx \frac{t_{BOX}}{2W} \left( \frac{t_{BOX}}{k_{BOX}k_v t_S} \right)^{1/2}
\]
A More Detailed Look

1. Monte Carlo heat generation in bulk and strained silicon

2. Self-heating in thin-body SOI and GOI devices

3. Self-heating and lessons from carbon nanotubes

Quick Recap of Phonons

- Phonons = lattice vibration waves
- Phonons are responsible for heat transport in semiconductors
- "Hot phonons" = highly occupied modes above room temperature
**Details Picture of Joule Heating**

- **High Electric Field**
- **Hot Electrons (Energy E)**
  - $E < 50 \text{ meV}$
  - $\tau \sim 0.1 \text{ps}$
  - $V_{ac} \sim 9000 \text{ m/s}$
- **Optical Phonons**
  - $E > 50 \text{ meV}$
  - $\tau \sim 0.1 \text{ps}$
  - $V_{op} \sim 1000 \text{ m/s}$
- **Acoustic Phonons**
  - $\tau \sim 5 \text{ ps}$
  - $V_{ac} \sim 9000 \text{ m/s}$
- **Heat Conduction to Package**

Note: optical phonon energy in CNTs (180 meV) about 3x higher than in Si (60 meV)

**2D Thin-Body SOI Simulation**

- Study of device matching
  - $L_G = 18 \text{ nm ITRS specs}$
  - if $W/L = 4$ then $N_{elec} \sim 2500$ total!
- Monte Carlo (MONET)

Notice heat is dissipated in device drain
• **Monte Carlo** vs. **Medici** (drift-diffusion commercial code):
  – “Long” (500 nm) device: same current, potential, nearly identical
  – Importance of non-local transport in short devices
  – **Heat dissipation in DRAIN** (optical, acoustic) of shortest devices

**Phonon Generation Spectrum in Silicon**

• Complete spectral information on phonon generation rates
• Note: effect of scattering selection rules (less f-scatt in strained Si)
• Note: same heat generation at high-field in Si and strained Si
What About Device Design?

Monte Carlo Analysis

Thermal Conductivity

Design and Scaling

What About Device Design?

Thin Film Thermal Conductivity


- Phonon boundary scattering and confinement
- Strong decrease in thin film or nanowire thermal conductivity \( (k) \), up to 10-100x lower than bulk
- How does this affect nanometer scale devices?
Boundary Thermal Resistance

- Thermal interface resistance at solid-solid material interfaces
- Caused by phonon dispersion mismatch b/w materials (~Cv/4), electron-phonon energy conversion at boundary, roughness at boundary
- Approximately equivalent to ~10-100 nm additional SiO$_2$

Self-Consistent Electro-Thermal Model

- $R_{td} = R_{ex} \pm R_Q + R_{sd} + R_{co}$
  - ($R_Q$ due to heat source position)
- $C_c = 2\beta e_e \ln (1 + L_{ex} / t_{ex}) / \pi$
- $T = PR$
- $P = VI$
- $I = \mu \times (V_{dd} - V_e)^n$
- $T^{-1} = 0.7 \text{ mV/K}$
**SOI/GOI Device Design Optimization**

E. Pop et al., Proc. IEDM 2004

- Larger Source/Drain (S/D) volume will help heat spreading in drain
- BUT… no improvement for S/D thickness $t_{SD} > 3-4 \times t_{film}$
- Effect of parasitic side-wall capacitance on Intrinsic Delay
- Optimized, “well-behaved” GOI devices 30% faster than optimized SOI

**Transient Device Thermal Modeling**


- Compact thermal device model including:
  - Non-equilibrium heat generation from Monte Carlo
  - Phonon relaxation parameter-matched to Boltzmann Transport Eq.
- Capture spatial and temporal temperature excursions
- What is the effect on leakage & reliability?
Onto Carbon Nanotubes...


Where Carbon Nanotubes Fit In

Allotropes of Carbon:
- Diamond
- Buckyball (C60)
- Amorphous (soot)
- Single-Walled Nanotube
- Graphite (pencil lead)
Carbon Nanotubes for Electronics

- Carbon nanotube = rolled up graphene sheet
- Great electrical properties
  - Semiconducting $\rightarrow$ Transistors
  - Metallic $\rightarrow$ Interconnects
  - Electrical Conductivity $\sigma \approx 100 \times \sigma_{Cu}$
  - Thermal Conductivity $k \approx k_{diamond} \approx 5 \times k_{Cu}$
- Nanotube challenges:
  - Reproducible growth
  - Control of electrical and thermal properties
  - Going “from one to a billion”

Nanotube Back-of-the-Envelope Estimates

- Typical $L \sim 2 \mu m$, $d \sim 2 \text{ nm}$
- On insulating solid substrate
- Heat dissipated into substrate
  - Moderate power $\sim 10 \mu W/\mu m$
  - Peak $\Delta T \sim 60$ K
- Thermal conductivity $k \sim 3000$ W/m/K
- Freely suspended nanotube
- Heat dissipated along tube length
  - Moderate power $\sim 10 \mu W$ (10 $\mu A$ @ 1 V)
  - Peak $\Delta T \sim 400$ K
Transport in Suspended Nanotubes


- Observation: significant current degradation and negative differential conductance at high bias in suspended tubes
- Question: Why? Answer: Tube gets HOT (how?)

Transport Model Including Hot Phonons


\[ R(V, T) = R_c + \frac{h}{4q^2} \left[ L + \lambda_{OP}(V, T) \right] \]

Include OP absorption:

\[ \lambda_{OP} = \left( \frac{1}{\lambda_{OP,ac}} + \frac{1}{\lambda_{OP,ac}} - \frac{1}{\lambda_{OP,ac}} \right) \]
Extracting SWNT Thermal Conductivity

- “Inverse” numerical extraction of $k$ from the high bias ($V > 0.3$ V) tail
- Comparison to data from 100-300 K of UT Austin group (C. Yu, NL Sep’05)
- Result: first “complete” picture of SWNT thermal conductivity from 100 – 800 K

Light Emission from Metallic SWNTs

- Joule-heated tubes emit light:
  - Comes from center, highly polarized
  - Quasi-metallic = small band gaps
  - Emitted photons at higher energy than applied bias (high energy tail)
Return to SWNTs On Substrates


- SWNT on insulating solid substrate
- Heat dissipated into substrate rather than along tube length
- Q: How do I model heat loss into substrate?
- [A: need some gauge of the tube temperature]

Nanotube Temperature Gauge
Nanotube Temperature Gauge

- Doesn’t exist
- But… oxidation (burning) temperature is known

\[ T_{BD} \sim 600 \, ^\circ C \]

Breakdown of SWNTs in Air (Oxygen)

\[ AV(kVT) + p' - g(T - T_0) = 0 \]

At breakdown: \[ p' = I_{BD}V_{BD} / L \]

\[ V_{BD} = gL(T_{BD} - T_0) / I_{BD} \]

- Data shows SWNTs exposed to air break down by oxidation at 500 < \( T_{BD} < 700 \, ^\circ C \) (800–1000 K)
- Joule breakdown voltage data shows \( V_{BD} \) scales with \( L \) in air
- Supports cooling mechanism along the length, into the substrate
Electrical Breakdown of SWNTs

- SWNT exposed to air from the top
- Sweep voltage low to high
- Temperature peaks in the middle
- When $T_{max} = T_{BD}$ → $V = V_{BD}$ and $P_{BD} = I_{BD}V_{BD}$

Breakdown Data from Literature

E. Pop, DRC (2007)

- “Short” vs. “long” breakdown: Compared to thermal “healing” length ~ 0.2 µm
- Note: There is a minimum breakdown power ~ 0.05 mW
- We can learn a lot more about electrical and thermal properties

\( P_{BD} = gL(T_{BD} - T_0) \frac{\cosh(L/2L_{th}) + gL_{th}R_s \sinh(L/2L_{th})}{\cosh(L/2L_{th}) + gL_{th}R_s \sinh(L/2L_{th}) - 1} \)

![Graph showing breakdown data from literature](image)

SWNT Compact Model Up to Breakdown


- Thermal “healing length” along SWNT ~ 0.2 µm
- Current saturation ~ 20 µA in long tubes (> 1 µm) due to self-heating
- Self-heating not significant when \( P' \) < 5 µW/µm (design goal?)
- More current in short nanotubes = less heating?

![Graph showing SWNT compact model up to breakdown](image)
Summary

- Small device dimensions, high local power densities
- Increased device thermal resistance with decreasing dimensions
- Physics-based models to capture:
  - Size effects
  - Phonon non-equilibrium
  - Transient temperature effects
- Opportunity for “bottom-up” thermal device and materials design

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