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CMOS-compatible strain engineering for monolayer semiconductor transistors

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Strain engineering has played a key role in modern silicon electronics, having been introduced as a mobility booster in the 1990s and commercialized in the early 2000s. Achieving similar advances with two-dimensional (2D) semiconductors in a complementary metal–oxide–semiconductor (CMOS)-compatible manner could improve the industrial viability of 2D material transistors. Here, we show that silicon nitride capping layers can impart strain to monolayer molybdenum disulfide (MoS_2) transistors on conventional silicon substrates, improving their performance with a CMOS-compatible approach, at a low thermal budget of 350 °C. Strained back-gated and dual-gated MoS_2 transistors exhibit median increases in on-state current of up to 60% and 45%, respectively. The greatest improvements are found when reducing both transistor channels and contacts from micrometre-scale to 200 nm, reaching saturation currents of 488 μA μm^{-1} in devices with just 400 nm contact pitch. Simulations show that the performance enhancement is mainly due to tensile strain lowering the contact Schottky barriers, and that further reducing device dimensions, including contacts, could lead to additional increases in strain and performance.

Commercial silicon complementary metal–oxide–semiconductor (CMOS) technology has benefitted from strain-boosting of transistor performance for two decades, ever since development of the 90 nm technology node[1–5]. Silicon nitride (SiN_x) capping layers have been used for n-type silicon transistors to achieve uniaxial tensile strain and increase electron mobility[6,7]. On the other hand, the selective growth of SiGe in the p-type silicon transistor source and drain has been used to create uniaxial compressive strain and enhance hole mobility[8]. These improvements are due to changes in the band structure, which lead to a reduction of electron and hole effective masses and scattering rates.

Two-dimensional (2D) semiconductors, such as transition-metal dichalcogenides (TMDs), have gained attention due to their atomically thin nature as transistor channels[9] for high-density and low-power electronics. Various advances in the growth[10,11], doping[12,13] and contact engineering[14–16] of TMDs, such as molybdenum disulfide (MoS_2), have been reported for transistor applications. As with silicon, strain engineering has been predicted to modulate the TMD band structure and mobility[17–19]. However, these effects have mainly been probed optically[20,21] and by electrical measurements of large, micrometre-scale devices on bent flexible substrates[22,23] or rigid substrates[24,25]. To integrate TMD-based transistors with future semiconductor technologies, the transistor strain must be applied in a scalable, CMOS-compatible fashion on planar, rigid, silicon substrates, and ideally used to boost the performance of nanoscale devices.

In this Article, we show that controllable strain can improve the performance of back-gated (BG) and dual-gated (DG) monolayer MoS_2 transistors down to nanoscale dimensions. This is achieved using SiN_x capping layers with tunable intrinsic stress, which are deposited by plasma-enhanced chemical vapour deposition (CVD) at 350 °C. The relatively low deposition temperature makes this an attractive CMOS- and

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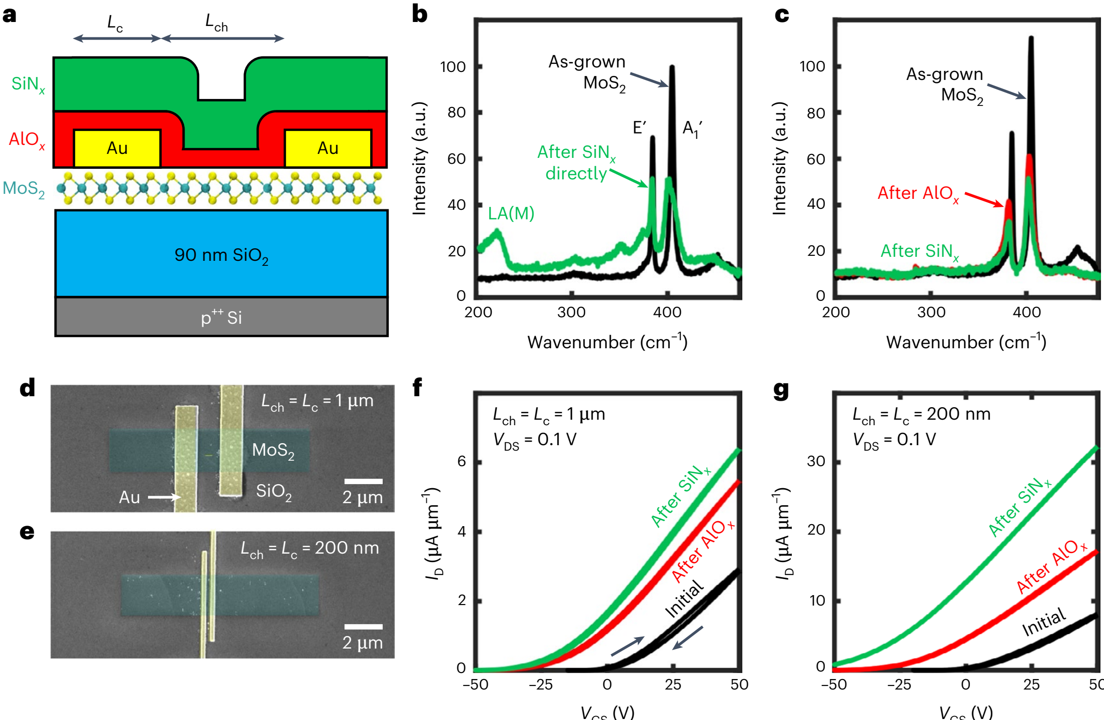

Fig. 1 | BG transistors with strain. a, Schematic of a BG monolayer MoS_2 transistor capped with AlO_x and tensile-stressed SiN_x. The contact pitch is the sum of the channel length and contact length, CP = $L_{ch} + L_c$. **b**,**c**, Raman spectra of monolayer MoS_2 before and after direct deposition of SiN_x, without the AlO_x barrier layer (**b**) and with the AlO_x barrier layer (**c**). **d**,**e**, Top-down, false-colour, scanning electron microscope images of a long device with $L_{ch} = L_c = 1$ µm (**d**) and a short device with $L_{ch} = L_c = 200$ nm (**e**). **f**,**g**, BG transfer characteristics of a high-stress SiN_x-capped MoS_2 transistor with long dimensions (**f**) and short dimensions (**g**). Small arrows mark forward and backward voltage sweeps, revealing minimal hysteresis. a.u., arbitrary units.

back-end-of-line compatible approach, as SiN_x is widely used in modern semiconductor technology[26]. The stress in these films can be varied from compressive to tensile by changing deposition parameters such as the precursor ratio, He gas dilution and pressure[27]. This approach also offers process tunability using a single capping layer, rather than needing separate materials to select between compressive and tensile stress. (Further details of SiN_x deposition and stress tuning are provided in Supplementary Section 1.)

Silicon nitride deposition on BG devices

To understand the effects of the strain due to SiN_x capping on a simplified device geometry, we first examined a conventional BG structure (Fig. 1a). Monolayer MoS_2 was grown by CVD on 90 nm SiO_2 on p^{++} Si substrates[28], which also served as back gates. The contact metal was 50 nm of Au deposited by electron-beam (e-beam) evaporation[16] at a pressure of ~10^{-8} Torr. Further details of device fabrication are given in Methods. Figure 1b shows that plasma-induced damage occurs when SiN_x films are directly deposited onto MoS_2, as indicated by the appearance of the defect-induced LA(M) peak[29] in the Raman spectra of MoS_2. To prevent such damage, we used a protective barrier layer of 1.5 nm e-beam evaporated Al followed by 10 nm AlO_x deposited by atomic layer deposition, which is a common encapsulation[12] for monolayer MoS_2. Figure 1c shows that when the SiN_x was deposited after the AlO_x, the Raman characteristics of the MoS_2 underneath do not display visible defect signatures.

Note that Raman analysis cannot be used to accurately estimate the strain in such encapsulated MoS_2, because doping and plasmon coupling from the AlO_x also affect the E' peak position[30]. Instead, we relied on grazing incidence X-ray diffraction measurements for blanket films (Supplementary Section 2), which indicated that compressive strain was created in the MoS_2 when a tensile SiN_x layer was deposited onto an unpatterned MoS_2 film, consistent with previous observations for large-area (micrometre-scale) capping with tensile MgF_2[20]. However, as we will show below, an important aspect of strain engineering is that the effect of stressor layers depends strongly on the dimensions of the device. The strain can change in both magnitude and sign along the transistor in the presence of metal contacts and gates, especially in nanoscale devices. This effect cannot be mapped by either Raman spectroscopy or X-ray diffraction due to their large spot sizes (~0.5 µm to millimetres) and their inability to probe the strain below metal layers. This challenge has been acknowledged in strained-Si technology, where strain distributions in nanoscale devices have been described with finite-element simulations, calibrated against transmission electron microscopy with dark-field electron holography[31,32]. To provide such insight, we used similar finite-element simulations to estimate the strain distributions in our nanoscale 2D devices.

As mentioned above, strain induced by capping layers in n-type Si transistors shows a strong dependence on the critical dimensions of the device, with shorter channels experiencing higher strain[33]. For this reason, we investigated the effect of MoS_2 transistor dimensions by varying the length of the channel (L_{ch}) and contacts (L_c), for 'long' and 'short' geometries with $L_{ch} = L_c$ of 1 µm and 200 nm, respectively, as shown in Fig. 1d,e. To understand the effect of capping layers, we performed electrical measurements on the same devices after each of the following steps: initial (no capping), after AlO_x deposition, and after SiN_x deposition. This allowed us to avoid the variability that could have occurred from using different MoS_2 growths.

Figure 1f,g shows the measured drain current versus back-gate voltage (I_D–V_{GS}) of long and short devices, respectively. In both cases, the AlO_x layer induced n-type doping, as previously reported[12,34], which negatively shifted the threshold voltage (V_T) and lowered the contact resistance. On the other hand, the effects of capping with SiN_x (75 nm thick, ~600 MPa tensile stress) were noticeably geometry-dependent. The long device had only a small negative V_T shift, whereas the short

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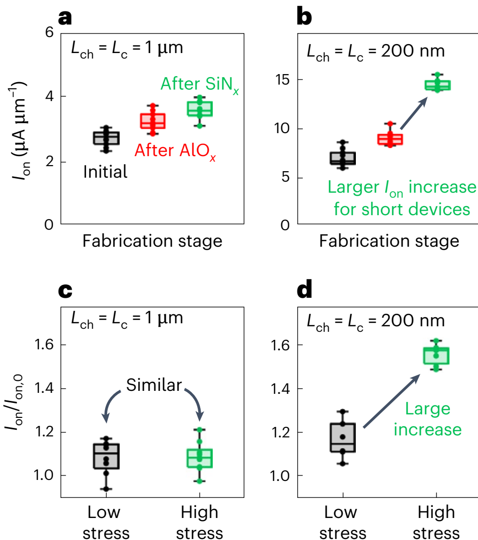

Fig. 2 | Geometry-dependent device statistics and low-stress control sample. **a**,**b**, Box plots of normalized on-state current (I_{on}) at $n \approx 8 \times 10^{12}$ cm^{-2} for several devices, after each fabrication step. **a**, $L_{ch} = L_c = 1$ µm (long) device. **b**, $L_{ch} = L_c = 200$ nm (short) device. Ten long devices were measured as-fabricated, but only eight were measured after SiN$_x$ capping due to imperfect yield. Similarly, nine short devices were measured as-fabricated and seven after SiN$_x$ capping. **c**,**d**, Relative improvement in I_{on} after capping with low-stress (50 to 100 MPa) and high-stress (600 MPa) SiN$_x$ films for long transistors (eight devices with low-stress capping and nine with high-stress capping) (**c**) and short transistors (six devices with low-stress capping and seven with high-stress capping) (**d**). The middle line in each box plot marks the median value. Upper and lower box ranges indicate upper and lower quartiles, while upper and lower ends of the whiskers mark the non-outlier maximum and minimum values. Devices within each box plot are unique, and the same devices were retested after each fabrication step. All measurements were at room temperature and $V_{DS} = 0.1$ V.

device displayed both a larger V_T shift as well as improved transconductance ($g_m = \partial I_D/\partial V_{GS}$) and on-state current ($I_{on}$). Although the V_T shift could be attributed to doping from the capping layers, the geometry dependence and improved transconductance suggest that the origin of this enhancement arose from the stressed SiN$_x$, as we investigate below.

We first confirmed that the improvement was reproducible by measuring several (six to ten) devices with both long and short geometries, as shown with box plots in Fig. 2a,b. To account for V_T shifting, I_{on} was extracted at a carrier density[16,28] of $n \approx 8 \times 10^{12}$ cm^{-2}. The median I_{on} increased by 14% in the long devices after SiN$_x$ capping (Fig. 2a) and by 60% in the short devices (Fig. 2b). This demonstrates that the effect of high-stress capping was consistent between devices of the same type, with larger increases of I_{on} observed only for the smaller geometry. Other combinations of channel and contact length are shown in Supplementary Section 3, which confirms that both dimensions must be reduced to maximize the I_{on} improvement from this technique. These findings are consistent with those from silicon technology, where greater strain-induced increases in performance (I_{on}) have also been found for smaller devices[33].

Next, we fabricated control samples by capping with a low-stress (50 to 100 MPa) SiN$_x$ layer with the same thickness and deposition temperature as the high-stress (600 MPa) SiN$_x$ described above. Figure 2c,d compares the effect of different stress levels on the relative $I_{on}/I_{on,0}$ at $n \approx 8 \times 10^{12}$ cm^{-2} for both device geometries. (Here, $I_{on,0}$ was the current level after the AlO$_x$ barrier but before SiN$_x$ capping.) For long devices (Fig. 2c), both low- and high-stress SiN$_x$ layers led to similar results, with only a small improvement (~10%) of median I_{on}. However, for short devices, Fig. 2d shows that capping with high-stress SiN$_x$ increased the median I_{on} by nearly ~60%, compared to 18% with the low-stress SiN$_x$. This confirms that the large improvement originated from the high tensile stress in the SiN$_x$ rather than from annealing or doping, which would be similar for both low- and high-stress capping.

Finite-element simulations of the strain profile

To understand the origin of the performance enhancement achieved with high-stress SiN$_x$, we performed finite-element simulations of such BG devices with various channel and contact lengths to estimate the strain distribution. Figure 3a shows the cross section of a short 200 nm device, with arrows indicating the traction applied by the SiN$_x$ on the underlying AlO$_x$ as well as the resulting displacement field of the MoS$_2$. A zoomed-in, exaggerated deformation of the right contact overlaid with a colour map of the strain field along the channel direction is shown in Fig. 3b. The tensile SiN$_x$ 'pushes down' on the contact while simultaneously 'pulling' on its bottom corners[31], like a taut tape simultaneously squeezing and pulling on a small object placed beneath. (See Supplementary Fig. 4 for a simple representation of this effect using adhesive tape, a drinking straw and a kitchen sponge.)

Thus, the tensile SiN$_x$ layer imparts a complex, non-uniform strain profile along the MoS$_2$ contact and channel, with uniaxial tensile strain under the contact and compressive strain in the channel, as shown in Fig. 3c. (More simulation details are included in Supplementary Section 5.) This figure displays the strain along the MoS$_2$ for several cases of $L_{ch} = L_c$, from 1 µm to 20 nm. At longer dimensions ($L_{ch} = L_c > 150$ nm), the tensile strain under the contact is highest near the edges and decays towards the centre of the contact with a characteristic length of ~120 nm. The compressive strain in the channel is highest near the contact. We estimate tensile strains of 0.1–0.2% near the contact, although note that factors such as thermal expansion during SiN$_x$ deposition, changes in the elastic modulus of the MoS$_2$ due to defects, increases in the SiN$_x$ stress during pre-measurement annealing, and slipping between the MoS$_2$ and the substrate can increase this strain in the devices. When the dimensions are reduced, the tensile strain under the contact increases and becomes more uniform, and the channel strain eventually becomes tensile as well. (Other trends are explored in more detail in Supplementary Sections 6 and 7.) Based on these projections, we expect that this technique offers the most benefit at sub-50 nm contact pitches, for which both the channel and contact resistances could be greatly improved.

Tensile (compressive) strain distribution in or under mesa-like structures capped with tensile (compressive) stressors have been noted in the silicon literature[31,35] and exploited to enhance device performance[33]. For a 2D semiconductor like monolayer MoS$_2$, tensile strain is expected to lower the K valley of the conduction band[18,22], bringing it closer to the Fermi level under our contacts and reducing the Schottky barrier height[36] (inset of Fig. 3c). In addition, the 'downward' pressure exerted by the tensile-strained contacts on the MoS$_2$ (Supplementary Section 8) could reduce the metal–MoS$_2$ van der Waals gap at the contact[37,38], thus improving electron tunnelling. The corresponding reduction of the contact resistance[39] is the probable mechanism for the performance enhancement seen in our devices capped with high-tensile-stressed SiN$_x$, with the greatest enhancement in our short (more contact-dominated) devices (Fig. 2d). Importantly, we also found that further performance enhancements are possible when the channel and contact lengths are scaled down towards 20 nm, due to increased strain under the contacts, as well as the channel going from compressive to tensile strain, which could substantially increase the channel mobility[18,22].

To examine the effect of stress on the contacts, we estimated the Schottky barrier height of devices capped with high-tensile-stressed SiN$_x$. As shown in Supplementary Section 9, we extracted an effective barrier of ~60 meV, which is lower than our control sample measurements and other values from the literature (120–150 meV)[40]. We also performed a pseudo-transfer length analysis (Supplementary Section 10), which confirmed that devices with short dimensions exhibit lower contact resistance. These results corroborate the findings

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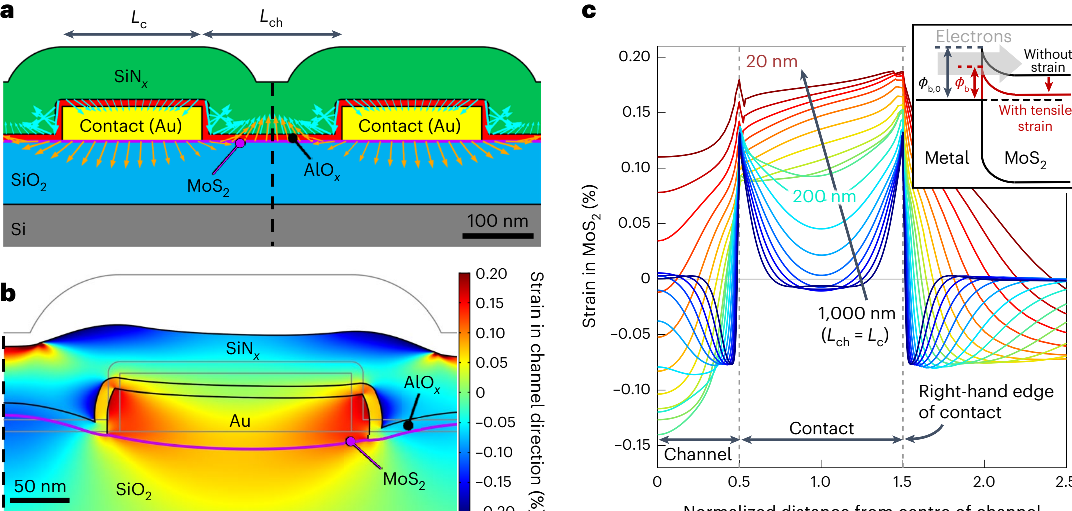

Fig. 3 | Strain simulations. a, Cross section of the short device with $L_{ch} = L_c = 200$ nm. The horizontal magenta line shows the location of the monolayer MoS_2. Cyan arrows indicate the traction applied by the SiN_x stressor layer on the underlying AlO_x. Orange arrows indicate the displacement of the MoS_2 after the structure is allowed to relax. The vertical dashed line marks the centre of the device (the symmetry plane). **b**, Zoom-in of the simulated right-hand contact region, overlaid with a heat map showing the horizontal strain field (tensile strain is positive). Deformations are exaggerated by a factor of 200. Grey lines are the material boundaries before deformation. **c**, Strain profile along the horizontal direction for devices with $L_{ch} = L_c$ from 1 µm down to 20 nm. Note that distances are normalized by the channel length. The inset illustrates the effect of tensile strain on the Schottky barrier at the MoS_2 contact.

of our finite-element simulations and show how strain can be used for CMOS-compatible contact engineering with 2D semiconductor transistors.

Strained DG field-effect transistors

Next, we extended our strain technique to DG transistors (schematic in Fig. 4a), which have a Pd top gate above the AlO_x encapsulation layer described earlier. As with the earlier BG transistors, we fabricated devices with different values of L_{ch} and L_c (up to 2 µm for the longest DG devices) and measured their electrical characteristics before and after capping with the SiN_x stress layer above the top gate (TG). A scanning electron microscope image of an encapsulated, short, DG device ($L_{ch} = L_c = 200$ nm) is shown in Fig. 4b. For optimal control of the transistor characteristics, we swept both the top-gate voltage (V_{TG}) and the back-gate voltage (V_{BG}) simultaneously, but with different ranges and voltage steps due to the unequal TG and BG dielectrics.

Figure 4c displays the electrical measurements of such a short device. After the high-tensile-stressed SiN_x capping, I_{on} increases by 33% (at maximum applied V_{BG} and V_{TG}), with only a small negative V_T shift. Any possible charge transfer doping from the SiN_x encapsulation is effectively blocked by the top gate, which fully overlaps the channel and contacts. The transconductance (slope, g_m) increases by 32% after the SiN_x capping, underlining that the higher I_{on} is almost entirely due to strain-induced improvements in mobility and contact resistance. Small V_T shifts due to strain are not unexpected (due to changes in the band gap) and have also been observed in silicon technology[41] but can be compensated for by gate stack engineering[42]. In addition, the larger band gap of monolayer TMDs (~2 times larger than Si) implies that any trade-offs in the off-state current will be easier to manage than in silicon.

The output characteristics in Fig. 4d reveal a drain saturation current of $I_{D,sat} = 488$ µA µm^{-1} (394 µA µm^{-1}) at $V_{DS} = 2$ V (1 V), which represents a high value for a 200 nm monolayer MoS_2 channel (with 400 nm contact pitch), in a device without otherwise optimized metal contacts or gate dielectrics. This is an important finding, which signifies that strained (but otherwise ordinary) contacts can yield device performance like that of the best Bi or Sb contacts available today[14,15]. The CMOS-compatible strain approach employed in this work is agnostic to the type of contacts, which opens the door to future device optimization with more industry-friendly metals.

We summarize measurements of several DG transistors with short (200 nm) and long (2 µm) geometries in Fig. 4e. For long devices, I_{on} increased only a few percent after high-stress capping. In contrast, short devices displayed a large median I_{on} increase of 45%. This effect was reproducible across all properly strained transistors and confirmed our findings for BG devices (Figs. 2 and 3) that strain boosts the performance of devices with smaller channel length and contact pitch (here, 200 and 400 nm, respectively). On a separate test chip, we found that short DG devices which used MoS_2 grown at lower temperature[11] (and, thus, were more weakly adhered to the substrate) suffered partial delamination due to the SiN_x strain and displayed no improvement in their I_{on} (Supplementary Section 11), again confirming the strain-related source of improvement in our short well-adhered devices. For properly strained devices, our DG simulations in Supplementary Section 6 show similar strain distributions as in BG transistors, indicating the performance increase is primarily due to the tensile contact strain and projecting further enhancement in smaller devices. These simulations also provide design guidelines on how channel and contact dimensions independently affect the strain.

Finally, we tested the stability of our method by measuring the transistor characteristics over time (Fig. 4f). After 7 months, the device showed no degradation of the on-state current, even when the measurements were performed in air, illustrating that SiN_x also offers robust encapsulation, which has been well studied for Si transistors as a diffusion barrier to moisture and gases[26,43]. Our CMOS-compatible strain technique could also be applied to other TMDs, which are expected to benefit from tensile strain[17], such as monolayer WSe_2 (Supplementary Section 12). We anticipate that this approach will offer further improvements to 2D semiconductor transistors with even shorter critical dimensions, paving the way for the implementation of CMOS-compatible strain in high-performance TMD devices.

Conclusions

We have reported a CMOS-compatible approach for creating strain in 2D semiconductor transistors down to nanoscale dimensions using low-temperature, tensile-stressed, silicon nitride capping layers. The

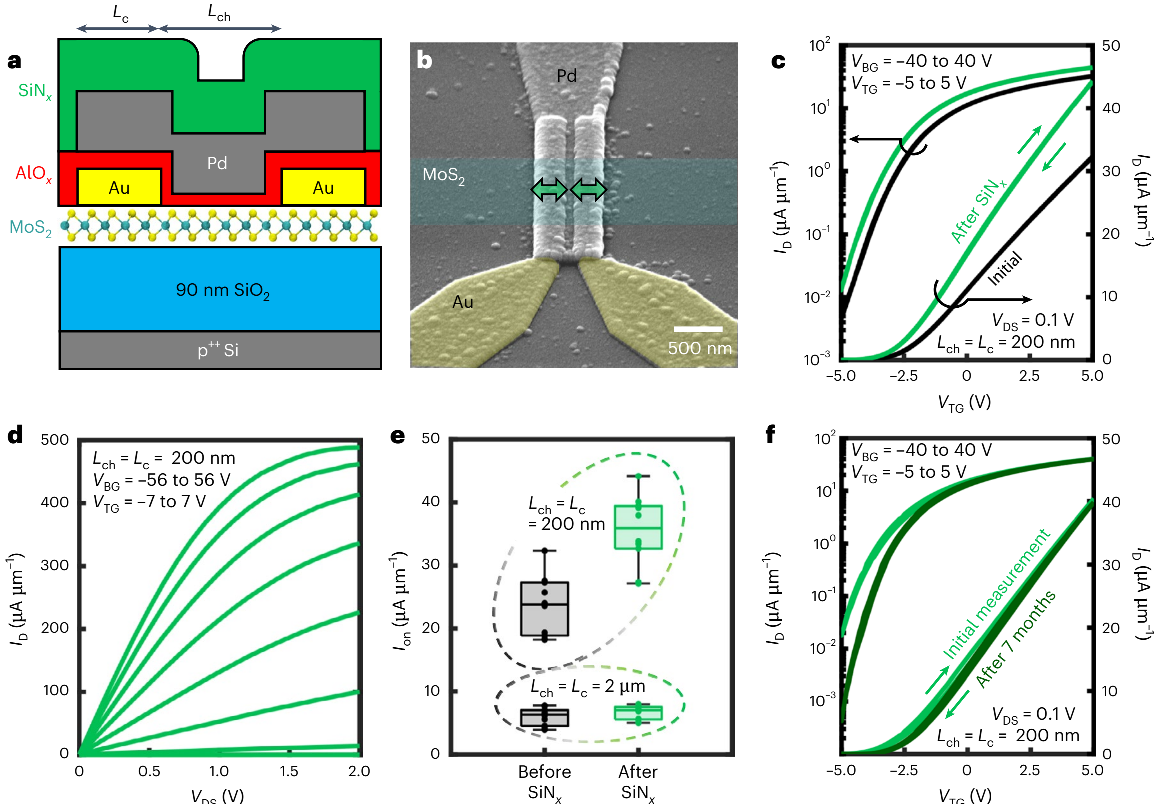

Fig. 4 | DG transistors with strain. **a**, Schematic of device structure for a DG (TG and BG) monolayer MoS_2 transistor capped with AlO_x and tensile-stressed SiN_x. **b**, Tilted, colourized, scanning electron microscope image of a short device with channel and contact lengths of 200 nm. The top Pd gate overlaps both the source and drain contacts. The green arrows represent the effect of the tensile-stressed SiN_x cap, which is otherwise transparent in this image. **c**, Transfer characteristics for a DG high-stress (~800 MPa) SiN_x-capped monolayer MoS_2 transistor with dimensions $L_{ch} = L_c = 200$ nm. **d**, Output characteristics after SiN_x capping, displaying on-state current $I_{D,sat} = 488$ μA μm^{-1} (with proper saturation at $V_{DS} = 2$ V) when both top and back gates are set to high bias. Each voltage step was 16 V on the back gate and 2 V on the top gate. **e**, Box plots summarizing the change in I_{on} at $V_{DS} = 0.1$ V for DG devices with long and short dimensions (ten devices each) after SiN_x capping. The middle line in each box plot marks the median value. Upper and lower box ranges indicate the upper and lower quartiles, while upper and lower ends of the whiskers mark the non-outlier maximum and minimum values. Devices within each box plot are unique, and the same devices were retested after each fabrication step. **f**, Transfer characteristics of a SiN_x-capped device after 7 months, showing no visible degradation of the on-state current. Measurements were performed in air at room temperature. Small arrows mark the forward and backward sweeps[44]. With SiN_x encapsulation, there was minimal hysteresis over this voltage range. For both **c** and **f**, the V_{BG} and V_{TG} step sizes had a ratio of 8:1, proportional to their respective voltage sweep ranges.

technique improves the performance of monolayer MoS_2 transistors up to 60%, reaching a saturation current of 488 μA μm^{-1} at a contact pitch of just 400 nm (channel plus contact). Simulations reveal that strain is expected to impart even greater benefits in transistors with smaller contact pitches, for example sub-50 nm. The results of this study will benefit the integration of 2D semiconductors into future electronics and could also motivate the exploration of strain engineering in other next-generation semiconductors.

Methods

Device fabrication and measurement

Monolayer MoS_2 was synthesized by CVD at 750 °C directly onto thermally grown SiO_2 (90 nm) on 1.5 cm × 2 cm p^{++} silicon substrates[28]. For the BG devices, the MoS_2 was used directly on the growth substrates, such that the p^{++} Si also served as the back gate. E-beam lithography (Raith VOYAGER) was used for each patterning step. The e-beam resist was made from poly(methyl methacrylate) to minimize potential delamination due to the aqueous developers used in photolithography. First, alignment marks (2 nm Ti/40 nm Au) were patterned and deposited by lift-off after e-beam evaporation. Discrete single-crystal MoS_2 triangles were identified under a microscope and lithography masks were designed such that each device was fabricated within a single triangle of MoS_2 in regions with minimal overgrowth. The channel dimensions were then defined using XeF_2 etching for 90 s at 3 Torr (Xactix e-1). Large probing pads (20 nm SiO_2/2 nm Ti/20 nm Pt) were then patterned and deposited by lift-off, with the evaporated SiO_2 layer serving to reduce any potential leakage to the back gate. Finally, source and drain device contacts (50 nm Au without an adhesion layer[16]), which connect the MoS_2 channels to the probing pads, were patterned and deposited by lift-off using e-beam evaporation at $<5 \times 10^{-8}$ Torr and a rate of 0.5 Å s^{-1}. All lift-off processes were performed in acetone for a minimum of 2 h.

Next, e-beam evaporation was used to deposit a 1.5 nm Al film[12] onto the finished BG devices. The Al oxidized in air to substoichiometric AlO_x. Subsequently, 10 nm Al_2O_3 was deposited by atomic layer deposition at 200 °C (Cambridge Nanotech Savannah S200). This served as the barrier layer before SiN_x capping for BG devices and as the TG insulator for DG devices. At this stage, the Al_2O_3 was wet-etched (JT-Baker, Aluminum etch) over the contact pads after optical lithography. BG devices were then encapsulated by SiN_x, which was removed from only over the contact pads after optical lithography and CF_4 plasma etching (Samco PC300). For DG devices, e-beam lithography was used to define the gate metal (50 nm Pd) by lift-off, followed by SiN_x deposition and contact access as described above.

All transistors were tested with a Keithley 4200 semiconductor parameter analyser. BG transistors were measured in a Janis ST-500 probe station under ~10^{-5} Torr vacuum after in situ annealing at 250 °C for 2 h. DG transistors were measured in air due to the minimal

hysteresis after encapsulation. All measurements were done at room temperature unless otherwise stated.

Silicon nitride deposition

Silicon nitride (SiN_x) was deposited using plasma-enhanced CVD in a PlasmaTherm Shuttlelock PECVD system using SiH_4 (5% in He) and NH_3 gases. Several recipes were developed to control the resultant film stress, and we found that the main process variable for controlling the stress was the ratio of NH_3 to SiH_4. At higher ratios of NH_3:SiH_4 >1, the film stress became tensile, whereas lower ratios promoted compressive stress (see Supplementary Section 1 for more details). Additionally, the amount of He in the process chamber can be used to further tune the stress if needed. For the transistors in this work, the deposition temperature was set to 350 °C, although this could be reduced to as low as 130 °C, both temperatures being back-end-of-line compatible. The deposition powers were tuned from 20 to 100 W. Process pressures between 1 and 2 Torr resulted in deposition rates between 10 and 15 nm min^{-1}. Films were characterized using ellipsometry, which precisely fitted both the refractive index and thickness. This accurate information about the deposition was necessary for making accurate stress measurements. The film stress was measured on reference 4 inch silicon wafers by a Flexus 2320 Stress Tester using radius of curvature measurements before and after deposition.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

References

1. Thompson, S. et al. A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low *k* ILD, and 1 μm² SRAM cell. In *Proc. IEEE International Electron Devices Meeting* 61–64 (IEEE, 2002).
2. Ghani, T. et al. A 90 nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. In *Proc. IEEE International Electron Devices Meeting* 978–980 (IEEE, 2003).
3. Welser, J., Hoyt, J. & Gibbons, J. NMOS and PMOS transistors fabricated in strained silicon/relaxed silicon-germanium structures. In *Proc. IEEE International Electron Devices Meeting* 1000–1002 (IEEE, 1992).
4. Rim, K., Hoyt, J. L. & Gibbons, J. F. Transconductance enhancement in deep submicron strained-Si n-MOSFETs. In *Proc. IEEE International Electron Devices Meeting* 707–710 (IEEE, 1998).
5. Takagi, S. I., Hoyt, J. L., Welser, J. J. & Gibbons, J. F. Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors. *J. Appl. Phys.* **80**, 1567–1577 (1996).
6. Ito, S. et al. Mechanical stress effect of etch-stop nitride and its impact on deep submicron transistor design. In *Proc. IEEE International Electron Devices Meeting* 247–250 (IEEE, 2000).
7. Shimizu, A. et al. Local mechanical-stress control (LMC): a new technique for CMOS-performance enhancement. In *Proc. IEEE International Electron Devices Meeting* 433–436 (IEEE, 2001).
8. Armstrong, M. et al. Delaying forever: uniaxial strained silicon transistors in a 90 nm CMOS technology. In *Proc. Symposium on VLSI Technology* 50–51 (IEEE, 2004).
9. Das, S. et al. Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* **4**, 786–799 (2021).
10. Zhu, J. et al. Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform. *Nat. Nanotechnol.* **18**, 456–463 (2023).
11. Tang, A. et al. Toward low-temperature solid-source synthesis of monolayer MoS_2. *ACS Appl. Mater. Interfaces* **13**, 41866–41874 (2021).
12. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).
13. Lan, H.-Y., Oleshko, V. P., Davydov, A. V., Appenzeller, J. & Chen, Z. Dielectric interface engineering for high-performance monolayer MoS_2 transistors via TaO_x interfacial layer. *IEEE Trans. Electron Devices* **70**, 2067–2074 (2023).
14. Shen, P.-C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
15. Li, W. et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).
16. English, C. D., Shine, G., Dorgan, V. E., Saraswat, K. C. & Pop, E. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett.* **16**, 3824–3830 (2016).
17. Hosseini, M., Elahi, M., Pourfath, M. & Esseni, D. Strain-induced modulation of electron mobility in single-layer transition metal dichalcogenides MX_2 (M = Mo, W; X = S, Se). *IEEE Trans. Electron Devices* **62**, 3192–3198 (2015).
18. Hosseini, M., Elahi, M., Pourfath, M. & Esseni, D. Strain induced mobility modulation in single-layer MoS_2. *J. Phys. D: Appl. Phys.* **48**, 375104 (2015).
19. Sohier, T. et al. Enhanced electron-phonon interaction in multivalley materials. *Phys. Rev. X* **9**, 031019 (2019).
20. Peña, T. et al. Strain engineering 2D MoS_2 with thin film stress capping layers. *2D Mater.* **8**, 045001 (2021).
21. Michail, A., Delikoukos, N., Parthenios, J., Galiotis, C. & Papagelis, K. Optical detection of strain and doping inhomogeneities in single layer MoS_2. *Appl. Phys. Lett.* **108**, 173102 (2016).
22. Datye, I. M. et al. Strain-enhanced mobility of monolayer MoS_2. *Nano Lett.* **22**, 8052–8059 (2022).
23. Yang, J. A. et al. Biaxial tensile strain enhances electron mobility of monolayer transition metal dichalcogenides. *ACS Nano* **18**, 18151–18159 (2024).
24. Chai, Y. et al. Strain gated bilayer molybdenum disulfide field effect transistor with edge contacts. *Sci. Rep.* **7**, 41593 (2017).
25. Zhang, Y., Zhao, H. L., Huang, S., Hossain, M. A. & van der Zande, A. M. Enhancing carrier mobility in monolayer MoS_2 transistors with process-Induced strain. *ACS Nano* **18**, 12377–12385 (2024).
26. Kaloyeros, A. E., Jové, F. A., Goff, J. & Arkles, B. Review—silicon nitride and silicon nitride-rich thin film technologies: trends in deposition techniques and related applications. *ECS J. Solid State Sci. Technol.* **6**, 691–714 (2017).
27. Mackenzie, K. D., Johnson, D. J., Devre, M. W., Westerman, R. J. & Reelfs, B. H. Stress control of Si-based PECVD dielectrics. In *Proc. 207th Electrochemical Society Meeting* 148–159 (ECS, 2005).
28. Smithe, K. K. H., English, C. D., Suryavanshi, S. V. & Pop, E. Intrinsic electrical transport and performance projections of synthetic monolayer MoS_2 devices. *2D Mater.* **4**, 011009 (2017).
29. Mignuzzi, S. et al. Effect of disorder on Raman scattering of single-layer MoS_2. *Phys. Rev. B* **91**, 195411 (2015).
30. Schauble, K. et al. Uncovering the effects of metal contacts on monolayer MoS_2. *ACS Nano* **14**, 14798–14808 (2020).
31. Reboh, S., Morin, P., Hÿtch, M. J., Houdellier, F. & Claverie, A. Mechanics of silicon nitride thin-film stressors on a transistor-like geometry. *APL Mater.* **1**, 042117 (2013).
32. Hüe, F., Hÿtch, M., Bender, H., Houdellier, F. & Claverie, A. Direct mapping of strain in a strained silicon transistor by high-resolution electron microscopy. *Phys. Rev. Lett.* **100**, 156602 (2008).
33. Thompson, S. E. et al. A 90-nm logic technology featuring strained-silicon. *IEEE Trans. Electron Devices* **51**, 1790–1797 (2004).
34. Leonhardt, A. et al. Material-selective doping of 2D TMDC through Al_xO_y encapsulation. *ACS Appl. Mater. Interfaces* **11**, 42697–42707 (2019).

35. Thompson, S. E., Sun, G., Choi, Y. S. & Nishida, T. Uniaxial-process-induced strained-Si: extending the CMOS roadmap. *IEEE Trans. Electron Devices* **53**, 1010–1020 (2006).
36. John, A. P., Thenapparambil, A. & Thalakulam, M. Strain-engineering the Schottky barrier and electrical transport on MoS_2. *Nanotechnology* **31**, 275703 (2020).
37. Manzanares-Negro, Y. et al. Low resistance electrical contacts to few-layered MoS_2 by local pressurization. *2D Mater.* **10**, 021003 (2023).
38. Chen, Y. et al. Pressurizing field-effect transistors of few-layer MoS_2 in a diamond anvil cell. *Nano Lett.* **17**, 194–199 (2017).
39. Jaikissoon, M., Pop, E. & Saraswat, K. C. Strain induced by evaporated-metal contacts on monolayer MoS_2 transistors. *IEEE Electron Device Lett.* **45**, 1528–1531 (2024).
40. Kaushik, N. et al. Schottky barrier heights for Au and Pd contacts to MoS_2. *Appl. Phys. Lett.* **105**, 113505 (2014).
41. Lim, J. S., Thompson, S. E. & Fossum, J. G. Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs. *IEEE Electron Device Lett.* **25**, 731–733 (2004).
42. Hashemi, P. et al. High performance and reliable strained SiGe PMOS FinFETs enabled by advanced gate stack engineering. In *Proc. 2017 IEEE International Electron Devices Meeting (IEDM)* 37.3.1–37.3.4 (IEEE, 2017).
43. Late, D. J., Liu, B., Matte, H. S. S. R., Dravid, V. P. & Rao, C. N. R. Hysteresis in single-layer MoS_2 field effect transistors. *ACS Nano* **6**, 5635–5641 (2012).
44. Cheng, Z. et al. How to report and benchmark emerging field-effect transistors. *Nat. Electron.* **5**, 416–423 (2022).

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Author contributions

M.J., E.P. and K.C.S. conceived the work. M.J. performed the MoS_2 synthesis, SiN_x recipe development, device fabrication, optical characterization, electrical measurements and scanning electron microscopy. C.K. contributed all the numerical simulations of the strain profiles. K.N. performed the WSe_2 synthesis and atomic layer deposition with J.A.Y. M.J. analysed all the data and wrote the manuscript with help from C.K. and E.P. All authors have given approval to the final version of the manuscript.

Competing interests

The authors declare no competing interests.

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CMOS-compatible strain engineering for monolayer semiconductor transistors

In the format provided by the authors and unedited

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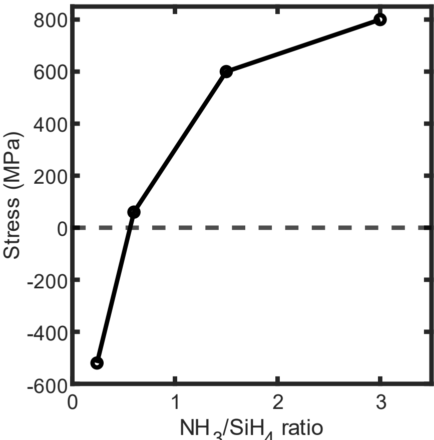
1. Silicon Nitride Film Stress Measurement

We benchmark our SiN_x deposition by measuring film stress on reference 4” silicon wafers as described in the Methods section. The Stoney equation $r = (E_s t_s^2)/[6(1-\nu_s)\sigma_f t_f]$ was used, where r is the radius of curvature of the sample measured by laser deflection, σ_f is the desired film stress, t_f is the film thickness measured by ellipsometry, ν_s is the Poisson’s ratio of the substrate, t_s is the substrate thickness and E_s is the Young’s modulus of the substrate. **Supplementary Figure 1** shows the measured film stress of several SiN_x films deposited with various ratios of NH_3:SiH_4, demonstrating the tunable nature of stress from compressive (nearly -600 MPa) to tensile (≈ 800 MPa).

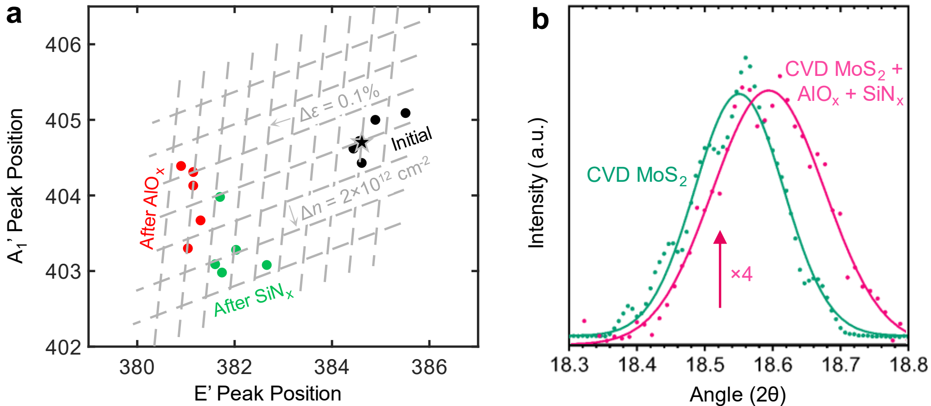


Supplementary Figure 1 | SiN_x stress measurement. Measured film stress in SiN_x deposited by PE-CVD at 350 °C as a function of NH_3:SiH_4 precursor ratio.

2. Raman and XRD Analysis of Strain in As-Grown and Encapsulated MoS_2 Films

We acquired Raman spectra at each stage of encapsulation of a blanket MoS_2 film (on SiO_2/Si), and the fitted E' vs. A_1' peak positions[1] are summarized in **Supplementary Figure 2a** below. The AlO_x capping (1.5 nm Al seed + 10 nm Al_2O_3 by ALD) causes a large, nearly ≈ 4 cm^{-1}, redshift of the E' peak of MoS_2. This would appear to imply a tensile strain > 0.75%, however we have found in previous work[2] that Raman analysis greatly overestimates MoS_2 strain under AlO_x encapsulation (as compared to accurate X-ray diffraction measurements). The apparent shift of the E' peak is instead caused by doping and plasmon coupling of the MoS_2 with the AlO_x encapsulation layer.

We could still gain some insight into the effect of blanket tensile SiN_x deposition (on AlO_x/MoS_2) by comparing peak positions before and after SiN_x capping (green dots), which indicates slight compression ($\Delta\varepsilon \approx -0.15\%$) relative to AlO_x/MoS_2 data points (red dots), as well as increased electron doping ($\Delta n \approx 5\times10^{12}$ cm^{-2}). This has been well-documented in the literature[3], and indicates that compressive strain is created in MoS_2 if a tensile SiN_x layer is deposited on an *unpatterned* film. (The tensile SiN_x contracts to relieve its built-in stress, in the process compressing the MoS_2 underneath.)



Supplementary Figure 2 | Estimating strain by Raman and X-Ray Diffraction on unpatterned MoS_2. a, Raman E' vs. A_1' peak positions acquired at several spots on unpatterned, as-grown MoS_2 (on SiO_2/Si) before and after encapsulation with AlO_x and then SiN_x. Dashed lines mark expected strain (ε) and electron density (n) changes[1]. We emphasize that the apparent strain after AlO_x coverage (~0.75%) is greatly overestimated by Raman analysis[2]. **b,** Grazing-incidence X-ray diffraction spectra acquired on as-grown MoS_2 before and after capping with AlO_x and high-tensile stress SiN_x.

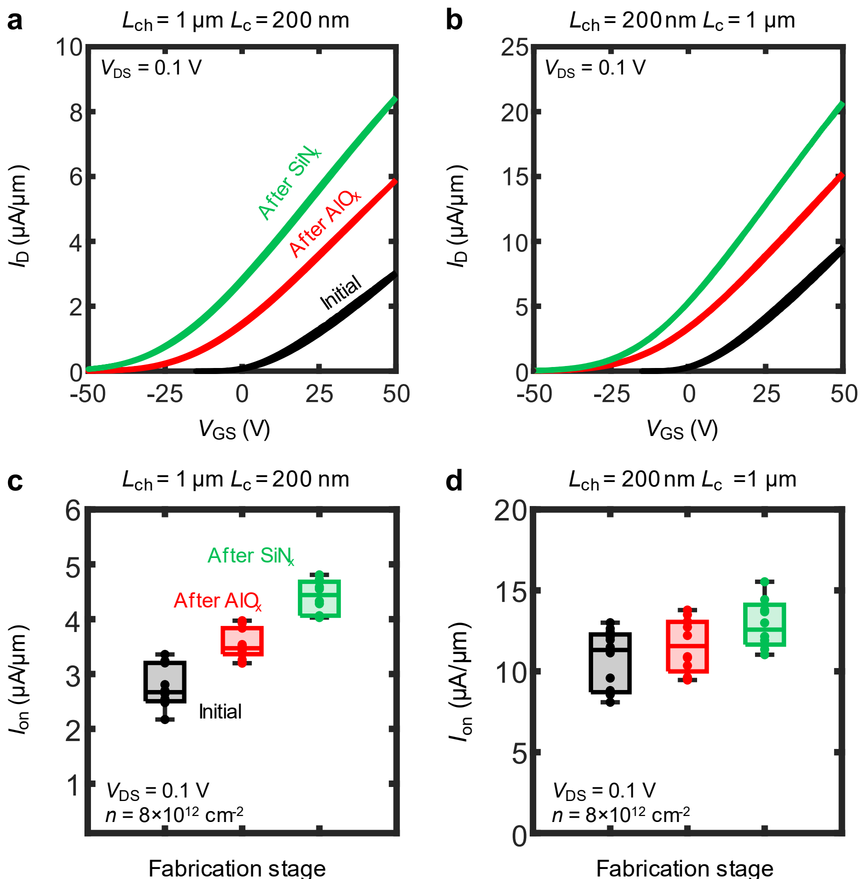
To probe strain more accurately in unpatterned MoS_2 films, we used grazing incidence X-ray diffraction measurements with a synchrotron X-ray source on as-grown MoS_2, before and after capping with AlO_x and high-tensile stress SiN_x, as shown in **Supplementary Figure 2b**. We observe an increase of

0.0422° of the in-plane (10) peak position of MoS_2, corresponding to a compressive biaxial strain of -0.23% after capping, again consistent with expectations for *unpatterned* films.

However, we note that both the Raman laser and X-ray spot sizes are large (~0.5 µm to several mm), which makes strain mapping difficult using these techniques in any sub-micron devices. Additionally, neither approach allows characterization of the full strain profile across a transistor including the regions of MoS_2 under the (metal) contacts and top gate, indicating the need for more sophisticated metrologies, such as transmission electron microscopy (TEM)[4,5], to measure strain in nanoscale devices. Therefore, we used finite element simulations (main text **Figure 3** and **Supplementary Information Sections 5-8**) to provide insight into the strain profiles and distributions in capped MoS_2, particularly within our nanoscale transistors (where strain is uniaxial, due to the presence of contacts). Such simulations have also been adopted for nanoscale silicon devices[4,5], and have been found in agreement with TEM-based metrology.

3. Other Back-gated Channel and Contact Combinations

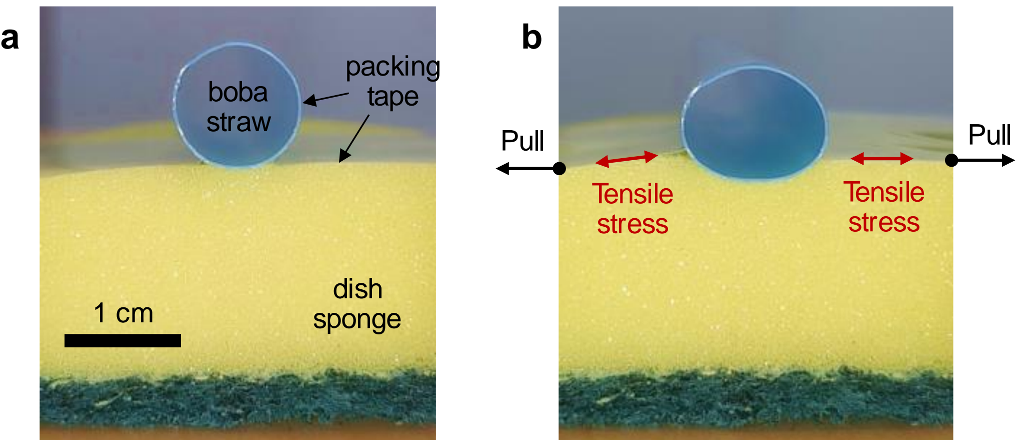
In addition to using 'long' and 'short' geometries (channel and contact length $L_{ch} = L_c = 1$ μm and 200 nm, respectively) mentioned in the main text, we also tested other combinations of L_{ch} and L_c. The drain current vs. gate voltage (I_D-V_{GS}) of devices with $L_{ch} = 1$ μm, $L_c = 200$ nm and $L_{ch} = 200$ nm, $L_c = 1$ μm are shown in **Supplementary Figure 3a,b**. Both cases demonstrate negative threshold voltage (V_T) shifts as reported for the devices in the main text after AlO_x and SiN_x capping, as well as improvements to transconductance ($g_m = \partial I_D/\partial V_{GS}$). Normalizing by carrier density to account for V_T shifts, box plots of I_{on} extracted at a carrier density of $n \approx 8\times10^{12}$ cm^{-2} are shown for $L_{ch} = 1$ μm, $L_c = 200$ nm



Supplementary Figure 3 | Characterization of other back-gated transistor geometries. Back-gated transfer characteristics of high-stress SiN_x-capped MoS_2 transistor with **a,** $L_{ch} = 1$ μm, $L_c = 200$ nm and **b,** $L_{ch} = 200$ nm, $L_c = 1$ μm. Box plots of normalized on-state current (I_{on}) at $n = 8\times10^{12}$ cm^{-2} for several devices, after each fabrication step. **c,** $L_{ch} = 1$ μm, $L_c = 200$ nm (10 devices) and **d,** $L_{ch} = 200$ nm, $L_c = 1$ μm (12 devices). The middle line in each box plot marks the median value, whereas the upper and lower ranges indicate the upper and lower quartiles. The upper and lower ends of the whiskers represent the nonoutlier maximum and minimum values, respectively. Devices within each box plot are unique, with the same devices being retested after each fabrication step. All measurements are carried out at room temperature and $V_{DS} = 0.1$ V.

and L_{ch} = 200 nm, L_c = 1 μm in **Supplementary Figure 3c,d**. We observe that I_{on} only increases by up to 27% for these combinations, indicating that larger improvements are only possible when both L_{ch} and L_c are reduced, as in the main text. Here and in the main text (e.g. Figure 2) the electron density per unit area is estimated[10] as $n \approx C_{ox}(V_{GS} - V_T - V_{DS}/2)/q$, where q is the elementary charge. Throughout this study, the back-gate oxide capacitance per unit area is $C_{ox} \approx 38$ nF/cm^2, corresponding to the 90 nm of SiO_2.

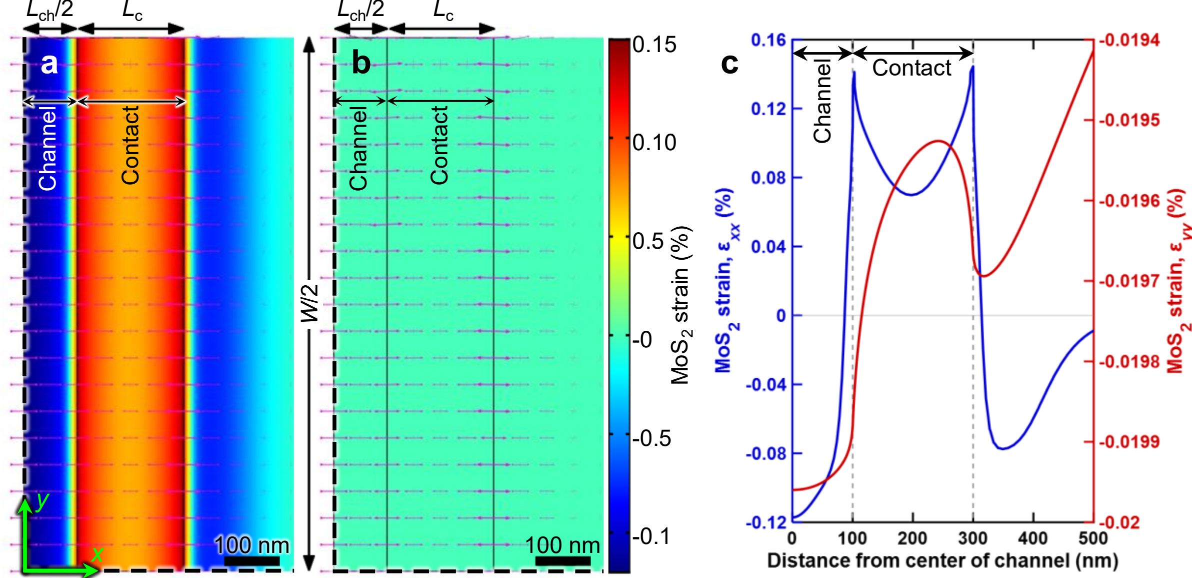
4. Macroscopic Visual Model of Deformation due to Tensile-Stressed Capping Layer



Supplementary Figure 4 | Visualization of contact electrode deformation by tensile strain, using everyday objects. a, The cross-section of a simple macroscopic visual analogy for the contact geometry of a back-gated MoS_2 transistor. Here, a plastic straw (from boba tea) stands in for the contact electrode, a dish sponge for the materials under the electrode ($MoS_2/SiO_2/Si$), and a layer of transparent packing tape (covering the top of the sponge and wrapping as an "Ω" around the straw) for the SiN_x film, initially unstressed. **b,** Contact deformation visualized when the adhesive packing tape is laterally tensile-stressed by pulling it outward from the sides, similar to the exaggerated simulated device deformation shown in **Figure 3b** of the main text.

5. Stress Simulations: Additional Information

Two-dimensional (2D) and three-dimensional (3D) stress simulations were performed for back-gated (BG) and dual-gated (DG) transistors, assuming linear elasticity. We confirmed through 3D simulations that the MoS_2 strain in the transistor width direction is small (i.e. MoS_2 strain is essentially uniaxial), as illustrated by **Supplementary Figure 5**. Consequently, 2D simulations are sufficient to accurately capture the uniaxial stress and strain distributions in our devices, and the results presented in this work were obtained through 2D simulations. After multi-scale simulations of the entire sample (including the transistor and the entire silicon substrate) confirmed that strains due to substrate bowing were negligible, later simulations used a smaller domain around the BG transistor with a fixed boundary condition at the bottom of a thinner section of substrate, with no appreciable errors in stress and strain distributions.



Supplementary Figure 5 | In-plane strain distribution across the device. a, b, The distributions of lengthwise in-plane strain (ε_{xx} given in **a**) and widthwise in-plane strain (ε_{yy} given in **b**) in MoS_2 in a BG transistor (with 600 MPa tensile-stressed SiN_x capping) for $L_{ch} = L_c = 200$ nm, as viewed from above. The bottom left corner corresponds to the center of the device, with the dashed lines indicating the two symmetry planes. The magenta arrows indicate the principal strain directions and values at each point, showing that the strain is predominantly in the direction of current flow (i.e. along the *x*-axis), and hence uniaxial. **c**, MoS_2 strains ε_{xx} (left axis) and ε_{yy} (right axis) along positive *x*-axis of the same device showing the widthwise strain is small, with a nearly uniform compressive strain < 0.02% in magnitude.

An isotropic "initial stress" (the stress before the geometry is allowed to relax) of 600 MPa was assumed in the SiN_x capping layer. The isotropic elastic properties assumed for the materials other than

MoS_2 are summarized in **Supplementary Table 1**. In contrast, MoS_2 is only transversely isotropic (i.e. isotropic in-plane), and thus is described by an anisotropic stiffness tensor. The elastic properties were taken from Li *et al.*[6], and can be summarized as $E_{xx} = E_{yy} = 265$ GPa, $E_{zz} = 100$ GPa, $G_{xz} = G_{yz} = 50$ GPa, and $\nu_{xy} = \nu_{yx} = \nu_{xz} = \nu_{yz} = 0.25$. Here, x and y correspond to the in-plane directions and z to the cross-plane direction, E denotes Young's modulus, G denotes shear modulus and ν_{ij} denotes Poisson's ratio for loading along i and transverse direction j. The remaining elastic properties can be determined from these, e.g. $\nu_{zx} = (E_{zz}/E_{xx})\nu_{xz}$ and $G_{xy} = E_{xx}/[2(1 + \nu_{xy})]$.

Supplementary Table 1: Young's moduli and Poisson's ratios assumed for materials except for MoS_2.

	Si	**SiO_2**	**AlO_x**	**SiN_x**	**Au**	**Pd**
Young's modulus (GPa)	170	70	400	250	70	73
Poisson's ratio	0.28	0.17	0.22	0.23	0.44	0.44

The MoS_2 grown by CVD (at 750 °C) directly on SiO_2 is tensile-stressed, which has been attributed to the mismatch in coefficients of thermal expansion[7–9] α_{MoS2} and α_{SiO2}. To model this observation, we take $\alpha_{MoS2} = 7\times10^{-6}$ K^{-1} and $\alpha_{SiO2} = 2\times10^{-6}$ K^{-1}, yielding an initial thermally-induced strain of $(\alpha_{MoS2} - \alpha_{SiO2})(T_{growth} - T_{ambient}) \cong 0.37\%$ in MoS_2, which represents the tensile strain in a planar MoS_2 film as-grown, relative to relaxed MoS_2. The in-plane strains reported in this work are all relative to MoS_2 as-grown: the residual MoS_2 strain (assumed 0.37% here) should be added to these values to obtain strains relative to relaxed MoS_2. We note that the built-in tensile stress in MoS_2 has negligible effect on the in-plane strains in MoS_2 in the relaxed structure, because MoS_2 is so thin and its film force (stress times thickness) is small compared to that effected by the stress in SiN_x. In other words, the MoS_2 strain is dictated mainly by the adjacent materials, and ultimately caused by the tensile stress in SiN_x.

We also note that it is possible for there to be some amount of slipping between MoS_2 and adjacent materials due to poor adhesion. While the quantitative details of this process are scarce and slipping is not included in the results we present, if MoS_2 is allowed to slip freely on the underlying SiO_2, simulations predict that the strains in both the channel and under the contacts increase by up to ~50%, and the strain peaks near the contact edges become more "rounded." However, the trends in the main text and **Supplementary Information Section 6** otherwise stay the same.

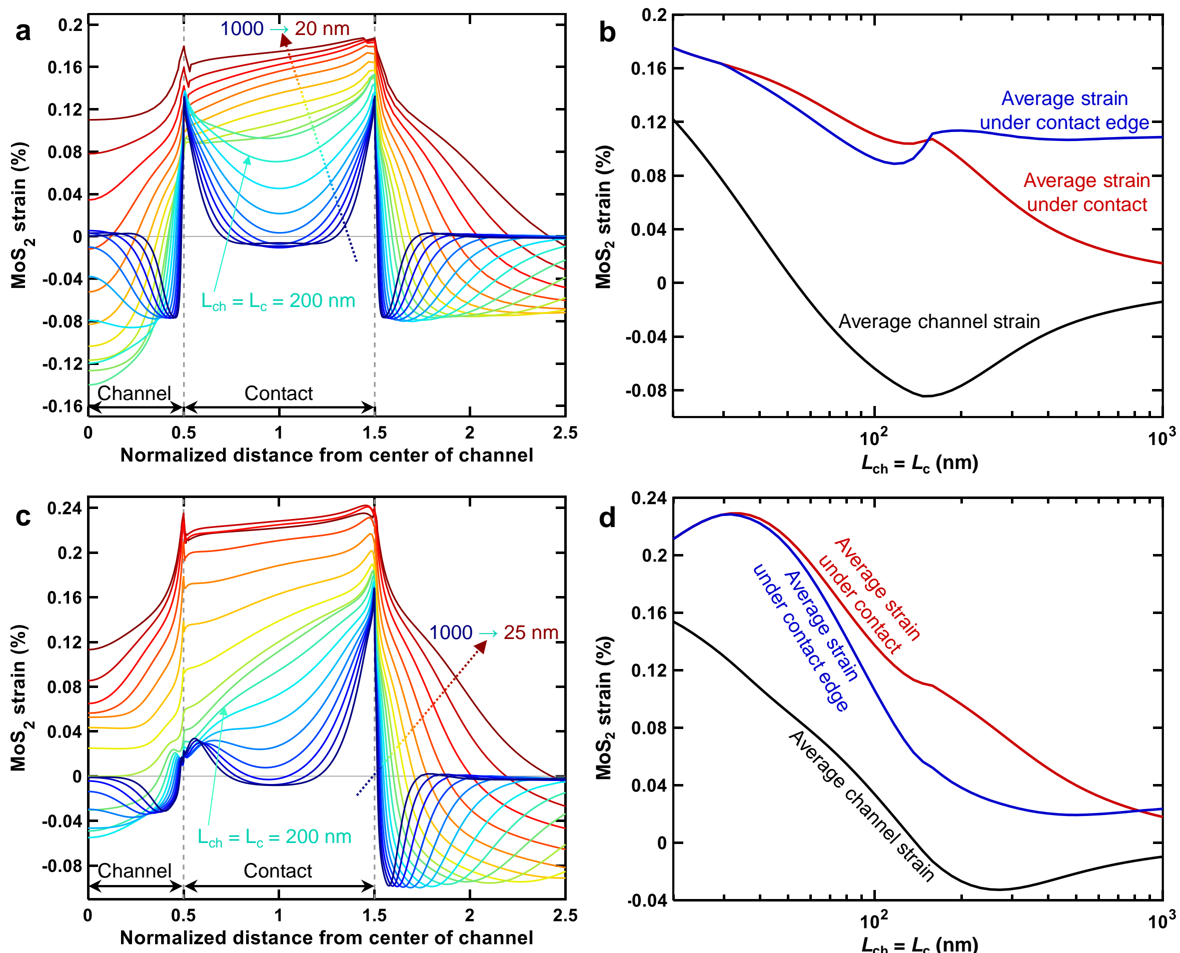
We note that all strain simulations in the subsequent sections assume a tensile-stressed SiN_x capping layer (600 MPa, as measured in our experiments) on top of either a DG or BG transistor geometry.

6. Strain Projections for Channel and Contact Scaling

We carried out additional simulations to study the impact of the SiN_x stressor on MoS_2 strain distributions in BG and DG transistors with different channel and contact lengths. Because our DG transistor geometry is similar to that of a typical top-gated (TG) transistor except for the conductive substrate, the corresponding conclusions apply equally well to TG devices (with no BG). The metrics we focus on are the average channel strain (in-plane, along the channel direction), average strain in MoS_2 under the contacts, and MoS_2 under the edge of the contact. The latter parameter is quantified as the average strain in the first 30 nm (or L_c, whichever is smaller) of MoS_2 under the contact, on the channel side. This parameter is relevant because the current under a contact is only distributed within about a few transfer lengths L_T of the contact edge, which is typically[10,11] on the order of tens of nanometers in good contacts with MoS_2.

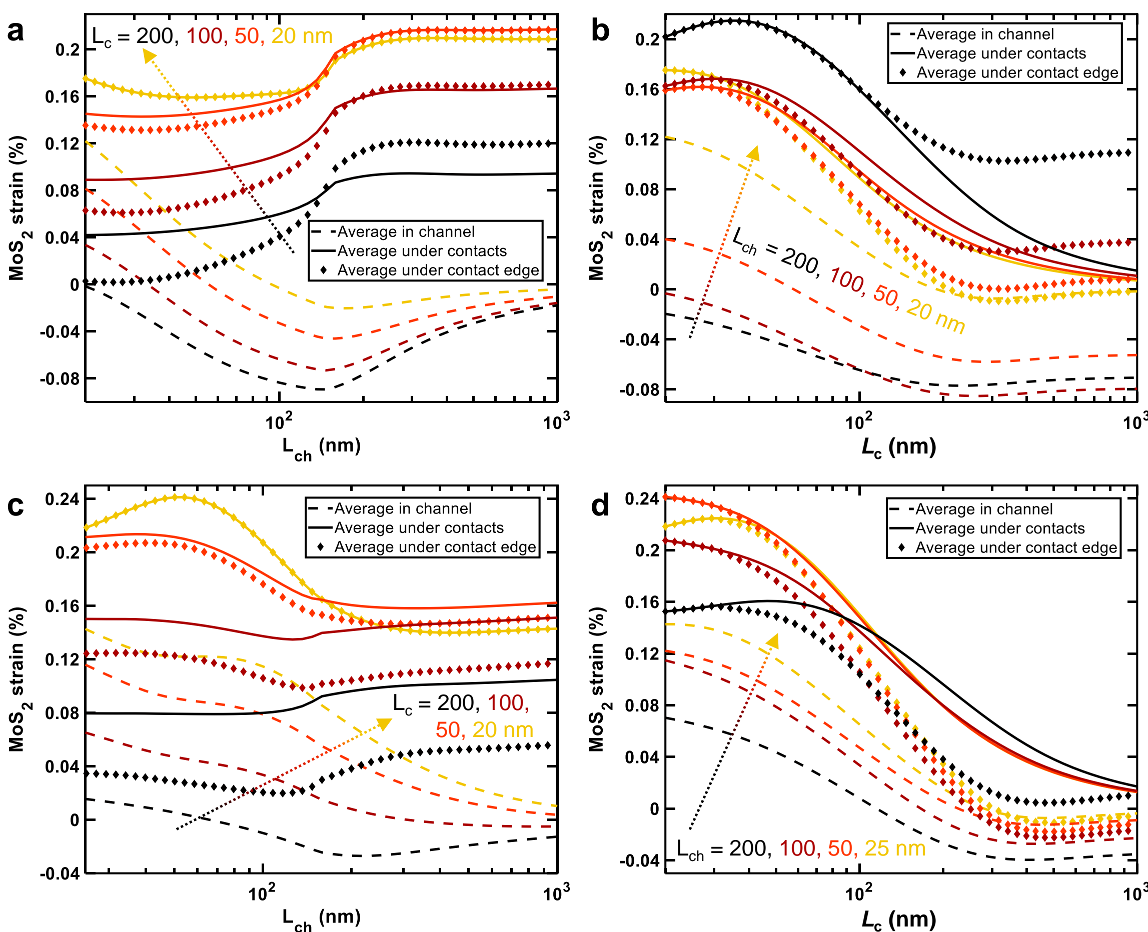
Supplementary Figure 6 shows the variation of the in-plane strain as a function of $L_{ch} = L_c$, for the BG (**Supplementary Figure 6a,b**) and DG (**Supplementary Figure 6c,d**) devices. **Supplementary Figure 6a** shows that in a BG transistor, the strain under contact is highest and approximately equal at the two edges. However, according to **Supplementary Figure 6c**, a DG transistor has lower strain under the "inner" contact edge than under the "outer" edge. This is because the nitride stressor only directly covers the outer side of the contacts in the DG device and not both sides like it does in the BG geometry. Consequently, as can be seen in **Supplementary Figure 6b,d**, the DG transistor has lower average tensile strain under the contacts for $L_{ch} > 100$ nm, but in shorter devices the DG transistor has higher tensile strain under the contacts as well as in the channel. Reducing the channel and contact lengths toward 20 nm in both BG and DG transistors increases the tensile strain under the contacts substantially, suggesting further improvements of contact resistance (with strain) are possible. Moreover, the tensile-strained channel at shorter channel lengths could lead to increased mobility[12,13], and thus, further performance enhancement. The kink seen in **Supplementary Figure 6b,d** at $L_{ch} = 160$ nm is the result of the fact that for $L_{ch} < 160$ nm, the curved sections of the nitride film above the channel, where it smoothly conforms around the edges of the contact (in the BG device) or the top gate (in the DG device), begin to merge.

We also varied L_{ch} and L_c separately to study their individual effects on the strain distribution in MoS_2, the results are given in **Supplementary Figure 7**. According to **Supplementary Figure 7a**, reducing L_{ch} below 160 nm in a BG transistor reduces the tensile strain under the contacts, especially for long contacts. This happens because in the limit of very short channels, the contacts effectively "merge",



Supplementary Figure 6 | Stress simulations and projections. a, The strain profiles along MoS_2 in a BG transistor (with 600 MPa tensile-stressed SiN_x capping), normalized by L_{ch}, for $L_{ch} = L_c$ varied from 1000 nm down to 20 nm (logarithmically spaced). **b,** The corresponding average in-plane strains along MoS_2 as a function of $L_{ch} = L_c$. **c,** The normalized strain profiles along MoS_2 in a DG transistor, for $L_{ch} = L_c$ varied from 1000 nm down to 25 nm (logarithmically spaced). **c,** Average in-plane strains in MoS_2 in a DG transistor, as a function of $L_{ch} = L_c$. **d,** The corresponding average in-plane strains along MoS_2 as a function of $L_{ch} = L_c$.

and the strain under the inner contact edge is lower for the same reason the strain in under the middle of the contact is lower than at the edges. Reducing L_{ch} also increases the channel strain significantly, turning it tensile for L_{ch} close to 20 nm. According to **Supplementary Figure 7b**, reducing L_c has a similar effect on the BG transistor channel strain, and also increases both the edge and average contact strains as it is reduced beyond 160 nm. **Supplementary Figure 7c** shows that in a DG transistor, reducing L_{ch} similarly increases the tensile channel strain, although its effect on contact strain is less



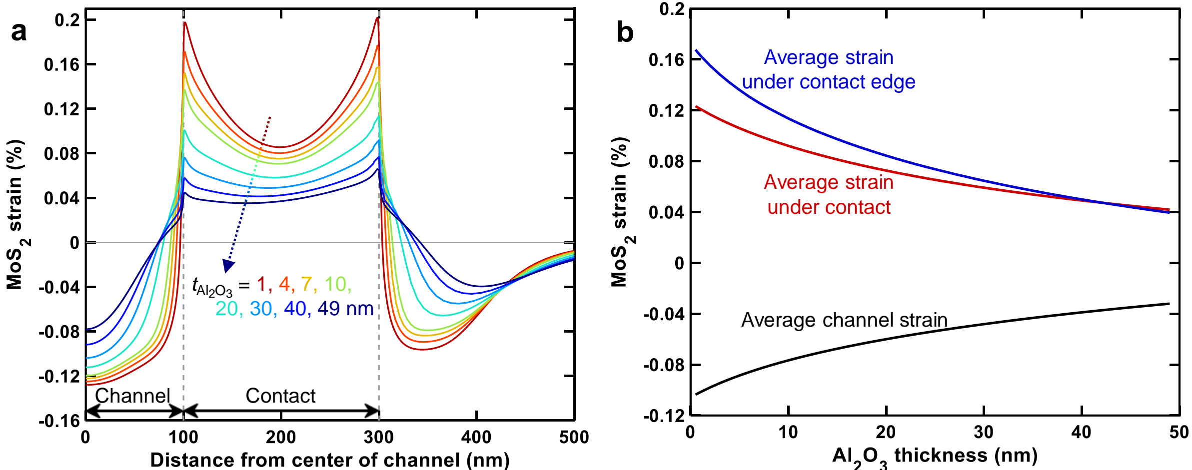
Supplementary Figure 7 | Strain projections for channel and contact scaling. Average in-plane strains in a back-gated (BG) MoS_2 transistor with a tensile-stressed SiN_x capping layer (600 MPa) when **a,** L_{ch} is varied with L_c fixed, and **b,** L_c is varied with L_{ch} fixed. Average in-plane strains in MoS_2 in a DG transistor when **c,** L_{ch} is varied with L_c fixed, and **d,** L_c is varied with L_{ch} fixed.

pronounced than in the BG case. Finally, a comparison of **Supplementary Figure 7d** to **Supplementary Figure 7b** reveals that the effect of reducing DG transistor contact lengths is similar to the BG transistor, increasing strain both in the channel and under contacts.

To summarize, in both BG and DG (or TG) transistors, shorter channels are expected to put tensile strain on the channel, while shorter contacts increase the tensile strain under the contacts as well as in the channel. Both of these effects are expected to increase performance in smaller devices, due to tensile strain under the contacts reducing contact resistance[14], and tensile strain in the channel increasing mobility[12,13].

7. Impact of Al_2O_3 Barrier Thickness on Strain Distribution

We have carried out simulations to understand the effect of the Al_2O_3 barrier layer thickness on the strain distribution in the BG transistor, presented in **Supplementary Figure 8**. It is seen that the MoS_2 strain in both the channel and the contact regions decrease steadily as Al_2O_3 is made thicker. As such, to further improve contact resistance via strain, there is possibility of enhancing the strain under contact edges by up to 50% by making the Al_2O_3 thinner than what we have used in this work (10 nm), or possibly even eliminating it.



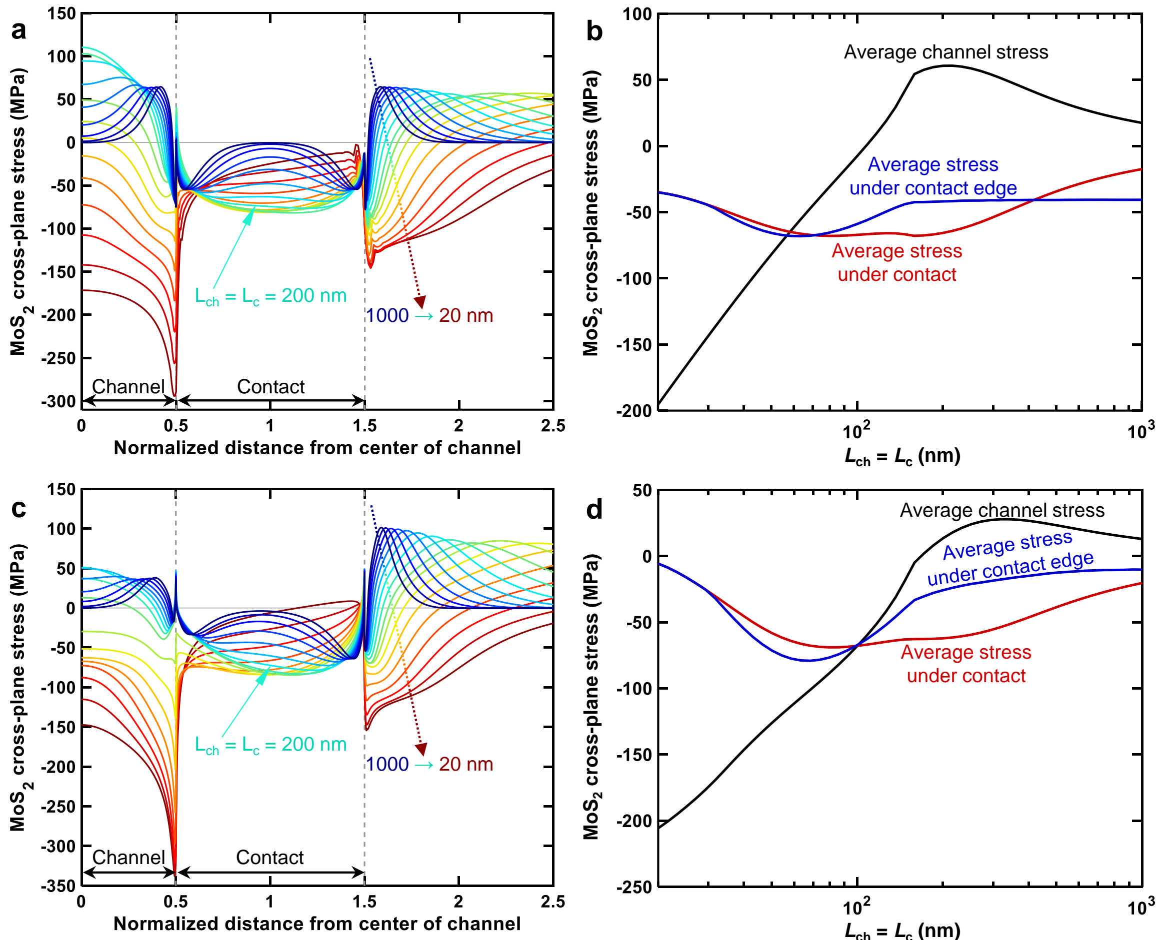
Supplementary Figure 8 | Dependence of strain profile on Al_2O_3 barrier layer thickness. a, In-plane strain distributions in a BG transistor with $L_{ch} = L_c = 200$ nm for several Al_2O_3 thicknesses ($t_{Al_2O_3}$). **b,** Average in-plane strains in MoS_2 in a BG transistor (with 600 MPa tensile-stressed SiN_x capping) as a function of Al_2O_3 thickness. The blue curve corresponds to the average strain in the first 30 nm of MoS_2 (a typical contact transfer length) under the contacts.

8. Cross-Plane Stress in MoS_2 due to "Downward Pressure" on Contacts

The tensile-stressed SiN_x capping layer pushes down on the contacts due to its tendency to contract, as visualized in **Figure 3a,b** of the main text, as well as **Supplementary Figure 4**, which may reduce the thickness of the van der Waals gap (an electron tunneling barrier) between the Au contacts and MoS_2. It is then possible that the vertical contact-MoS_2 pressure (i.e. the cross-plane MoS_2 stress) due to this effect (in addition to the in-plane tensile strain of MoS_2 under the contacts) contributes to the contact resistance improvement we observe in SiN_x-capped devices, as the reduction in MoS_2 contact resistance with applied pressure has been observed experimentally[15,16].

To better understand the role of the SiN_x in vertically compressing the contacts, we plot the cross-plane stress in BG (**Supplementary Figure 9a,b**) and DG (**Supplementary Figure 9c,d**) MoS_2 devices, as a function of $L_{ch} = L_c$ from 1000 nm down to ~20 nm. For both BG and DG devices, the compressive cross-plane stress at the contact is close to about 50 MPa for 50 nm $< L_{ch} = L_c <$ 200 nm. Based on measurements of Chen *et al.*[15] this would correspond to a contact resistance reduction of ~12%.

Another interesting feature observed in **Supplementary Figure 9b,d** is that while the vertical stress in the channel is moderately tensile for $L_{ch} = L_c >$ ~100 nm, scaling the devices down to $L_{ch} = L_c$ ~20 nm results in a sizable compressive vertical channel stress, up to ~200 MPa. In other words, the MoS_2 channel is "vertically squeezed" by the contacts at the shortest channel and contact dimensions (here ~20 nm). This vertical compression of MoS_2 has a similar effect on the conduction band structure as lateral tensile strain[17], i.e. lowering the K valley and raising the Q valley (thus expected to reduce intervalley scattering and improve mobility[12,13]), and has also been reported experimentally to improve in-plane conduction[15]. Therefore, the vertical compression of the MoS_2 channel could enable further enhancement of device performance at the smallest dimensions, in addition to the effect of in-plane tensile strain discussed in **Supplementary Information Section 6**.



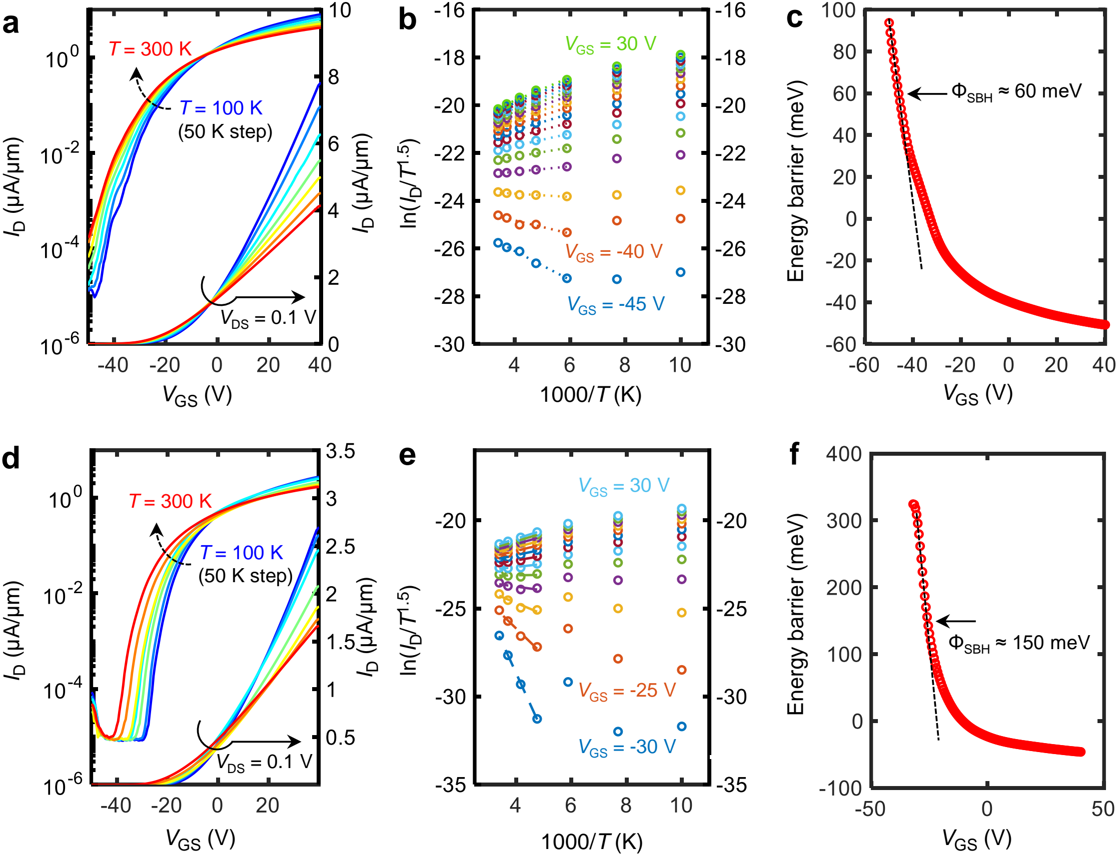
Supplementary Figure 9 | Cross-plane stress in MoS_2. a, Normalized cross-plane stress profiles along MoS_2 in back-gated (BG) transistors (with 600 MPa tensile-stressed SiN_x capping), normalized by L_{ch}, for $L_{ch} = L_c$ from 1000 nm down to 20 nm (logarithmically spaced). **b,** Corresponding average cross-plane stresses along BG MoS_2 as a function of $L_{ch} = L_c$. "Average stress under contact edge" refers to the cross-plane stress *averaged* along the first 30 nm of contact length (30 nm is a typical value of contact transfer length). **c,** Normalized cross-plane stress profiles along MoS_2 in dual-gated (DG) transistors, for $L_{ch} = L_c$ from 1000 nm down to 20 nm (logarithmically spaced). **d,** Corresponding average cross-plane stresses in MoS_2 in DG transistors, as a function of $L_{ch} = L_c$.

9. Schottky Barrier Height Measurement

To further investigate the behavior at the contacts, we estimate the Schottky barrier height (SBH) based on the thermionic emission current dictated by the equation:

$$I_D = A_{2D}^* T^{3/2} \exp\left(-\frac{q\Phi_{SBH}}{k_B T}\right)\left[1 - \exp\left(-\frac{qV}{k_B T}\right)\right],$$

where A_{2D}^* is the 2D-equivalent Richardson constant, T is the temperature, q is the elementary charge, k_B is Boltzmann's constant, V is the applied voltage, and Φ_{SBH} is the Schottky barrier height[18,19]. **Supplementary Figure 10a-c** shows the results of temperature-dependent measurements to extract the SBH of a strained device having L_{ch} = 1 μm and L_c = 200 nm at V_{DS} = 0.1 V, while Supplementary **Figure 10d-f** shows the results of measurements performed on an uncapped control sample with Au contacts having L_{ch} = 2 μm and L_c = 200 nm.



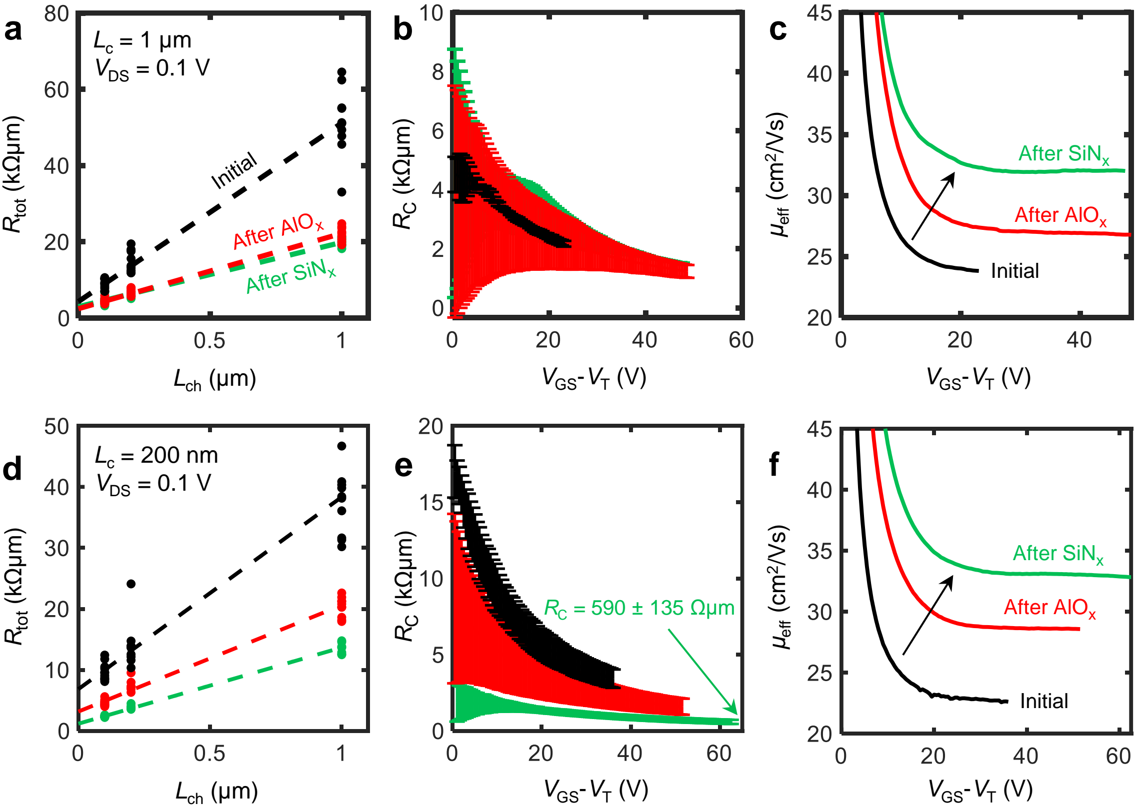
Supplementary Figure 10 | Schottky barrier height extraction. Measurements, **a-c,** (top row) of a high tensile-stress SiN_x-capped device and **d-f,** (bottom row) an uncapped control device with Au contacts. **a, d**, Temperature-dependent transfer characteristics measured between T = 100 and 300 K at V_{DS} = 0.1 V. **b, e**, Arrhenius plots measured at various gate voltages. **c, f**, Estimates of the effective electron Schottky barrier height.

Supplementary Figure 10a shows the device I_D-V_{GS} characteristics measured from T = 100 to 300 K. From this, the slope of the Arrhenius plot of $\ln(I_D/T^{3/2})$ vs $1000/T$ can be constructed at each value of V_{GS}, with the slope giving the effective barrier height at that particular bias as shown in **Supplementary Figure 10b**. Finally, the estimated energy barrier is plotted vs. V_{GS} in **Supplementary Figure 10c**, with the true value of Schottky barrier height (SBH) being determined as the effective barrier height at the flat band voltage indicated by the point above which the effective barrier height starts to deviate from a linear dependence of the gate voltage. We extract a SBH of ~60 meV for the stressed device. The results of SBH measurement on a control device (without SiN_x capping, but otherwise identical) are shown in **Supplementary Figure 10d-f**, indicating a barrier of ~ 150 meV.

10. Pseudo-Transfer Length Method Analysis

We estimate contact resistance (R_C) and effective electron mobility (μ_{eff}) using pseudo-transfer length method[20–22] (TLM) measurements. We call these "pseudo" TLM measurements, because we fit the median resistance (R_{tot}) vs. channel length (L_{ch}) for *all* devices we have, rather than choosing a single TLM structure[10] with shared contacts and a larger range of L_{ch}, fabricated in a single region of MoS_2.

Supplementary Figure 11a displays $R_{tot} = L_{ch}R_{sh} + 2R_C$ vs. L_{ch}, where R_{sh} is the channel sheet resistance, for devices with 'long' contacts (L_c = 1 μm) at various stages of capping. To account for threshold voltage (V_T) variation, we normalize all devices to the same maximum gate overdrive ($V_{ov} = V_{GS} - V_T$) using linear extrapolation to estimate V_T. The *y*-intercept of the linear fit allows us to extract $2R_C$, which is plotted vs. overdrive voltage in **Supplementary Figure 11b**. For devices with 'long' contacts, the extracted R_C remains similar at different stages of capping. This reflects the lower average stress across the devices with long contacts. Additionally, the slope of the fit allows us to estimate the



Supplementary Figure 11 | Pseudo-transfer length method (TLM) analysis. Comparison of high tensile-stress SiN_x-capped devices fabricated with (**a-c**) long, 1 μm and (**d-f**) short, 200 nm contacts. **a, d,** R_{tot} vs. L_{ch} at maximum gate overdrive ($V_{GS} - V_T$) for V_{DS} = 0.1 V, at different stages of capping. **b, e,** Extracted R_C vs. gate overdrive voltage. We observe reduced R_C after SiN_x capping only for the short contacts. **c, f,** Estimated effective mobility μ_{eff} vs. gate overdrive voltage.

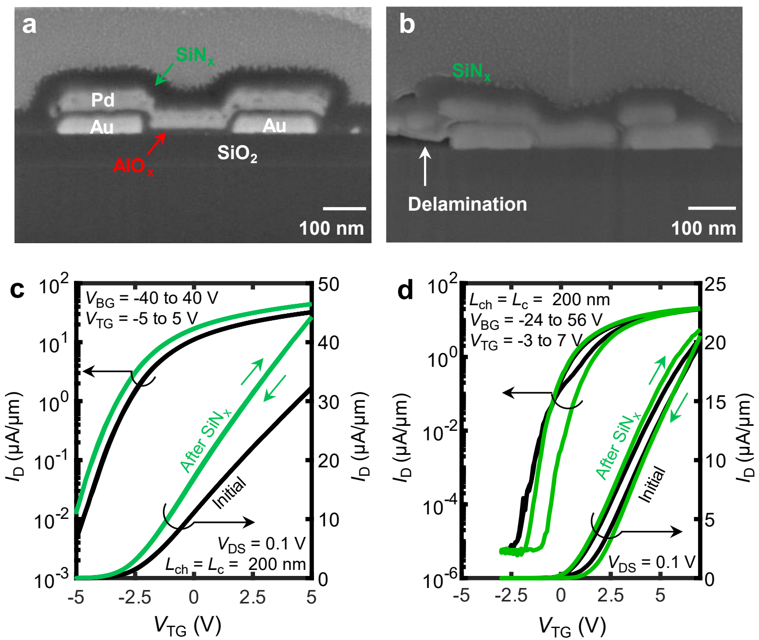
effective mobility, $\mu_{eff} = (qnR_{sh})^{-1}$ where q is the elementary charge and $n = C_{ox}(V_{GS} - V_T - V_{DS}/2)/q$ is the electron density per unit area[10]. Throughout this study, the back-gate oxide capacitance per unit area is $C_{ox} \approx 38$ nF/cm^2, corresponding to the 90 nm of SiO_2.

Supplementary Figure 11c shows the extracted μ_{eff} vs. overdrive voltage for devices with 'long' contacts, indicating a small improvement after SiN_x capping. We caution against relying too strongly on TLM mobility estimates, because the strain distribution (between the various channel lengths in the TLM) is non-uniform. In addition, we cannot be certain that the apparent mobility increase is entirely due to strain; other contributions could come from dielectric screening and the additional thermal annealing seen by the AlO_x/SiN_x capped samples. For these reasons we have put more emphasis on changes in transistor *current* density (I_D) in the main text. The current density (at a given voltage, e.g. 1 V) is also ultimately what most impacts the circuit performance of a transistor.

We repeat this analysis for devices with 'short' contacts (L_c = 200 nm) in **Supplementary Figure 11d**. After SiN_x capping, the extracted R_C is now significantly reduced to 590 ± 135 Ω·µm as shown in **Supplementary Figure 11e**, demonstrating that high-stress capping has a larger effect on the shorter contacts. The extracted mobility trend is similar in **Supplementary Figure 11f**, which is expected because the channel dimensions used are consistent with those in **Supplementary Figure 11a-c**.

11. Measurement of Transistors That Suffered Stress-Induced Delamination

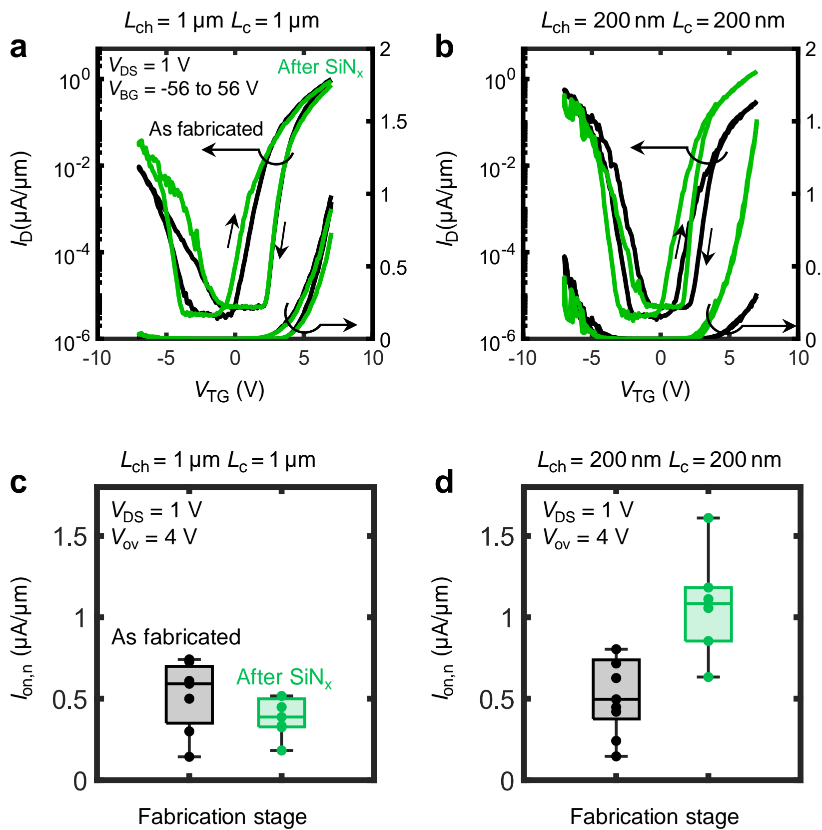
Here, we present additional evidence for strain-related improvements in our transistors by illustrating the effect of strain release/delamination. **Supplementary Figure 12a** shows a focused ion-beam scanning electron microscope (FIB-SEM) cross sectional image for one of our dual-gated 'short' (L_{ch} = L_c = 200 nm) devices, such as the one in main text Figure 3, where we see conformal coverage of SiN_x around the device. By comparison, **Supplementary Figure 12b** shows the cross-section of another 'short' device on a separate chip which experienced delamination after tensile SiN_x capping; this occurred because here we used MoS_2 grown at a lower temperature, which is more weakly adhered to the substrate[23]. **Supplementary Figure 12c** (same as main text Figure 4c) and **Figure 12d** compare the measured I_D vs. V_{GS} of a typical well-adhered 'short' transistor with that of a similar device which undergoes delamination, respectively. The former experiences 33% improvement in I_{on} after capping while the latter displays no observable improvement in I_{on}. This provides further confirmation that strain transfer is the main source of the improvements observed in our 'short' well-adhered devices.



Supplementary Figure 12 | FIB-SEM cross-sections of **(a)** typical well-adhered dual-gated MoS_2 transistor capped with tensile SiN_x and **(b)** a transistor on a separate chip which experienced stress release/delamination after SiN_x capping. These are 'short' devices with L_{ch} = L_c = 200 nm. Measured transfer characteristics for **(c)** a typical well-adhered 'short' transistor and **(d)** a similar transistor which experienced stress release. We observe no visible improvement in the on-state current when stress release occurs, indicating that strain (rather than encapsulation or annealing) is the source of improvement in our well-adhered devices. All measurements are at room temperature and V_{DS} = 0.1 V.

12. Strained Dual-Gated WSe_2 Transistors

Monolayer WSe_2 is another 2D semiconductor which is predicted to benefit from the application of uniaxial tensile strain. To further verify the effectiveness of our strain technique, we fabricated dual-gated (DG) transistors using CVD-grown monolayer WSe_2 using the approach described in the main text, with the only process difference being the use of 10 nm HfO_x deposited by atomic layer deposition at 200 °C serving as the top gate dielectric, instead of 10 nm AlO_x. The I_D-V_{GS} of DG WSe_2 transistors measured before and after capping with high tensile-stressed SiN_x are shown for 'long' (L_{ch} = L_c = 1 µm) and 'short' (L_{ch} = L_c = 200 nm) devices in **Supplementary Figure 13a,b**, respectively.



Supplementary Figure 13 | Strained DG WSe_2 transistors. Dual-gated transfer characteristics of high-stress SiN_x-capped WSe_2 transistor with **a**, 'long' (L_{ch} = L_c = 1 µm) and **b**, 'short' (L_{ch} = L_c = 200 nm) dimensions. Small arrows mark forward and backward sweeps. Relative improvement in *n*-branch I_{on} at fixed overdrive after capping with high-stress SiN_x films (green) for **c**, 'long' (7 devices) and **d**, 'short' geometries (8 devices). The middle line in each box plot marks the median value, whereas the upper and lower ranges indicate the upper and lower quartiles. The upper and lower ends of the whiskers represent the nonoutlier maximum and minimum values, respectively. Devices within each box plot are unique, with the same devices being retested after each fabrication step. All measurements are carried out at room temperature and V_{DS} = 1 V.

We compare the *n*-branch I_{on} (at fixed $V_{ov} = V_{TG} - V_T > 0$) of each case in **Supplementary Figure 13c,d**. Similar to the trends observed in the case of monolayer MoS_2 (main text **Figure 4c,e**), the larger improvement of I_{on} is observed for the devices with the shortest channel and contact lengths.

Supplementary References

(1) Michail, A.; Delikoukos, N.; Parthenios, J.; Galiotis, C.; Papagelis, K. Optical Detection of Strain and Doping Inhomogeneities in Single Layer MoS_2. *Appl Phys Lett* **2016**, *108*, 173102.

(2) Schauble, K.; Zakhidov, D.; Yalon, E.; Deshmukh, S.; Grady, R. W.; Cooley, K. A.; McClellan, C. J.; Vaziri, S.; Passarello, D.; Mohney, S. E.; Toney, M. F.; Sood, A. K.; Salleo, A.; Pop, E. Uncovering the Effects of Metal Contacts on Monolayer MoS_2. *ACS Nano* **2020**, *14*, 14798–14808.

(3) Peña, T.; Chowdhury, S. A.; Azizimanesh, A.; Sewaket, A.; Askari, H.; Wu, S. M. Strain Engineering 2D MoS_2 with Thin Film Stress Capping Layers. *2D Mater* **2021**, *8*, 045001.

(4) Reboh, S.; Morin, P.; Hÿtch, M. J.; Houdellier, F.; Claverie, A. Mechanics of Silicon Nitride Thin-Film Stressors on a Transistor-like Geometry. *APL Mater* **2013**, *1*, 042117.

(5) Hüe, F.; Hÿtch, M.; Bender, H.; Houdellier, F.; Claverie, A. Direct Mapping of Strain in a Strained Silicon Transistor by High-Resolution Electron Microscopy. *Phys Rev Lett* **2008**, *100*, 156602.

(6) Li, Y.; Yu, C.; Gan, Y.; Jiang, P.; Yu, J.; Ou, Y.; Zou, D.-F.; Huang, C.; Wang, J.; Jia, T.; Luo, Q.; Yu, X.-F.; Zhao, H.; Gao, C.-F.; Li, J. Mapping the Elastic Properties of Two-Dimensional MoS_2 via Bimodal Atomic Force Microscopy and Finite Element Simulation. *npj Comput Mater* **2018**, *4*, 49.

(7) Amani, M.; Chin, M. L.; Mazzoni, A. L.; Burke, R. A.; Najmaei, S.; Ajayan, P. M.; Lou, J.; Dubey, M. Growth-Substrate Induced Performance Degradation in Chemically Synthesized Monolayer MoS_2 Field Effect Transistors. *Appl Phys Lett* **2014**, *104*, 203506.

(8) Kataria, S.; Wagner, S.; Cusati, T.; Fortunelli, A.; Iannaccone, G.; Pandey, H.; Fiori, G.; Lemme, M. C. Growth-Induced Strain in Chemical Vapor Deposited Monolayer MoS_2: Experimental and Theoretical Investigation. *Adv Mater Interfaces* **2017**, *4*, 1700031.

(9) Luo, S.; Cullen, C. P.; Guo, G.; Zhong, J.; Duesberg, G. S. Investigation of Growth-Induced Strain in Monolayer MoS_2 Grown by Chemical Vapor Deposition. *Appl Surf Sci* **2020**, *508*, 145126.

(10) English, C. D.; Shine, G.; Dorgan, V. E.; Saraswat, K. C.; Pop, E. Improved Contacts to MoS_2 Transistors by Ultra-High Vacuum Metal Deposition. *Nano Lett* **2016**, *16*, 3824–3830.

(11) Schranghamer, T. F.; Sakib, N. U.; Sadaf, M. U. K.; Subbulakshmi Radhakrishnan, S.; Pendurthi, R.; Agyapong, A. D.; Stepanoff, S. P.; Torsi, R.; Chen, C.; Redwing, J. M.; Robinson, J. A.; Wolfe, D. E.; Mohney, S. E.; Das, S. Ultrascaled Contacts to Monolayer MoS_2 Field Effect Transistors. *Nano Lett* **2023**, *23*, 3426–3434.

(12) Datye, I. M.; Daus, A.; Grady, R. W.; Brenner, K.; Vaziri, S.; Pop, E. Strain-Enhanced Mobility of Monolayer MoS_2. *Nano Lett* **2022**, *22*, 8052–8059.

(13) Hosseini, M.; Elahi, M.; Pourfath, M.; Esseni, D. Strain Induced Mobility Modulation in Single-Layer MoS_2. *J Phys D Appl Phys* **2015**, *48*, 375104.

(14) John, A. P.; Thenapparambil, A.; Thalakulam, M. Strain-Engineering the Schottky Barrier and Electrical Transport on MoS_2. *Nanotechnology* **2020**, *31*, 275703.

(15) Chen, Y.; Ke, F.; Ci, P.; Ko, C.; Park, T.; Saremi, S.; Liu, H.; Lee, Y.; Suh, J.; Martin, L. W.; Ager, J. W.; Chen, B.; Wu, J. Pressurizing Field-Effect Transistors of Few-Layer MoS_2 in a Diamond Anvil Cell. *Nano Lett* **2017**, *17*, 194–199.

(16) Manzanares-Negro, Y.; Quan, J.; Rassekh, M.; Moaied, M.; Li, X.; Ares, P.; Palacios, J. J.; Gomez-Herrero, J.; Gomez-Navarro, C. Low Resistance Electrical Contacts to Few-Layered MoS_2 by Local Pressurization. *2D Mater* **2023**, *10*, 021003.

(17) Sohier, T.; Ponomarev, E.; Gibertini, M.; Berger, H.; Marzari, N.; Ubrig, N.; Morpurgo, A. F. Enhanced Electron-Phonon Interaction in Multivalley Materials. *Phys Rev X* **2019**, *9*, 031019.

(18) Shen, P.-C.; Su, C.; Lin, Y.; Chou, A. S.; Cheng, C. C.; Park, J. H.; Chiu, M. H.; Lu, A. Y.; Tang, H. L.; Tavakoli, M. M.; Pitner, G.; Ji, X.; Cai, Z.; Mao, N.; Wang, J.; Tung, V.; Li, J.; Bokor, J.; Zettl, A.; Wu, C. I.; Palacios, T.; Li, L. J.; Kong, J. Ultralow Contact Resistance between Semimetal and Monolayer Semiconductors. *Nature* **2021**, *593*, 211–217.

(19) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS_2 Transistors with Scandium Contacts. *Nano Lett* **2013**, *13*, 100–105.

(20) Schroder, D. K. *Semiconductor Material and Device Characterization*, 3rd ed.; John Wiley & Sons, Inc., 2006.

(21) Smithe, K. K. H.; Suryavanshi, S. V.; Muñoz Rojo, M.; Tedjarati, A. D.; Pop, E. Low Variability in Synthetic Monolayer MoS_2 Devices. *ACS Nano* **2017**, *11*, 8456–8463.

(22) Dorow, C.; O'Brien, K.; Naylor, C. H.; Lee, S.; Penumatcha, A.; Hsiao, A.; Tronic, T.; Christenson, M.; Maxey, K.; Zhu, H.; Oni, A.; Alaan, U.; Gosavi, T.; Gupta, A. Sen; Bristol, R.; Clendenning, S.; Metz, M.; Avci, U. Advancing Monolayer 2-D NMOS and PMOS Transistor Integration from Growth to Van Der Waals Interface Engineering for Ultimate CMOS Scaling. *IEEE Trans Electron Devices* **2021**, *68*, 6592–6598.

(23) Tang, A.; Kumar, A.; Jaikissoon, M.; Saraswat, K.; Wong, H.-S. P.; Pop, E. Toward Low-Temperature Solid-Source Synthesis of Monolayer MoS_2. *ACS Appl Mater Interfaces* **2021**, *13*, 41866–41874.