Two-Fold Reduction of Switching Current Density in Phase Change Memory Using Bi$_2$Te$_3$ Thermoelectric Interfacial Layer

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Abstract—High switching current density has been a key bottleneck for phase change memory (PCM) technology. Here, we demonstrate interfacial thermoelectric heating (TEH) as a promising way of tackling this challenge. We use TEH induced by a thin Bi$_2$Te$_3$ interfacial layer to demonstrate ~2x reduction of reset current density ($J_{\text{reset}}$) and power ($P_{\text{reset}}$) compared to control PCM devices based on Ge$_2$Sb$_2$Te$_5$ (GST). Measurements of polarity-dependent reset current and power in well-cycled devices reveal the strong TEH caused by the Bi$_2$Te$_3$ interfacial layer. The TEH origin of $J_{\text{reset}}$ reduction is further confirmed by electrothermal simulations. Such TEH-engineered PCM devices are scalable with the bottom electrode diameter and thus could be promising for high density data storage applications.

Index Terms—Phase change memory, interfacial thermoelectric engineering, reset current density reduction.

I. INTRODUCTION

Phase change memory has shown promise for storage-class applications due to its fast switching speed, good resistance window, and scalability [1], [2]. PCM also offers nonvolatility and longer write endurance than flash memory [1], [2]. However, concerns remain over its relatively high reset current density ($J_{\text{reset}}$) and power ($P_{\text{reset}}$), both for data storage and emerging applications such as neuromorphic computing [1]–[3]. In addition, the reset current ($I_{\text{reset}}$) of PCM must be provided by selector devices in a memory array. As a result, the selectors need to have larger area, limiting storage density [1], [4]. Hence, reduction of $J_{\text{reset}}$ is essential for high density data storage [2], [5]. In a PCM cell, data are encoded as the resistance change of a phase change material (like Ge$_2$Sb$_2$Te$_5$, or GST) contacted by a top and bottom electrode (BE). Resistive heating induced by the BE can reversibly transform the GST between amorphous (high-resistance) and crystalline (low-resistance) states. Reducing the BE diameter reduces $I_{\text{reset}}$, but $J_{\text{reset}}$ does not decrease unless the heating efficiency is improved [2], [4], [6].

Heating efficiency could be improved with better thermal insulation of the PCM cell [7], [8], or by improving the heating process itself. Commonly, the latter only relies on Joule heating, however thermoelectric heating (TEH) could also be introduced, especially because GST itself has a non-negligible, positive Seebeck coefficient ($S_p$) [9], [10]. Hence, utilization and enhancement of this TEH effect can decrease the requirement of large $J_{\text{reset}}$ in PCM [10]. Several previous studies have modeled and characterized TEH in GST [10]–[12]. Also, by using a polysilicon BE instead of a TiN BE, a moderate ~25% reduction of $I_{\text{reset}}$ has been experimentally demonstrated due to TEH [13], further inspiring such work.

Here we show a ~2x reduction of $J_{\text{reset}}$ in mushroom-cell PCM with TEH induced by a thin Bi$_2$Te$_3$ interfacial layer at the BE interface. Bi$_2$Te$_3$ is a thermoelectric material with significant but negative $S_p$ [14]–[16], which amplifies the TEH effect at the Bi$_2$Te$_3$/GST interface due to the difference in their Seebeck coefficients, thus improving the overall heating efficiency. Polarity-dependent experiments and simulations further confirm the TEH effect arising from interfacial engineering to reduce $J_{\text{reset}}$ and $P_{\text{reset}}$ at similar voltage, while maintaining scalability with the BE diameter.

II. DEVICE FABRICATION AND MEASUREMENT

Figs. 1(a,b) show the schematic and the cross-sectional scanning electron microscope (SEM) images of our Bi$_2$Te$_3$/GST PCM devices with ~4 nm Bi$_2$Te$_3$ and ~50 nm GST thickness, here on a ~150 nm diameter TiN BE. Before sputter depositing ~4 nm polycrystalline Bi$_2$Te$_3$ at room temperature (RT), we clean the BE surface in situ with Ar ions to remove native TiO$_x$ [8], then anneal at 180°C for 30 minutes. We subsequently sputter 50 nm GST and then ~10 nm TiN capping layer at RT, all without breaking vacuum. Next, we pattern and dry etch the device region followed by the fabrication of top electrode (TiN/Pl) using sputtering. For set and reset programming, we use 1/200 ns and 1/20/1 ns rise/width/fall pulses, respectively.
and measurement details were further described in [8]. Unless stated otherwise, all measurements reported here were done after cycling the devices 3000 times to ensure reliable and consistent operation.

III. RESULTS AND DISCUSSION

Fig. 1(c) displays resistance ($R$) vs. current ($I$) for multiple devices with $\sim 150$ nm BE diameter, showing $\sim 2 \times$ lower $I_{\text{reset}}$ for Bi$_2$Te$_3$/GST vs. control GST devices. Fig. 1(d) shows $I_{\text{reset}}$ of our devices scales with the BE diameter (here from $\sim 100$ to $\sim 300$ nm), demonstrating the scalability [4] of this technology.

Examining the reset current density in Fig. 2(a) reveals that $J_{\text{reset}}$ for our mushroom-type Bi$_2$Te$_3$/GST is $\sim 10$ MA/cm$^2$, half that of a control GST device ($\sim 20$ MA/cm$^2$), typical for GST in this configuration [4], [8]. Figs. 2(b,c) show Bi$_2$Te$_3$/GST devices switch at similar voltage and thus $\sim 2 \times$ lower $P_{\text{reset}}$ compared to GST control devices. Fig. 2(d) reveals that Bi$_2$Te$_3$/GST devices can maintain $\geq 10^5$ cycles. Fig. 2(e) shows the stability of the Bi$_2$Te$_3$/GST devices, as the $\sim 2 \times$ reduction in $I_{\text{reset}}$ is maintained even after $10^4$ switching cycles. We also find $\sim 40\%$ less resistance drift ($\nu$ = resistance drift coefficient) compared to control GST PCM devices [Fig. 2(f)], thereby projecting larger retention in the Bi$_2$Te$_3$/GST devices.

Next, we perform polarity dependent measurements (NP = normal polarity, RP = reverse polarity) with Bi$_2$Te$_3$/GST and control GST devices, as shown in Figs. 3(a,b). While Joule heating is always positive, the thermoelectric effect is expected to switch sign when the current direction is reversed i.e. from TEH in NP to cooling in RP [10]. As shown in Fig. 3(c), Bi$_2$Te$_3$/GST devices require $\sim 2 \times$ lower $I_{\text{reset}}$ in NP vs. RP operation, a direct consequence of the thermoelectric effect at the Bi$_2$Te$_3$ ($n$-type) to GST ($p$-type) interface. Crystalline GST has $S_n > 0$ ($\approx 40$ to $100$ $\mu$V/K from RT to $200^\circ$C) [9], [10], [13], whereas Bi$_2$Te$_3$ films have large $S_n < 0$ ($\approx -200$ $\mu$V/K to $-150$ $\mu$V/K from RT to $200^\circ$C) [15]. The sign of the Seebeck coefficient indicates if the charge current flows in the same or opposite direction as the heat carried by holes or electrons, respectively. In addition, it is the difference in Seebeck coefficient ($\Delta S = S_p - S_n$) which drives an interfacial thermoelectric heating or cooling effect [10], [17]. $|S_n|$ is expected to increase for thinner layers like Bi$_2$Te$_3$ ($\sim 4$ nm here) [18] due to carrier confinement [16], [19], further enhancing $\Delta S$ at the interface.

In contrast, control GST devices in Fig. 3(d) display only small intrinsic asymmetry with respect to the current flow direction [10], confirming the much larger TEH introduced by the thin Bi$_2$Te$_3$ layer in Bi$_2$Te$_3$/GST devices. At the same time, we note that the Bi$_2$Te$_3$ layer only introduces $\sim 13\%$
additional thermal resistance in the PCM stack, as shown by separate thermal [20] measurements on similar blanket films (Dataport Fig. S1 at DOI: 10.21227/wq7q-bx17). In other words, the small additional thermal resistance alone cannot be responsible for the \( \sim 2 \times \) change in \( J_{\text{reset}} \), instead pointing to the key role of TEH at the Bi\(_2\)Te\(_3\)/GST interface.

To gain deeper insight, we perform finite element electrothermal simulations of the device structures from Figs. 3(a,b), including both Joule heating and thermoelectric phenomena. This approach solves the heat equation self-consistently with the current flow [10], taking advantage of the cylindrical symmetry of the PCM device (Fig. 4). The Seebeck heating or cooling is \( \nabla T \Delta S \) at the junction of two materials, e.g. between GST and Bi\(_2\)Te\(_3\), between Bi\(_2\)Te\(_3\) and TiN, or between GST and TiN. These simulations also include the \( T \)-dependent thermal conductivity, resistivity, and \( S \) of GST [12], [13], [21], [22], \( T \)-dependent \( S \) of Bi\(_2\)Te\(_3\) [15] and of TiN [12], \( T \) dependent thermal conductivity and electrical resistivity of TiN and Bi\(_2\)Te\(_3\) [23]–[25] as well as the measured thermal and thermal boundary resistances at the appropriate interfaces.

Fig. 4 shows the temperature profiles computed in the Bi\(_2\)Te\(_3\)/GST and GST PCM at the end of a reset pulse (2 mA, 20 ns) for both NP and RP. In NP operation, the Seebeck effect generates additional TEH, due to the positive \( \Delta S \) between GST and Bi\(_2\)Te\(_3\). This helps the GST reach the melting temperature at lower \( J_{\text{reset}} \). TEH causes a significantly altered thermal path for low-power high-density PCM data storage.

IV. Conclusion

We introduced a novel, thermoelectrically-enhanced PCM with a thin Bi\(_2\)Te\(_3\) interfacial layer in an otherwise common mushroom-cell configuration. Such devices achieve \( \sim 2 \times \) reduction in reset current density due to the additional thermoelectric heating caused by the Bi\(_2\)Te\(_3\) layer. Devices display scalability with BE diameter, and could be combined with other PCM options (e.g. structural or thermal confinement) to further reduce the reset current density. These results should inspire further studies of thermoelectric heating as a novel pathway for low-power high-density PCM data storage.