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Sub-Nanometer Equivalent Oxide Thickness and Threshold Voltage Control Enabled by Silicon Seed Layer on Monolayer MoS_2 Transistors

Jung-Soo Ko, Sol Lee, Robert K. A. Bennett, Kirstin Schauble, Marc Jaikissoon, Kathryn Neilson, Anh Tuan Hoang, Andrew J. Mannix, Kwanpyo Kim, Krishna C. Saraswat, and Eric Pop*

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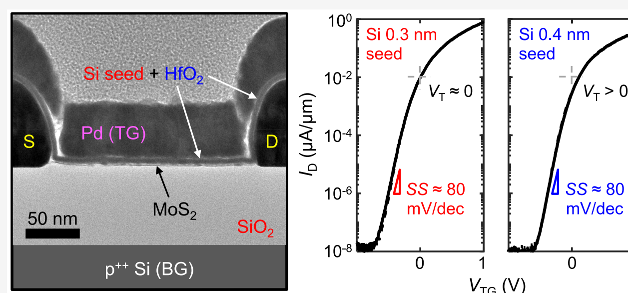
ABSTRACT: Low-power transistors based on two-dimensional (2D) semiconductors require ultrathin gate insulators, whose atomic layer deposition (ALD) has been difficult without adequate surface preparation. Here, we achieve sub-1 nm equivalent oxide thickness (EOT) on monolayer MoS_2 using HfO_2 and a simple, commonly available Si seed. We first investigate six seed layer candidates (Si, Ge, Hf, La, Gd, Al_2O_3) and find that only Si and Ge cause no measurable damage to the MoS_2. With these, we build monolayer MoS_2 transistors using ALD of HfO_2 top-gate dielectric and find that the Si seed provides the better, low-hysteresis interface. The thickness of this interfacial layer also controls the threshold voltage, enabling normally-off, well-behaved transistors. The thinnest gate stack reached low EOT ≈ 0.9 nm with low leakage (<0.6 μA/cm^2) and ~80 mV/dec subthreshold swing at room temperature. This represents a simple top-gate dielectric deposition approach, achievable within many common nanofabrication facilities.



KEYWORDS: *2D materials, transistors, equivalent oxide thickness, gate stack, threshold voltage*

Two-dimensional (2D) semiconducting transition metal dichalcogenides (TMDs) are of growing interest for integration with mainstream manufacturing of nanoscale electronics. For instance, monolayer MoS_2, a common TMD and 2D semiconductor, maintains good mobility at monolayer thickness,[1] enables transistors with on/off current ratio[2] > 10^{10}, and can be grown at relatively low temperatures[3,4] (<560 °C) compatible with back-end-of-line (BEOL) integration.[5] However, low-power operation requires low-voltage transistors with ultrathin gate dielectrics, but these have been difficult to achieve by atomic layer deposition (ALD) on 2D TMDs, which tend to lack the partially filled surface dangling bonds needed for ALD nucleation.[6] Gate insulators must be as thin as possible, with an effective oxide thickness (EOT) below 1 nm, while limiting gate leakage current density below 10^{-2} A/cm^2 for low-power applications.[7] Here, EOT refers to the thickness of SiO_2 which would give the same capacitance as the actual gate insulator being used.[8] (Concretely, an EOT of 1 nm corresponds to a capacitance of 3.45 μF/cm^2.)

In addition, top-gate, dual-gate or gate-all-around transistors[9,10] are preferred to limit short-channel effects, improving device and circuit performance. To overcome the ALD "adhesion" problem on TMD transistor channels, a common approach to form the top-gate insulator is to add a thin seed layer onto the 2D material, providing nucleation sites for the subsequent ALD of an ultrathin high-κ dielectric.[11−24] For example, a thin Al seed layer evaporated onto MoS_2 can assist the nucleation of ALD Al_2O_3, ostensibly without damaging the monolayer TMD[13,19] but potentially introducing some trapped charges and doping.[15,20] Other seed layers have included Hf,[17] Er,[22] Sb,[23] Ta,[24] or even organic molecules,[12,16] with various trade-offs between dielectric performance (e.g., EOT and leakage), defects, hysteresis, or (lack of) semiconductor industry compatibility.

In this work, we investigate multiple seed layer candidates: Si, Ge, Hf, La, Gd and Al_2O_3, on monolayer MoS_2, aiming to achieve top-gated transistors with ultrathin EOT and controllable threshold voltage. Such a seed layer should also, ideally, be easy to deposit in typical cleanroom facilities, be compatible with complementary metal-oxide semiconductor (CMOS) processing, and introduce minimal defects and charge traps. We study the seed layer effects on monolayer MoS_2 by Raman spectroscopy and X-ray photoelectron spectroscopy (XPS), finding that most of them either damage the MoS_2 or

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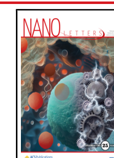

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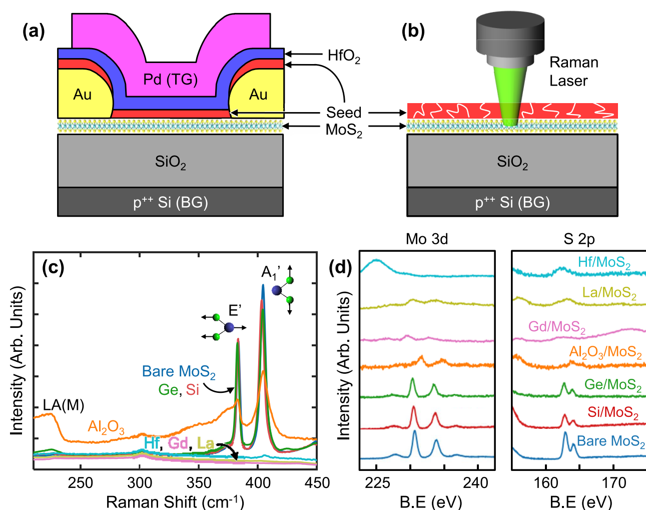

Figure 1. (a) Cross-section schematic of dual-gated monolayer MoS_2 transistor, not to scale. Evaporated seed layer (red) does not deposit on the source and drain contact sidewalls because the deposition is directional. The top gate (TG) has ≥200 nm overlap with the contacts. BG is the back gate. (b) Cross-section of samples for Raman spectroscopy and XPS, employing the same seed layer deposition as the transistors. Due to the surface energy difference, evaporated materials may form small clusters on the MoS_2. Here, ~2 nm of seed layers (Si, Ge, Hf, La, Gd, Al_2O_3) were deposited by e-beam evaporation on monolayer MoS_2 grown on SiO_2/Si substrates. (c) Raman spectroscopy (532 nm laser) and (d) XPS on the same ~2 nm evaporated seed layers on monolayer MoS_2 on SiO_2/Si substrates. Raman spectra are normalized to the Si substrate peak at 520 cm^{-1}. XPS spectra show Mo 3d and S 2p peaks vs binding energy (B.E.), including control data on bare monolayer MoS_2.

introduce transistor hysteresis. Ultimately, the Si seed (which oxidizes to SiO_x) provides the most reliable interfacial layer for uniform ALD of HfO_2 on MoS_2, also enabling partial top-gate threshold voltage control, which has been difficult to achieve in the past. Our well-behaved top-gated MoS_2 transistors have EOT <1 nm and gate leakage <0.6 μA/cm^2, with a simple process that can be readily adopted in many common cleanroom facilities.

Figure 1a shows the cross-section schematic of a monolayer MoS_2 transistor, and Figure 1b shows the cross-section for Raman spectroscopy and XPS studies. Monolayer MoS_2 is grown by chemical vapor deposition (CVD) on thermally oxidized SiO_2 (90 nm) on Si (p^{++} doped) substrates.[25] The transistor schematic shown in Figure 1a is dual-gated, with the doped Si substrate used as a global back gate (BG). The seed layers studied in this work are Si, Ge, Hf, La, Gd, and Al_2O_3, all e-beam evaporated onto monolayer MoS_2 under high vacuum (~10^{-7} Torr). To complete the transistor top gate (TG) stack, HfO_2 is then deposited by ALD at 200 °C using tetrakis-(dimethylamido)hafnium and water, and Pd as the top-gate metal. Additional details of the fabrication flow are provided in Section 1 and Figure S1 in the Supporting Information. As illustrated in Figure 1a, the top gate is partly overlapped with the source and drain (Au) contacts, to reduce access resistance and simplify our later analysis. This overlap length is ≥200 nm and the contact length is ≥1 μm. Devices with a top gate are measured at room temperature after annealing at 150 °C for 2 h in vacuum (~10^{-4} Torr).

Figure 1c shows Raman spectra of MoS_2 samples with evaporated seed layers and Figure 1d shows XPS data on the same samples. (Figure S2 in the Supporting Information shows the same Raman data including the Si substrate peak and additional XPS data of the Si seed on MoS_2.) After Hf, Gd, or La evaporation, the E' and A_1' peaks of monolayer MoS_2 are no longer visible, indicating these metals react with or destroy the MoS_2. This is also corroborated by our XPS data, which show broadening of S 2p spectra, evidence of metal-sulfide formation.[26] (Interestingly, there is some evidence[17,19] that a Hf seed layer *could* work on monolayer TMDs, potentially due to different evaporator conditions, e.g. higher base pressure. In other words, the more reactive seeds, like Hf, Gd and La, may work but require carefully optimized deposition to prevent damage to the monolayer TMDs.) For our Al_2O_3 seed evaporation, we observe the defect-related LA(M) peak[27] suggesting the MoS_2 is partially damaged during this process. Among the seed layers tested here, only Si and Ge preserve the E' and A_1' peaks of monolayer MoS_2, without any broadening or other spectroscopic evidence of MoS_2 damage. This could be explained by the lower melting point of Si or Ge (compared to Al_2O_3) and their weak enthalpies of formation with sulfur, unlike other seed layers tested in this work (Table S1 in the Supporting Information), as Si or Ge oxidize and are not expected to react with sulfur from MoS_2.

Based on the evidence above, we turn our focus to Si and Ge seed layers, which are the most benign among all options tested here on monolayer MoS_2. Atomic force microscopy reveals that a ~ 1 nm Si seed layer has nearly the same surface roughness as the underlying MoS_2, but a similar Ge seed deposits with pinholes (Figure S3 in the Supporting Information). From back-gated measurements (with only the seed layers on the channel) we observe that the Si seed shifts the back-gate threshold voltage more negative and the Ge seed slightly shifts it positive, while degrading the average MoS_2 mobility by approximately 17% to 29%, respectively (Figure S4 in the Supporting Information and related discussion). However, from top-gated transistor measurements with ~5 nm HfO_2 top dielectric (Figure S5 in the Supporting Information), we note the Si seed enables lower hysteresis, steeper subthreshold slope, and higher transistor current, all indicating fewer interface traps (D_{it}) than the Ge seed. For these reasons, for the rest of this study we use the Si seed to enable the high-κ ALD of HfO_2 on MoS_2, and to achieve ultrathin top-gate insulators.

Figure 2a shows the cross-section transmission electron microscope (TEM) image of a MoS_2 transistor with 200 nm channel length using ~0.7 nm evaporated Si seed followed by 38 cycles of ALD HfO_2 as the top-gate dielectric. (Details of TEM sample preparation are described in Section 4 in the Supporting Information.) This confirms the conformal nature of the top-gate dielectric and the top-gate overlap with the source and drain contacts, which reduces the access resistance. Figure 2b shows the scanning TEM (STEM) image corresponding to Figure 2a and its energy dispersive X-ray spectroscopy (EDS) elemental mapping, revealing the Pd–Hf–Si components of the top-gate stack. Figure 2c further shows vertical EDS line profiles from Figure 2b, displaying the Si seed signal between the MoS_2 and HfO_2. The flat Si signal in the line profile (from −10 to 0 nm) arises from the SiO_2 substrate below the as-grown monolayer MoS_2 channel.

Figure 2d zooms into the TEM image from Figure 2a, revealing that ~0.7 nm of evaporated Si becomes ~1.6 nm of SiO_x on MoS_2 after oxidation. We also find a discrepancy in the ALD growth rate of HfO_2 on Si seed layer (on MoS_2)

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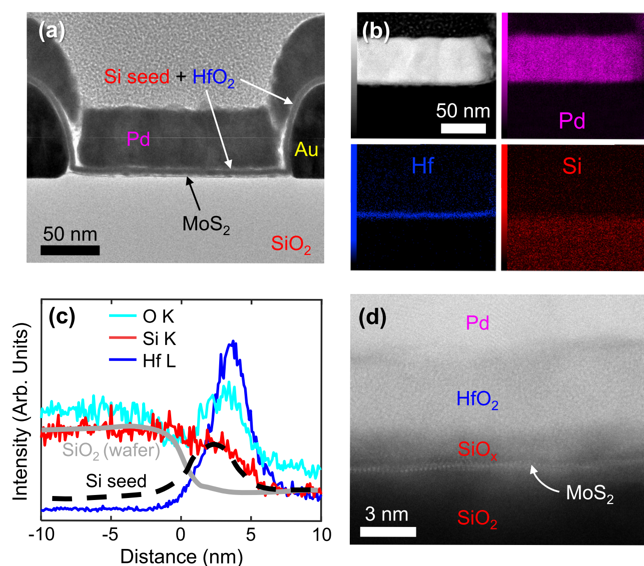

Figure 2. (a) Cross-section transmission electron microscope (TEM) image of a top-gated monolayer MoS_2 transistor with 200 nm channel length with Au contacts. The gate stack consists of ~0.7 nm evaporated Si followed by 38 cycles (~4 nm) of ALD HfO_2, and the Pd top gate. (b) High-angle annular dark-field (HAADF) cross-section scanning TEM (STEM) of the top gate stack (top left), and elemental mapping by energy-dispersive spectroscopy (EDS) of Pd (top right), Hf (bottom left), and Si (bottom right). (c) Vertical EDS profile through the gate stack, with MoS_2 set at 0 nm and positive distance into the top gate. The Si signal (red) comes from the sum of the SiO_2 substrate (gray) and the Si seed layer (dashed black). (d) Zoomed in cross-section STEM HAADF image, showing three-atom-thick monolayer MoS_2 and the SiO_x-HfO_2-Pd top-gate stack.

compared to on SiO_2/Si. The 38 ALD cycles of HfO_2 result in ~5 nm on a bare SiO_2/Si substrate but we observe HfO_2 thickness of ~4 nm on Si seed layer on MoS_2. This is consistent with a previous study,[14] suggesting the ALD growth (of HfO_2) is partially consumed to fill up gaps in the Si seed, which is not perfectly uniform on the MoS_2 surface. As a result, the subsequent ALD of HfO_2 grows not only vertically but also somewhat laterally, to fill in any gaps.

From the physical thicknesses confirmed by TEM, we estimate the top-gate EOT ≈ 2.3 nm using a dielectric constant of 3.9 for SiO_x and 22 for HfO_2.[28] This is an approximation, because the SiO_x layer likely incorporates some of the HfO_2, as mentioned above. (Thinner Si seed layers are more discontinuous, yielding an EOT even more dominated by the HfO_2 alone.) Our estimate is consistent with the EOT extracted from transistor measurements in Figure S6 of the Supporting Information. Plotting the top-gate threshold voltage ($V_{T,TG}$) vs the back-gate bias (V_{BG}), the magnitude of the resulting slope is the ratio of top-gate and back-gate EOT,[21−23,29,30] which provides an estimate of the top-gate EOT as 2.1 ± 0.3 nm, given the known back-gate insulator (90 nm of SiO_2). For the subsequent top-gated transistors, we use this method to estimate the top-gate EOT. Note that EOT and CET (the capacitance equivalent thickness[8]) are used interchangeably here, especially because the CET contains a contribution[31] from the MoS_2 channel, which is automatically included in our capacitance-based estimates. Additional discussion of this method is provided in Section 5 of the Supporting Information.

Next, we investigate the effect of reducing the Si seed thickness, in order to achieve lower EOT. We fabricate top-gated monolayer MoS_2 transistors with 0.3 or 0.4 nm Si seed, each followed by 38 cycles of ALD HfO_2, and compare these with the 0.7 nm Si seed described earlier. Figure 3a shows the comparison of top-gate threshold voltage, $V_{T,TG}$, for 3 μm long devices with TG dielectrics obtained with the three Si seed thicknesses tested. (Corresponding I_D vs V_{TG} measurements are given in Figure S9 of the Supporting Information.) Despite some device-to-device variability inherent to academic nano-fabrication, we note that reducing the Si seed layer thickness enables partial control of the top-gate threshold voltage. This is an important finding for two reasons: first, we show that relying on single device measurements is not sufficient in the face of fabrication-induced variability. (Not only from MoS_2 film variation, but also from additional steps of the top-gate process going beyond previous back-gate studies.[34,35]) Rather, box plots (as in Figure 3a) across groups of devices are needed to draw reasonable conclusions about trends.

Second, we uncover that the top-gate threshold voltage can be partly controlled by the thickness of the Si seed and the resulting SiO_x interlayer, which is essential for 2D transistors. The threshold voltages of well-behaved, i.e. normally off, *n*-type transistors must be small but positive (0.2 to 0.3 V range), to enable low-power devices with very low I_D at zero gate voltage and sufficiently high I_D at low supply voltage (0.7 to 1 V). The threshold voltage trend observed in Figure 3a is consistent with a similar roll-off when the EOT is reduced in Si transistors,[36−39] which has been attributed to positive charge in the interfacial SiO_x layer[36] or to dipoles at the HfO_2/SiO_x interface.[37−39] (Figure S11 in the Supporting Information displays an energy band diagram across the gate-to-channel stack.) We expect that the threshold voltage can be further controlled by adjusting the gate metal work function, and by introducing elements with different electronegativity (e.g., Al or La) near the dielectric interfaces.[8,38]

Figure 3b displays the subthreshold swing (*SS*) from forward and reverse top-gate sweeps, as a function of I_D, from devices with 0.3 and 0.4 nm Si seeding the HfO_2; in both cases, transistors reach $SS \approx 80$ mV/dec at room temperature and $V_{DS} = 1$ V. This is a good value, but we caution that low *SS*, by itself, is not a sufficient indicator of gate insulator quality, because certain charge trapping dynamics could even lead to $SS < 60$ mV/dec, albeit with hysteretic measurements.[40] Thus, having low SS *and* low hysteresis is more important, and Figure 3c shows dual-sweep I_D vs V_{TG} measurements, revealing very small hysteresis, < 5 mV, at both 0.1 and 10 nA/μm. These transistors also have a max/min current ratio of nearly 10^8 over a 2 V range, but the device with 0.4 nm Si seed is "better behaved," having $V_{T,TG} > 0$ V at 10 nA/μm constant-current[32] (the device with 0.3 nm seed has $V_{T,TG} \approx 0$ V). Finally, Figure 3d shows the measured I_D vs V_{DS} data from 1 μm long devices with 0.3 and 0.4 nm Si-seeded top-gate dielectrics. The transistor with 0.3 nm Si seed turns on at small negative V_{TG}, but the device with 0.4 nm Si seed is again "better behaved," turning on only at small positive V_{TG}. These findings are consistent with the broader data sets shown in Figure 3a.

From a historical perspective, it is interesting to note that the devices displayed in Figure 3d are modern, atomically thin monolayer successors of Dennard's 1 μm Si transistor[41] from 1974. They display a good linear region, good turn-on, and they operate at relatively low gate and drain voltages, simultaneously. (Something often overlooked in the 2D

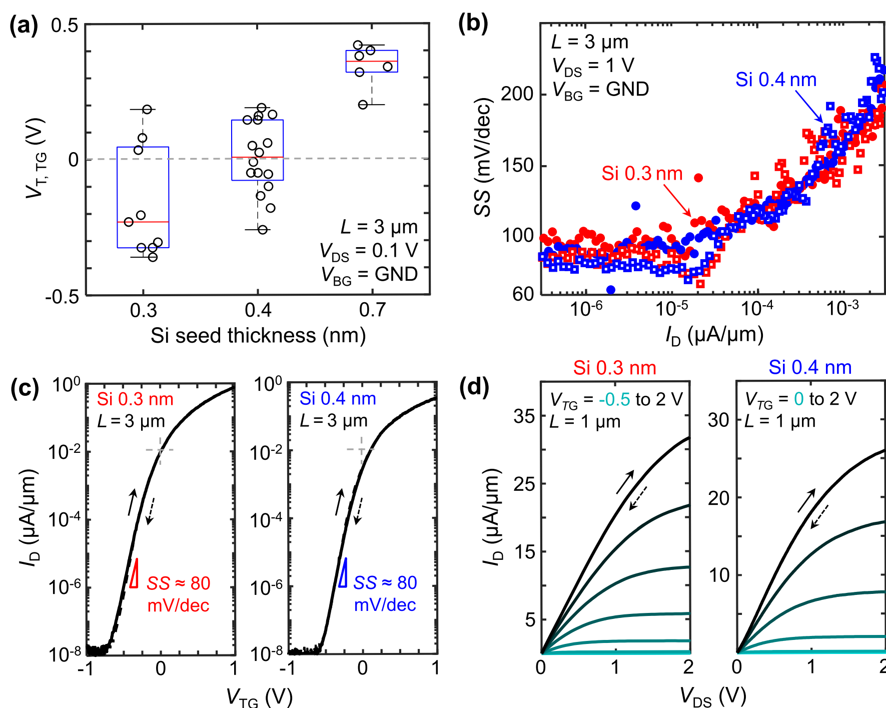

Figure 3. (a) Box plots of top-gate (TG) threshold voltage vs Si seed thickness. Each TG stack on monolayer MoS_2 has a Si seed of 0.3, 0.4, or 0.7 nm followed by ~4 nm of ALD HfO_2 and a Pd gate. Devices here are 3 μm long, with V_{DS} = 0.1 V and V_{BG} = 0 V. TG threshold voltages are evaluated[32] at I_D = 10 nA/μm. (Figure S10 in the Supporting Information shows more positive $V_{T,TG}$ at I_D = 100 nA/μm, as expected.) The three data sets include 9, 16, and 6 devices, from left to right, and within each set the symbols are given small, random lateral offsets to make them easier to distinguish. (b) Subthreshold swing (SS) vs I_D for two 3 μm long devices with 0.3 nm (red) and 0.4 nm (blue) Si seed below the HfO_2. Filled and hollow symbols mark forward and reverse V_{TG} sweeps, respectively. (c) Measured I_D vs V_{TG} of the same devices as in (b), with 0.3 nm (left) and 0.4 nm (right) Si seed layer. Solid and dashed lines are forward and reverse V_{TG} sweeps,[33] respectively, confirming very small hysteresis. Small gray crosses mark (0 V, 10 nA/μm), to illustrate the relative location of $V_{T,TG} \approx 0$ (left) and $V_{T,TG} > 0$ (right). V_{BG} = 0 V and V_{DS} = 1 V here. The I_D lower bound is the instrument noise floor (~10 fA with preamp and triax cables). (d) Measured I_D vs V_{DS} of 1 μm devices with 0.3 nm (left) and 0.4 nm (right) Si seed for the TG stack. Solid and dashed lines and arrows mark forward and reverse sweeps,[33] revealing negligible hysteresis. V_{TG} is raised in 0.5 V steps between bounds listed on the figure, and V_{BG} = 0 V. All measurements shown at room temperature.

transistor literature, where thick, unoptimized gate insulators frequently impose large gate and threshold voltages.) Unlike Dennard's transistor,[41] the modern EOT employed here is much thinner (~1 nm vs ~20 nm in 1974) and the supply voltages are lower (2 V vs 4 V), which also explains the weaker current saturation observed in our devices.

Before concluding, we wish to focus on our transistors with the thinnest EOT. Figure 4a shows the measured I_D vs V_{TG} at various back-gate biases (V_{BG}) of a device using the 0.3 nm Si-seeded HfO_2 top-gate dielectric. The inset plots the top-gate threshold voltage vs V_{BG}, wherein the magnitude of the slope represents the ratio of top-gate and back-gate EOT,[21−23,29,30] providing an estimate of the top-gate EOT = 0.90 ± 0.07 nm, given the BG insulator is 90 nm of SiO_2. This device has top-gate leakage current density <6 × 10^{-7} A/cm^2 at V_{TG} = 1 V, limited by our measurement noise floor. Because the top gate has some overlap with the source and drain (Figure 2a), the true leakage from the channel area is likely lower, in part aided by the large band gap of the SiO_x interfacial layer. This top-gate dielectric stack does not experience breakdown up to V_{TG} = 4 V, as shown in Figure S12 in the Supporting Information. We note that at such thin EOT (≤1 nm), estimating the on-state electron density in the MoS_2 channel (when $V_{GS} \gg V_T$) requires up to ~20% quantum and charge centroid capacitance corrections.[31,42]

Similarly analyzing one of our devices with 0.4 nm Si-seeded top-gate stack (Figure S13 in the Supporting Information), we find an EOT = 1.0 ± 0.1 nm with TG leakage current density <5 × 10^{-7} A/cm^2 at V_{TG} = 1 V, also limited by our measurement noise floor. In both cases of EOT ~ 0.90 nm and ~1.0 nm, the top-gate leakage current densities are over 4 orders of magnitude lower than the leakage current density requirement of <10^{-2} A/cm^2 for low standby power devices.[7]

Figure 4b shows a box plot of top-gate threshold voltages for devices with ~0.90 nm EOT and channel lengths between 0.1 and 3 μm (the I_D vs V_{TG} curves are in Figure S14 of the Supporting Information). Threshold voltages are extracted at constant current of 10 nA/μm (in red) and linear extrapolation (in blue).[32] With these devices, we observe that the estimated $V_{T,TG}$ (at 10 nA/μm) is lower than that from linear extrapolation, which has also been noted by others.[34,35] This occurs partly because the contacts and the channel may not have the same gate voltage dependence,[45] and the contact effect is more pronounced at shorter channel lengths. We also note that the $V_{T,TG}$ decreases, i.e. rolls-off, and *SS* increases at shorter channel lengths. This has also been observed in fully depleted silicon-on-insulator (SOI) transistors[46] and is caused by lateral field penetration through the thicker back-gate dielectric (here, 90 nm SiO_2). In other words, this effect is not fundamental to 2D semiconductors and is greatly reduced when a thin back-gate dielectric is used[28,35] (also see the *SS* in Figure S14 of the Supporting Information).

Finally, Figure 4c benchmarks gate leakage at V_{GS} = 1 V as a function of EOT or CET (capacitance equivalent thickness),

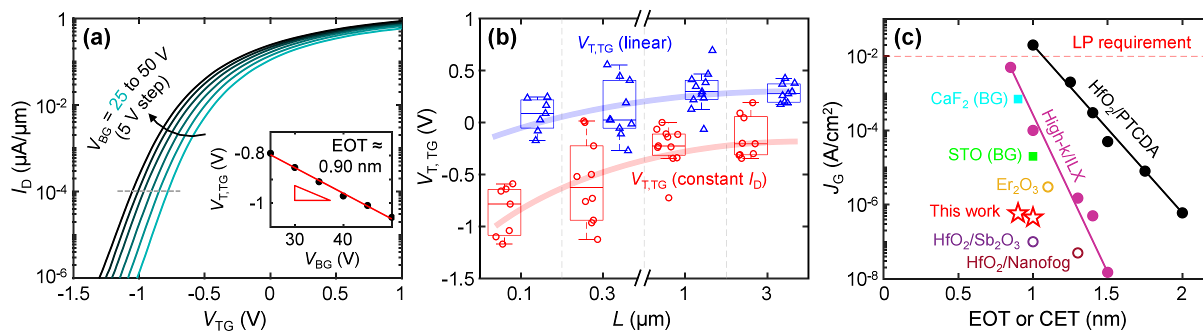

Figure 4. (a) Measured I_D vs V_{TG} of a device using 0.3 nm Si seed for the top-gate dielectric, at multiple back-gate biases V_{BG}, as labeled. Here, V_{DS} = 0.1 V and channel length L = 3 μm. Inset shows the extracted top-gate threshold voltages, $V_{T,TG}$ (at 0.1 nA/μm constant current) as a function of V_{BG}. (b) Box plot of extracted threshold voltages for different channel lengths (0.1 to 3 μm) using 0.3 nm Si seed layer for the top-gate dielectric. Red and blue are threshold voltages from constant current (at 10 nA/μm) and linear extrapolation methods,[32] respectively, at V_{DS} = 0.1 V and V_{BG} = 0 V. The number of devices measured is 7, 10, 11, and 9 from 0.1 to 3 μm, respectively. Symbols are given small, random lateral offsets to make them easier to distinguish. Red and blue trend lines are guides to the eye. (c) Benchmarking gate leakage current density (J_G, at V_{GS} = 1 V) as a function of EOT or CET, compared to previous results with monolayer MoS_2 channels.[16,21−23,30,43,44] (Due to varying extraction methods, this plot uses EOT and CET interchangeably.) Hollow symbols represent measurements with J_G limited by the instrumentation. The BG label refers to EOT of back-gate dielectrics without a top gate. The horizontal dashed line marks low-power (LP) requirements.[7]

comparing our results with those in the literature. At an estimated top-gate EOT ≈ 0.90 nm and leakage $<6 \times 10^{-7}$ A/cm², our results are among the best reported, due to the quality, uniformity, and large band gap of the SiO_x interfacial layer. Importantly, the materials used in our gate stack are standard in industrial semiconductor processing and widely available in research fabrication facilities, as well. (In contrast, some interfacial layers like Sb_2O_3 and PTCDA have smaller band gaps and may not be compatible with industrial CMOS processes.[16,23]) Although the e-beam evaporated Si seed used here is not expected to be conformal on high aspect ratio 3D structures or gate-all-around transistors, low-temperature ALD processes of SiO_2[47−49] or similar seed layers exist, and could be adapted on TMDs.[11,30,50,51]

In summary, we studied various interfacial (seed) layers for top-gate dielectrics on monolayer MoS_2. Among the seed layers used here, only Si and Ge appear benign to MoS_2, and the evaporated Si provides an SiO_x interfacial layer with the best results for seeding HfO_2 onto MoS_2 with nearly hysteresis-free transistor behavior. Using ~0.3 nm Si seed, we achieve sub-1 nm top-gate equivalent oxide thickness (EOT) on monolayer MoS_2, with low leakage (<1 μA/cm²) and ~80 mV/dec subthreshold swing at room temperature. Importantly, the interfacial layer can be used to tune the top-gate threshold voltage, which is a significant advance for TMD transistors. A Si-based seed layer which enables ultrathin EOT on TMDs is highly practical because all materials are CMOS-compatible, and the simple deposition can also facilitate such top-gate fabrication in many academic and research facilities.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.4c01775.

Device fabrication details, AFM and XPS analysis, comparison of Si and Ge seed layers, discussion of top-gate EOT estimation procedure, additional current−voltage measurements and threshold voltages, approximate energy band diagram of the gate stack, top-gate leakage measurements, and comments about variation and yield (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Eric Pop − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States; Department of Materials Science & Engineering and Department of Applied Physics, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-0436-8534; Email: epop@stanford.edu

Authors

Jung-Soo Ko − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0009-0006-1890-9038

Sol Lee − *Department of Physics, Yonsei University, Seoul 03722, Republic of Korea; Center for Nanomedicine, Institute for Basic Science, Seoul 03722, Republic of Korea;* orcid.org/0000-0002-4334-5063

Robert K. A. Bennett − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0001-7427-8724

Kirstin Schauble − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0002-4130-9181

Marc Jaikissoon − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0001-5102-6348

Kathryn Neilson − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-1061-2919

Anh Tuan Hoang − *Department of Materials Science & Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-0911-1391

Andrew J. Mannix − *Department of Materials Science & Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-4788-1506

Kwanpyo Kim − *Department of Physics, Yonsei University, Seoul 03722, Republic of Korea; Center for Nanomedicine, Institute for Basic Science, Seoul 03722, Republic of Korea;* orcid.org/0000-0001-8497-2330

Krishna C. Saraswat − *Department of Electrical Engineering, Stanford University, Stanford, California 94305, United States; Department of Materials Science & Engineering,*

Stanford University, Stanford, California 94305, United States

Complete contact information is available at:
https://pubs.acs.org/10.1021/acs.nanolett.4c01775

Notes

The authors declare no competing financial interest.

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Supporting Information

Sub-Nanometer Equivalent Oxide Thickness and Threshold Voltage Control Enabled by Silicon Seed Layer on Monolayer MoS_2 Transistors

Jung-Soo Ko,[1] Sol Lee,[2,3] Robert K. A. Bennett,[1] Kirstin Schauble,[1] Marc Jaikissoon,[1] Kathryn Neilson,[1] Anh Tuan Hoang,[4] Andrew J. Mannix,[4] Kwanpyo Kim,[2,3] Krishna C. Saraswat,[1,4] Eric Pop[1,4,5]

[1]*Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA*
[2]*Department of Physics, Yonsei University, Seoul 03722, Republic of Korea*
[3]*Center for Nanomedicine, Institute for Basic Science, Seoul 03722, Republic of Korea*
[4]*Department of Materials Science & Engineering, Stanford University, Stanford, CA 94305, USA*
[5]*Department of Applied Physics, Stanford University, Stanford, CA 94305, USA*

1. Device Fabrication Process Flow

As shown in **Figure S1**, MoS_2 is first grown by chemical vapor deposition (CVD) at 750 °C on a thermally oxidized SiO_2 (90 nm) on p^{++} Si substrates.[1] After depositing alignment markers, we define and pattern large contact pads (100 × 100 μm^2) consisting of SiO_2 (10 nm), Ti (2 nm), and Pd (30 to 50 nm), followed by lift-off. The SiO_2 under the pads minimizes pad-to-substrate leakage. Then, device channels are patterned by electron-beam lithography and etched using XeF_2 chemistry. Next, Au source and drain contacts are patterned and e-beam evaporated (from 45 to 90 nm thick, among various samples), connecting the MoS_2 channels with the large contact pads. After this step, the devices can serve as back-gated transistors using the highly-doped Si as the global back-gate.

For top-gating, dielectric seed layers are e-beam evaporated at ~10^{-7} Torr. After the seed layers are evaporated, they are exposed to air before the Raman and X-ray photoelectron spectroscopy (XPS) measurements shown in **Figure 1** of the main text. Only the Si and Ge seeds are chosen for subsequent top-gate formation and, on average, these were exposed to air for ~1 hour before placing them in the atomic layer deposition (ALD) chamber. The samples sit in the ALD chamber at 200 °C for ~30 min before HfO_2 is deposited at 200 °C using tetrakis(dimethylamido)hafnium and H_2O. Based on a previous study,[2] sub-1 nm thin Si layers on MoS_2 are not continuous and they are expected to fully oxidize. For example, we do not see evidence of remaining Si on the MoS_2 from TEM in our main text **Figure 2**, and we also do not see remaining Si on the surface from XPS, as shown in **Figure S2** below.

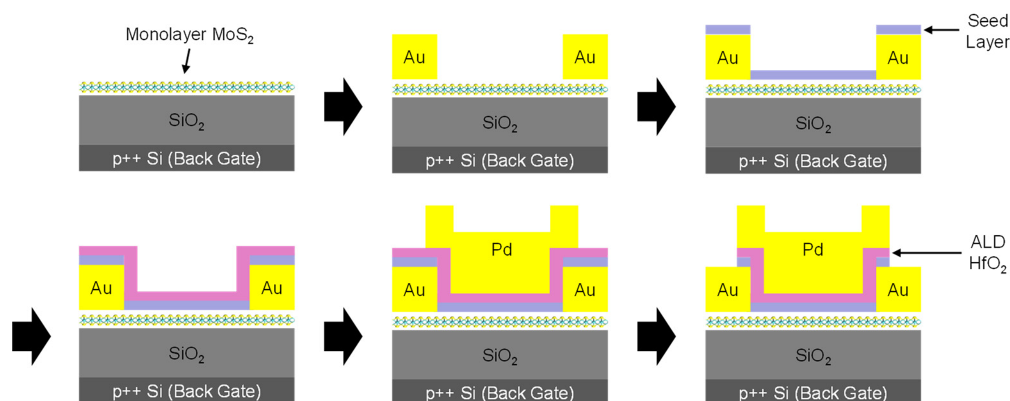

Figure S1. Top-gated transistor fabrication process flow starting from as-grown CVD monolayer MoS_2 on a SiO_2/p^{++} substrate. Figures show the cross-section of the devices. The devices are also back-gated by the p^{++} Si.

Finally, we pattern, e-beam evaporate, and lift-off the Pd top-gate. Then, we etch the top gate oxide over the large-area pads (to enable probing) using inductively-coupled plasma etching with CF_4. All measurements are performed at room temperature (unless stated otherwise) in a vacuum probe station at ~10^{-4} Torr. Top-gated devices were annealed in the same vacuum probe station at 150 °C, while those without a top gate were annealed at 250 °C, both for two hours.

2. Comparison Before and After Seed Layer Deposition on Monolayer MoS_2

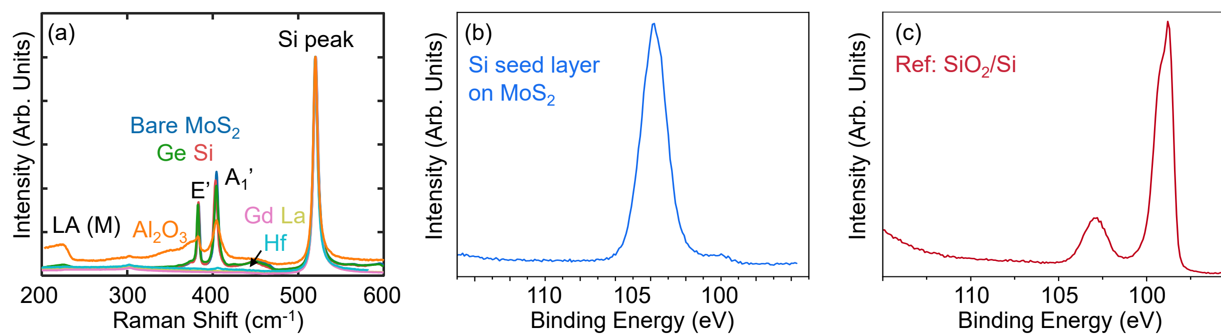

Figure S2. (a) Wider range of the Raman spectra from **Figure 1c**. (b) XPS measurement of evaporated Si ~0.3 nm after oxidation, on our lab-grown monolayer MoS_2 on SiO_2/Si substrate and (c) XPS of bare Si substrate with native oxide. The Si-Si bonding signal appears at ~99.4 eV only in the bare Si sample with native oxide, but not in the Si seed layer on MoS_2 sample, indicating that our ultrathin evaporated Si seed layer oxidizes into amorphous SiO_x.

Figure S2a shows Raman spectra between 200 and 600 cm^{-1} from the main text **Figure 2a**, normalized to the Si peak at 520 cm^{-1}. Raman spectra are measured in air, using a Horiba Labram, with a 532 nm wavelength laser source, 2.5% incident power (corresponding to 0.12 mW), and 1800 grooves/mm grating. Note that with Al_2O_3 evaporation on monolayer MoS_2, we see the appearance of the LA(M) peak, indicating damage to the monolayer MoS_2.[3] **Figures S2b,c** display XPS measurements of oxidized Si seed on MoS_2 (on SiO_2) and of a Si surface with native SiO_2. The samples with Si seed on MoS_2 were exposed to air for a few hours, similar to the device top-gate fabrication steps, and this Si seed appears almost completely oxidized to SiO_x. Any remaining Si is expected to oxidize in the ALD chamber, before and during the subsequent HfO_2 deposition at 200 °C.

Table S1 shows the list of evaporated seed layers used in this work and information about damage or reaction with the monolayer MoS_2, melting point, and enthalpy of formation with sulfur and oxygen.

Seed	Damage or Reaction with Monolayer MoS_2	Melting Point (°C)	Enthalpy of Formation with Sulfur (kJ/mol)	Enthalpy of Formation with Oxygen (kJ/mol)
Si	No	1410	-120	-859
Ge	No	938	-69	-452
Al_2O_3	Yes	2072	-	-
Hf	Yes	2227	-248.9	-1112
La	Yes	920	-912	-1195
Gd	Yes	1312	-	-1213

Table S1. Table of investigated seed layer materials, damage or reaction with monolayer MoS_2 (based on Raman and XPS spectra in main text **Figures 1c,d**), melting point, and enthalpy of formation with sulfur and oxygen.[4-7]

Figure S3 shows atomic force microscopy (AFM) maps of as-grown monolayer MoS_2, and after evaporating Si or Ge. The root-mean-square (RMS) roughness does not change much after Si evaporation, suggesting that Si forms a uniform seeding layer on MoS_2. With Ge evaporation, we observe Ge clustering that leads to pinholes visible from the AFM image.

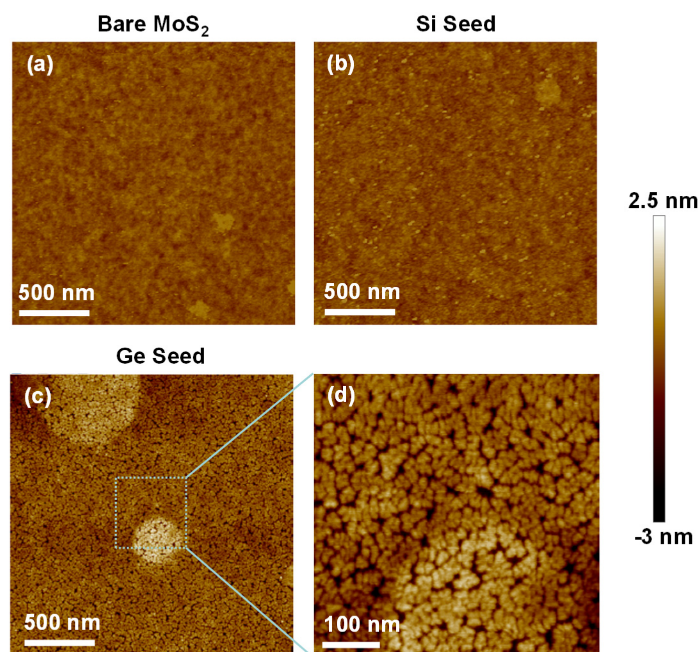

Figure S3. Atomic force microscopy images of (a) bare, as-grown monolayer MoS_2 (on SiO_2), (b) after Si evaporation, (c) after Ge evaporation, and (d) zoomed-in image from the dashed square in (c). Seed layers are deposited with 0.2 Å/s rate and thickness of ~1 nm. Root-mean-square roughness RMS = 0.20 nm for bare MoS_2, 0.25 nm after Si evaporation, and 0.55 nm after Ge evaporation.

Figures S4a,b show measured transfer characteristics of back-gated monolayer MoS_2 field-effect transistors (FETs) without any top gates. Devices are first measured as fabricated (in blue) and then re-measured after Si or Ge seed evaporation (red). Measurements are done in vacuum after annealing at 250 °C to remove surface moisture, before each measurement (i.e., devices with seed layer on the MoS_2 channel have undergone two such vacuum anneal steps, see **Figure S4c**). The Si seed layer shifts the average back-gate threshold voltage more negative and the Ge seed shifts it in a positive direction, on average. This occurs likely due to different signs of fixed charge[8-9] (i.e., positive vs. negative) in the sub-stoichiometric SiO_x and GeO_x layers formed on top of the MoS_2 channel.

The average field-effect mobility of all measured devices in **Figure S4a** decreases by ~17% from ~32 $cm^2V^{-1}s^{-1}$ before to ~27 $cm^2V^{-1}s^{-1}$ after Si seed layer evaporation. With Ge seed evaporation, the average field-effect mobility decreases by ~29% from ~34 $cm^2V^{-1}s^{-1}$ (before) to ~24 $cm^2V^{-1}s^{-1}$ (after). These mobility values are nevertheless well within the typical range we have previously found for our CVD-grown monolayer MoS_2, including growth-to-growth and device-to-device variations.[10-11]

The reduced mobility after seed layer evaporation could be attributed to one or more of three causes: (1) The oxidized seed layers (as SiO_x or GeO_x) may introduce some amount of interfacial charged impurities or interface surface roughness, which increase electron scattering in the MoS_2 channel. (2) The samples with seed layer have undergone *two* anneal steps at 250 °C (**Figure S4c**) to remove surface moisture, and the additional anneal could have affected the monolayer MoS_2. (3) The seed evaporation process *could* introduce some defects in the MoS_2 (due to thermal energy from the evaporation) which

are not detectable by Raman spectroscopy in main text **Figure 1c**. We think the latter is less likely, because Si has a higher melting point than Ge (see **Table S1**) but shows a lower average decrease of field-effect mobility. The devices employed here are 3 µm long, and we expect that the field-effect mobility is a reasonable proxy for transport in the channel, with contacts playing less of a role.

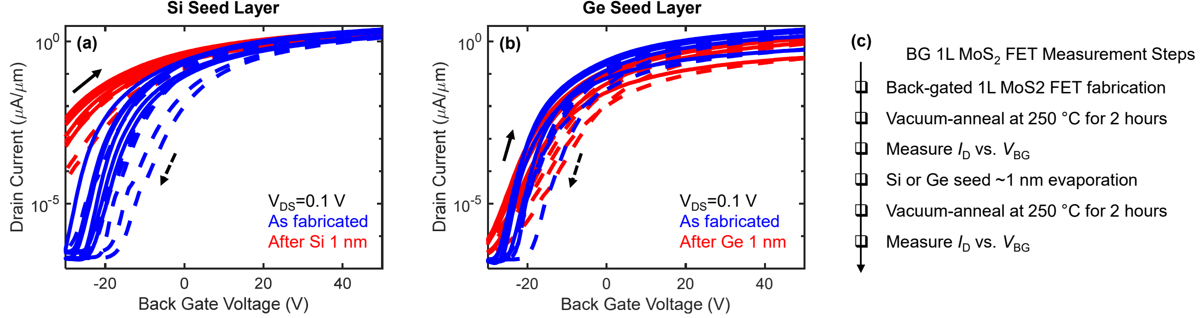

Figure S4. Measured I_D vs. V_{BG} using (a) ~1 nm Si seed layer and (b) ~1 nm Ge seed layer on monolayer MoS_2 (no HfO_2 and no top-gate). Channels are L = 3 µm long. Blue curves are from as-fabricated devices, red curves are after seed layer evaporation. Solid and dashed lines show forward and reverse sweeps, respectively. 6 devices are shown for Si and 5 for Ge seed layer. On average, the Si seed shifts the back-gate V_T negatively and decreases the average field-effect mobility by ~17%. The Ge seed slightly shifts the back-gate V_T positively and decreases the average field-effect mobility by ~29%. (c) Measurement steps for the back-gated monolayer MoS_2 transistors in (a) and (b); measurements are conducted at room temperature, in a vacuum probe station after annealing at 250 °C. Note that red curves in (a) and (b) have gone through two 250 °C anneal steps in the probe station vacuum before measurement.

3. Top-gated Monolayer MoS_2 FETs Comparing Si and Ge Seed Layer

Figure S5 shows the I_D-V_{TG} curves of top-gated MoS_2 FET using Si or Ge seed layers for ALD HfO_2. Measurements are done in an N_2 environment after annealing in vacuum at 150 °C. Seed layers are all deposited at a rate of 0.2 Å/s for ~1 nm, followed by 38 cycles (~5 nm) of ALD HfO_2 and Pd top gate (as described in **Figure S1**). Compared to Ge, the ~1 nm Si seed enables smaller hysteresis and steeper subthreshold slope at any drain current, indicating that Si (which oxidizes to SiO_x after removal from the evaporation chamber) provides a better interface to MoS_2.

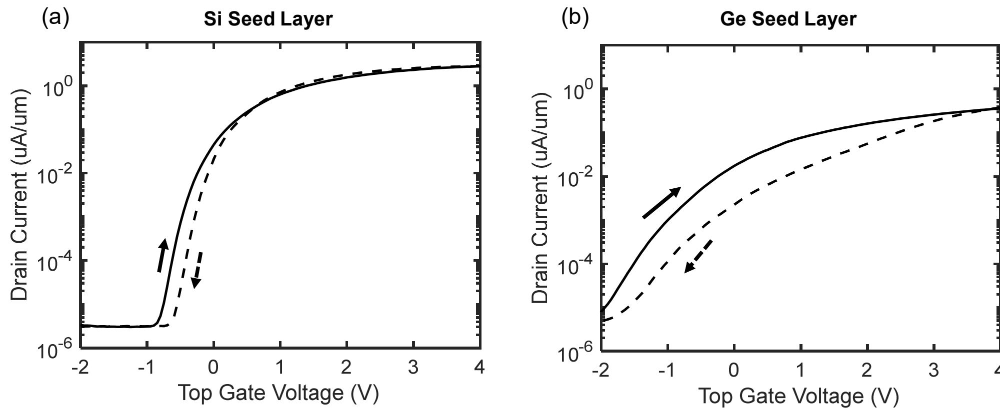

Figure S5. Measured I_D vs. V_{TG} from top-gated (TG) monolayer MoS_2 FETs with L = 3 µm using (a) ~1 nm Si seed layer and (b) ~1 nm Ge seed layer. Measurements were done in N_2 ambient without annealing prior to electrical characterization, at V_{BG} = 0 V and V_{DS} = 0.1 V. Solid and dashed lines show forward and reverse sweeps, respectively.

4. Top-gated Monolayer MoS_2 FETs Using Ultrathin Evaporated Si Seed Layer

For the transmission electron microscopy (TEM) image in main text **Figure 2**, cross-sectional TEM samples are prepared using a focused ion beam (Crossbeam 540, ZEISS). TEM, high-angle annular dark-field scanning TEM (HAADF-STEM) imaging, and scanning TEM energy dispersive X-ray spectroscopy (EDS) mapping are performed with a double Cs-aberration corrected ARM-200F operated at 200 kV. For HAADF imaging, the detector's inner and outer collection semi-angles were set to 68 and 280 mrad, respectively, with a convergence semi-angle of 30 mrad.

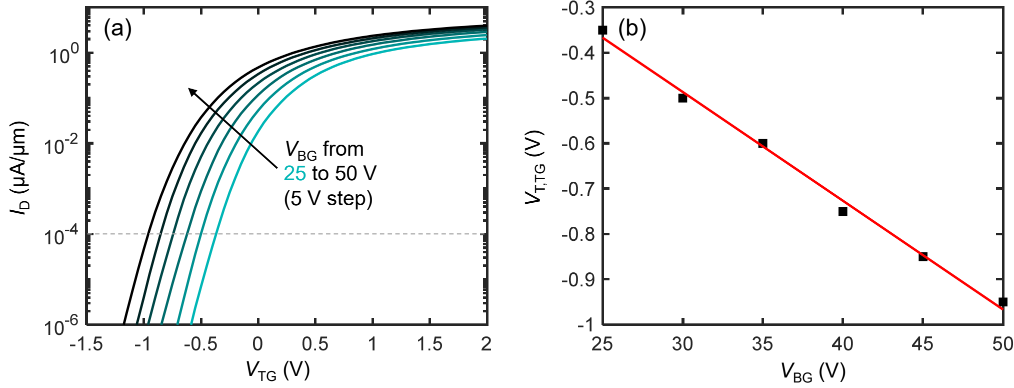

Figure S6. (a) Measured I_D vs. V_{TG} curves from a 1 μm-long top-gated MoS_2 FET using 0.7 nm Si seed layer followed by 38 cycles of ALD HfO_2. Devices are measured at V_{DS} = 0.1 V and V_{BG} ranges from 25 V to 50 V with a 5 V step. (b) Threshold voltages from the top gate sweep as a function of the applied V_{BG} from (a). Top-gate threshold voltages were extracted at the constant current of 0.1 nA/μm [dashed line in (a)].

Figure S6 shows the EOT estimated using the transistor transfer characteristics from a 1 μm long device on the same chip that has the device shown in main text **Figure 2**. The top-gate dielectric consists of 0.7 nm evaporated Si seed followed by 38 cycles of ALD HfO_2. **Figure S6a** shows measured I_D-V_{TG} curves at various V_{BG} and **Figure S6b** shows the extracted top-gate threshold voltages ($V_{T,TG}$) from the top gate sweeps as a function of the applied back-gate biases. Here, we extract $V_{T,TG}$ by the constant current method[12] at 0.1 nA/μm, to ensure that for all given V_{BG}, subthreshold swings (around $V_{T,TG}$) are nearly the same at the fixed constant current. We have also tested this extraction method at 10 pA/um, 1 nA/um and 10 nA/um, all with similar results. The magnitude of the slope in **Figure S6b** represents the ratio of the top-gate EOT to the back-gate EOT (here, 90 nm).[13-17] For this particular device type, the extracted top-gate dielectric EOT = 2.1 ± 0.3 nm, where the mean and error are estimated by linear fitting to subsets of 3 to 6 points among the ones shown in **Figure S6b**.

5. Additional Discussion on the Top-Gate EOT Estimate

The procedure we have used to estimate the EOT relies on a simple capacitance divider (between the top-gate and bottom-gate), and it is widely used in the 2D transistor literature.[13-17] We have found that the most important consideration is to minimize the effects of the transistor contacts, because the fringing fields around the contacts are not identical from the top gate compared to the bottom gate (the rest of the channel is a parallel plate capacitor). To achieve this, we rely on long-channel devices (3 μm, unless stated otherwise) for such estimates throughout our work. That these can be considered proper long-channel devices is apparent from our previous work with such Au contacts,[18] and can also be seen in main text **Figure 3d**. In addition, we have found that estimating the EOT only at large V_{BG} is important, because this "gates the contacts" and minimizes their Schottky barrier. In **Figure S7** below, we show an example where we have swept the back-gate voltage over a much wider range,

while monitoring the top-gate threshold voltage, $V_{T,TG}$. The correct EOT (≈ 1 nm) can be estimated at V_{BG} > 30 V here (red slope below), because at lower back-gate voltages the contacts dominate and cause an erroneous EOT estimate. It is also important to use *I*-*V* measurements with very low hysteresis for this technique, as done throughout this study.

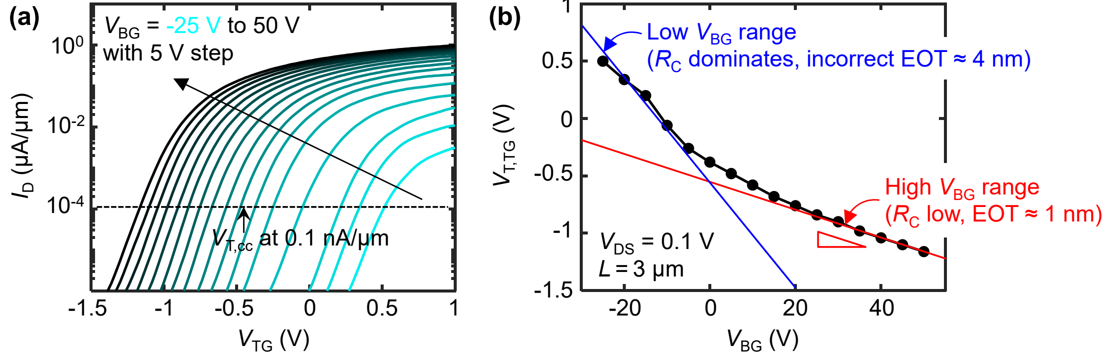

Figure S7. (a) Measured I_D vs. V_{TG} from a 3 μm long top-gated MoS_2 transistor with 0.3 nm Si seed layer followed by 38 cycles of ALD HfO_2. The measurement is deliberately shown over a wide V_{BG} range (-25 V to 50 V). The top-gate threshold voltage $V_{T,TG}$ in (b) is taken at constant current of 0.1 nA/μm vs. applied V_{BG}. The EOT can be estimated from the magnitude of the slope, but the blue slope at low V_{BG} gives an incorrect EOT estimate due to contact effects. The red slope at high V_{BG} "back-gates" the contacts and minimizes their effect, giving the correct EOT ≈ 1 nm. The red slope is the ratio of top-gate EOT to the back-gate EOT (here 90 nm SiO_2).

Whenever possible, we also compare the estimated EOT with the physical thickness estimated from cross-sectional TEM images (e.g., in main text **Figure 2**). In a separate effort,[19] we fabricated a chip with top-gate dielectric of 0.2 nm Si seed followed by 38 cycles ALD HfO_2 (same as for the transistors shown in the main manuscript). After electrical analysis, this also provided a top-gate EOT of ~0.9 nm using our estimates. We note that both 0.2 and 0.3 nm Si seed layers are very likely discontinuous, so it is unsurprising that they yield similar EOT (0.9 to 1 nm) when followed by the same 38 cycles of HfO_2. **Figure S8** below displays this analysis, where the estimated ~0.9 nm EOT is in good agreement with the physical thickness from TEM, using the typical dielectric constants of our oxides.

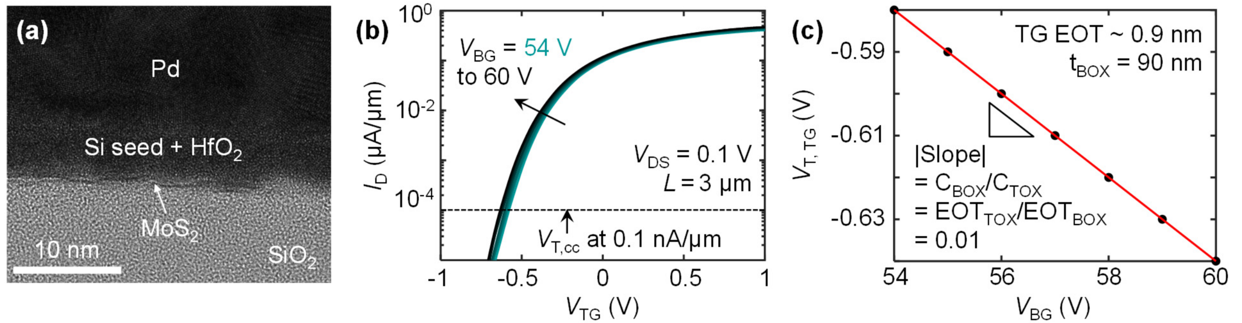

Figure S8. (a) Cross-section TEM image of top-gated (TG) monolayer MoS_2 transistor channel using TG dielectric of 0.2 nm evaporated Si seed followed by 38 cycles ALD HfO_2 (same number of cycles as for devices in our main manuscript). (b) Measured I_D vs. V_{TG} at V_{BG} from 54 V to 60 V with a 1 V step on the MoS_2 device from (a), and its corresponding (c) $V_{T,TG}$ vs. V_{BG} (V_T is extracted by constant current at 0.1 nA/μm).

6. Additional Figures and Discussion

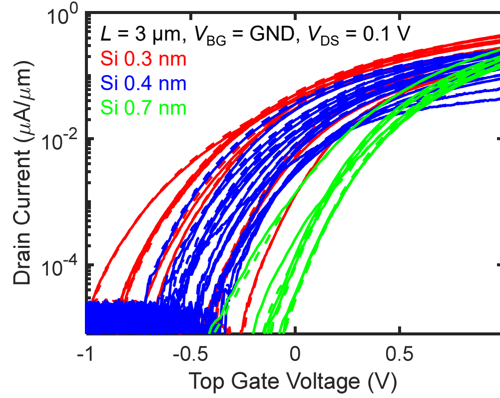

Figure S9. Measured I_D vs. V_{TG} curves from top-gated monolayer MoS_2 devices with Si seed layer thicknesses of 0.3 nm (red), 0.4 nm (blue), and 0.7 nm (green) followed by 38 cycles of ALD HfO_2 and the Pd top gate. All device channels are 3 µm long, and measurements are done with V_{DS} = 0.1 V and back-gate bias V_{BG} = 0 V. The number of measured devices is 9, 16, and 6 for 0.3, 0.4, and 0.7 nm of evaporated Si seed, respectively. Solid and dashed lines represent forward and reverse sweeps, respectively, showing minimal hysteresis.

Figure S9 shows measured I_D vs. V_{TG} curves from 3 µm long top-gated monolayer MoS_2 transistors with varying evaporated Si seed thicknesses of 0.3, 0.4 and 0.7 nm. On average, we observe a negative shift of the top-gate threshold voltage when reducing the Si seed thickness. (This figure is where the $V_{T,TG}$ from main text Figure 3a are taken from, at 10 nA/µm.) We note that there is some variation in the number of devices reported in **Figure S9** for each group, which is due to differences in fabrication yield, initially arising from variations in MoS_2 growth and back-gated device functionality. Among working back-gated devices, the top-gate process with Si seed yielded >90% success rate, especially for the later sets (with 0.3-0.4 nm Si seed) compared to earlier ones, as our top-gate process improved.

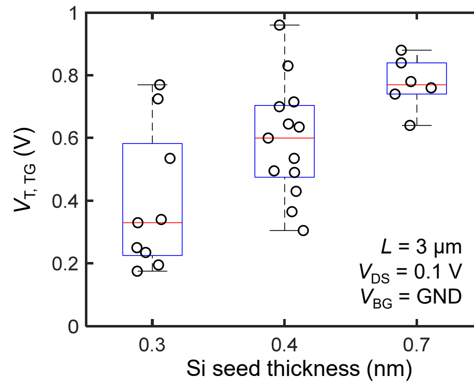

Figure S10. Top-gate threshold voltage vs. Si seed thickness for the devices from main text **Figure 3a**, but extracting $V_{T,TG}$ at 100 nA/µm constant current. A few devices in **Figure 3a** that do not reach 100 nA/µm are excluded here. Within each group the data points are given small (random) lateral offsets to make them easier to distinguish.

Figure S10 shows the top-gate threshold voltage ($V_{T,TG}$) as a function of the evaporated Si seed thickness, with $V_{T,TG}$ extracted at a higher constant current (100 nA/µm) than in **Figure 3a** (10 nA/µm). As expected, the median $V_{T,TG}$ values for each Si seed thickness are higher here than in **Figure 3a**, but the trend is the same: the $V_{T,TG}$ decreases as the Si seed layer thickness decreases.

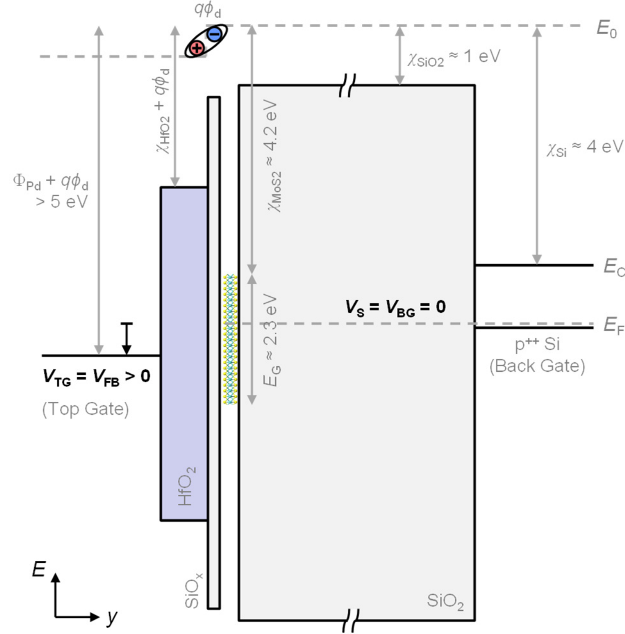

Figure S11. Approximate energy band diagram through the top gate, the gate dielectric stack, the MoS_2 channel, and the SiO_2/Si substrate, at flatband ($V_{TG} = V_{FB}$). Here a dipole at the HfO_2/SiO_x interface, ϕ_d, has been suggested[20-21] to increase the flatband voltage, V_{FB} (vs. the case without a dipole). As the SiO_x thickness is reduced, this dipole could be diminished, causing a flatband (V_{FB}) voltage reduction and thus a $V_{T,TG}$ reduction, as shown in Figure 3a. A similar explanation of the observed $V_{T,TG}$ roll-off could be provided by enhanced positive charge generation in the interfacial SiO_x layer as its thickness is reduced below a critical value.[9] We note that the trend observed in Figure 3a is *opposite* of that expected from reducing EOT in traditional Si transistors,[22] when considering the depletion charge in MoS_2 is positive (*n*-doping by S vacancies) rather than negative in traditional *n*-type Si transistors with acceptor channel doping. In the figure, Φ_{Pd} is the gate workfunction, χ are electron affinities, ϕ_d is the dipole, E_G is the monolayer MoS_2 band gap, E_0 is the vacuum level, E_C is the conduction band, and E_F is the Fermi level. Layer thicknesses are not to scale.

Figure S11 shows the approximate energy band diagram of the gate dielectric stack from the top-gate Pd metal down to the p^{++} Si back-gate at the flat-band condition. The dipole at the interface of the SiO_x seed and the ALD HfO_2 is represented as $q\phi_d$. As the SiO_x thickness decreases below some critical 0.8-1.0 nm range, the dipole is reduced or destroyed, causing decreasing V_{FB} and V_T.[23]

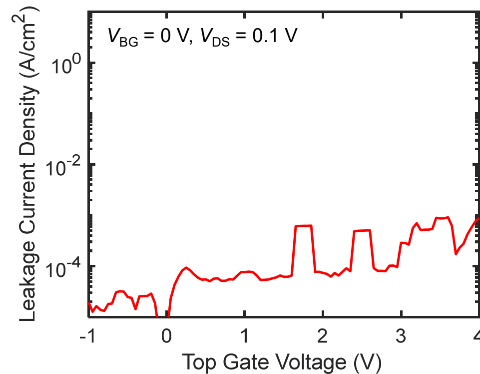

Figure S12. Top-gate leakage current density vs. applied top-gate voltage (V_{TG}) from a 1 μm-long device with a monolayer MoS_2 channel, and a top-gate stack with 0.3 nm Si seed layer, 38 cycles ALD HfO_2 (same as for all devices in this work, unless stated otherwise), and Pd gate. The top gate does not show dielectric breakdown up to $V_{TG} = 4$ V. As the top gate overlaps with the source/drain, the gate leakage purely from the channel is lower than shown.

Figure S12 displays the top-gate leakage current density as a function of the top-gate voltage from a 1 μm-long device using a top-gate dielectric of 0.3 nm evaporated Si seed layer followed by 38 cycles of ALD HfO_2. This device is on the same chip as the device with EOT ≈ 0.90 nm (in Figure 4a) and it shows breakdown voltage higher than 4 V. The relatively good (low) leakage and (high) breakdown voltage is at least in part enabled by the large band gap of the interfacial SiO_x layer.

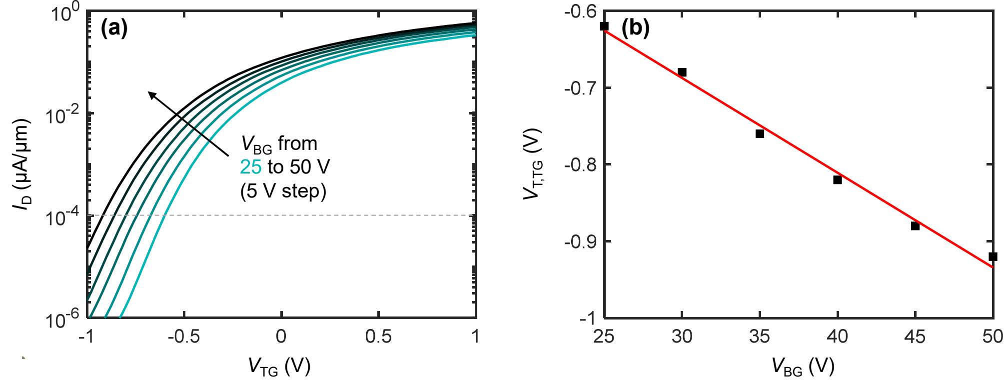

Figure S13. (a) Measured drain current vs. top-gate voltage with various back-gate biases using evaporated 0.4 nm Si seed followed by 38 cycles of ALD HfO_2. V_{DS} = 0.1 V is applied, and the channel length of this device is 3 μm. The $V_{T,TG}$ was extracted at a constant current of 0.1 nA/μm [dashed line in (a)]. (b) Extracted $V_{T,TG}$ vs. back-gate voltage, wherein the magnitude of the linear slope represents the ratio of top-gate and back-gate EOT.

Figure S13a shows measured I_D vs. V_{TG} curves from a 3 μm long device at various back-gate biases using the top dielectric stack of evaporated Si 0.4 nm followed by 38 cycles of ALD HfO_2. Using the magnitude of the slope from **Figure S13b** and the back-gate dielectric thickness of 90 nm SiO_2, we estimate the top-gate dielectric EOT = 1.0 ± 0.1 nm. The same device also reaches a top-gate leakage current density of 5×10^{-7} A/cm^2 at V_{GS} = 1 V, limited by the instrument noise floor. Because the top gate overlaps with the source and drain, the leakage current over the channel is expected to be lower.

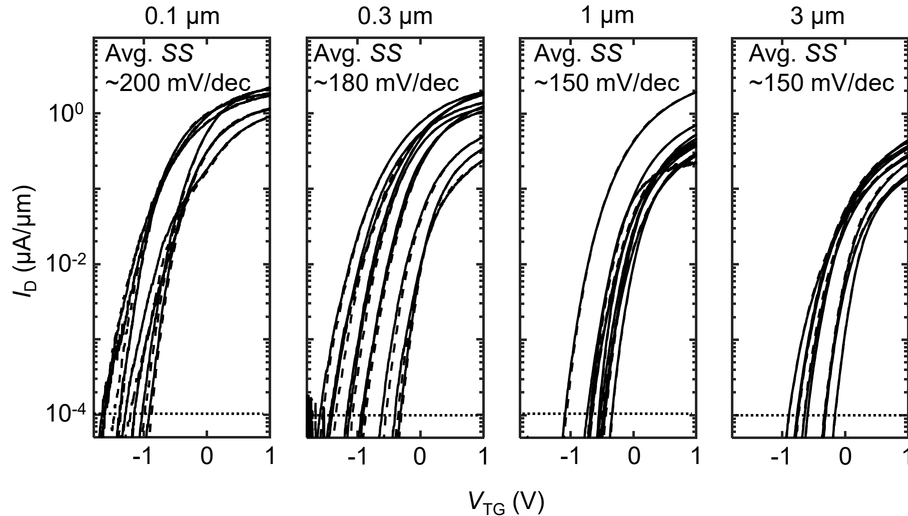

Figure S14. Measured I_D vs. V_{TG} with V_{BG} = 0 V and V_{DS} = 0.1 V, for channel lengths between 0.1 μm to 3 μm, as labeled. Solid and dashed lines represent forward and reverse sweeps, respectively, essentially indistinguishable due to the very small hysteresis. The number of devices measured is 7, 10, 11, and 9 for 0.1 μm, 0.3 μm, 1.0 μm, and 3 μm channels, respectively, and the top-gate threshold voltage ($V_{T,TG}$) distributions are shown in Figure 4b of the main text. At a constant current of 0.1 nA/μm, the average subthreshold swing (avg. *SS*) is labeled for each channel length, showing an increase (degradation) of the *SS* as the channel length is reduced. This occurs due to field penetration through the thick back-gate SiO_2 used here, similar to previous observations for silicon-on-insulator (SOI) devices.[24]

Figure S14 shows measured I_D vs. V_{TG} from devices with channel lengths of 0.1 μm, 0.3 μm, 1.0 μm, and 3 μm using the top-gate dielectric stack of 0.3 nm evaporated Si followed by 38 cycles of ALD HfO_2. All measured devices show negligible hysteresis, likely because SiO_x defects appear at energies above the monolayer MoS_2 conduction band.[25] Here, we observe that while *SS* remains relatively unchanged in the long channel regime ($L > 1$ μm), *SS* increases at shorter channel lengths ($L < 1$ μm) which is caused by lateral field penetration through the thick back-gate dielectric (here 90 nm of SiO_2). This is consistent with previous observations on fully depleted silicon-on-insulator transistors.[24]

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