Compact Model for Carbon Nanotube Field-Effect Transistors Including Nonidealities and Calibrated With Experimental Data Down to 9-nm Gate Length

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***Abstract*— A semianalytical carbon nanotube field-effect transistor (CNFET) model based on the virtual-source model is presented, which includes series resistance, parasitic capacitance, and direct source-to-drain tunneling leakage. The model is calibrated with recent experimental data down to 9-nm gate length. Device performance of 22- to 7-nm technology nodes is analyzed. The results suggest that contact resistance is the key performance limiter for CNFETs; direct source-to-drain tunneling results in significant leakage due to low effective mass in carbon nanotubes and prevents further downscaling of the gate length. The design space that minimizes the gate delay in CNFETs subject to OFF-state leakage current (I_{OFF}) constraints is explored. Through the optimization of the length of the gate, contact, and extension regions to balance the parasitic effects, the gate delay can be improved by more than 10% at 11- and 7-nm technology nodes compared with the conventional 0.7× scaling rule, while the OFF-state leakage current remains below 0.5 μA/μm.**

***Index Terms*— Carbon nanotube (CNT), carbon nanotube field effect transistor (CNFET), contact resistance, direct source-to-drain tunneling.**

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I. Introduction

CARBON nanotube field-effect transistors (CNFETs) are among the most promising candidates to replace Si CMOS technology toward the 7-nm node and beyond [1], [2]. Carbon nanotubes (CNTs) provide high carrier velocity, quasi-ballistic transport, and inherent quasi-one-dimensional (1-D) nanometer-scale (<2 nm) structure. Numerous CNFET demonstrations have been made recently [3]: highly aligned CNTs grown on full wafer scale [4], complex logic gates [5], [6], stable complementary n- and p-channel transistors on the same chip [7]–[10], and operation at 0.4-V power supply [11], and CNFETs have been shown to outperform the best Si transistors for low-power applications [12]. These device/technology and circuit design advances [13] further strengthen the leading position of CNFETs as a promising candidate to complement Si CMOS in future technology nodes.

A computationally efficient compact model for the CNFET is indispensible for the design of large-scale circuit and for estimating and optimizing the performance of CNFET circuits for future technology nodes. Most published compact models focus on the intrinsic properties of CNFETs [14]–[17], with only a few exceptions accounting for the parasitic capacitances [18]. However, beyond the 22-nm technology node, extrinsic components become important and careful optimization to balance the tradeoffs is required [19], [20]. Tunneling is another obstacle to the advance of transistor scaling. Direct source-to-drain tunneling has been found significant when the gate length is scaled down to sub-10 nm [21]–[23], from both experimental and simulation perspectives. Numerical simulation using the nonequilibrium Green's function (NEGF) formalism [24], [25] provides physically sound means, but is too computationally expensive for device optimization and circuit simulation. Therefore, it is essential to develop a compact CNFET model capturing both the parasitic effects and the tunneling current.

In this paper, we demonstrate a compact CNFET model that is based on the virtual-source (VS) model. The VS model is a semiempirical model applicable to MOSFETs and relies on a large amount of reproducible data to extract empirical parameters such as mobility and inverse subthreshold slope (SS). For emerging devices such as the CNFET,

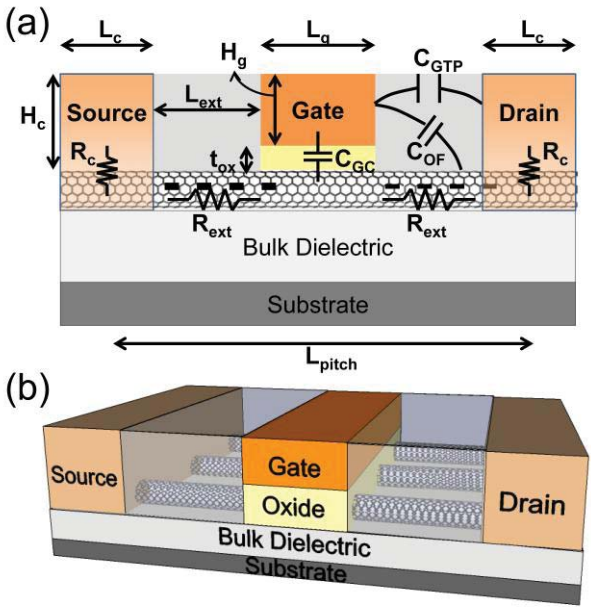

Fig. 1. CNFET structrue with planar top gate and multiple CNTs in the channel. (a) Lengthwise cut view. (b) 3-D view.

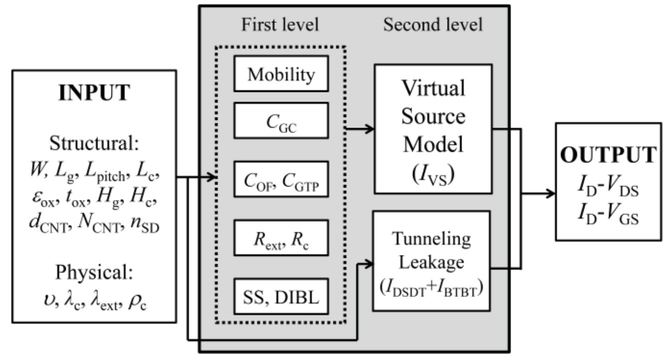

Fig. 2. Hierarchical structure of the CNFET model. The inputs are the design and physical parameters labeled in Fig. 1(a).

it is difficult to obtain large amounts of reliable data, yet there is a strong need for a realistic model to assess their potential for future use. In our proposed model, we relate the empirical parameters, as much as possible, with the device structures such as gate length and contact length to enable projections that reflect changes in the device design, while the other parameters are extracted from a few sets of experimental data. This model captures CNFET's physical properties such as diameter-dependent tunneling and CNT–metal contact resistance, which are important for the purpose of performance benchmarking, projection, and circuit design and optimization.

The VS model is one of the components of this hierarchical model. While each of the constituent components have been published by authors before, the constituent components do not lend themselves to gaining physical insights into how to optimize the CNFET and how to use them for design optimization and circuit simulation. The way the constituent models are put gather is the main contribution of this paper.

This paper is organized as follows. In Section II, each level of the model is described. Calibration with experimental data from 300-nm down to 9-nm gate length is presented in Section III. Based on the parameters extracted from Section III, the performances of 22- to 7-nm technology nodes are projected and the challenges related to parasitic effects and direct tunneling are highlighted in Section IV. Finally, Section V illustrates the use of the model for device the optimization of CNFETs at the 11- and 7-nm technology nodes.

II. CNFET MODEL

Fig. 1 illustrates the modeled device structure. It is a planar top-gated CNFET with an undoped CNT channel and ungated, highly-doped source/drain (S/D) extensions. A single CNFET contains multiple CNTs in parallel within the channel to boost the drive current. The ungated S/D extensions can offset the gate electrode from the S/D contact plugs and reduce the parasitic capacitance [27]. Present experimental CNFETs often employ a back gate with gate-to-S/D overlap [28], [29] or undoped (not intentionally doped), underlapped, and ungated extension regions [30], because a stable and well-controlled CNT doping technology is not yet available. However, it is well known that the structure in Fig. 1 can achieve better device performance with CMOS-compatible fabrication [31], [32] due to its effectiveness in reducing parasitic capacitances.

The model takes the CNFET structure design and physical parameters as inputs. The design parameters include the device pitch (L_{pitch}), length of the gate (L_g) and the contact (L_{c}), the gate width (W), the dielectric constant (ε_{ox}) and thickness (t_{ox}) of the gate oxide, the height of the gate (H_g) and the S/D contact plugs (H_c), the CNT diameter (d_{CNT}), the CNT density (N_{CNT}), and the doping density at the extensions (n_{SD}). d_{CNT} is an intrinsic physical property of the CNT. The bandgap of the semiconducting CNT can be approximated by $E_g \approx 2\gamma a_{\text{CC}}/d_{\text{CNT}}$ [33], where $a_{\text{CC}} \approx 1.42$ Å is the length of carbon–carbon bonds, and $\gamma \approx 3$ eV is the nearest-neighbor overlap energy that is used as a fitting parameter in the tight-binding method. The physical parameters are the velocity at the VS (υ), the carrier mean free paths in the CNTs (denoted by λ_c and λ_{ext} for the parts under the S/D metal contacts and extensions, respectively), and the specific contact resistance of the metal–CNT contact (ρ_c), all of which can be extracted from the experiments.

The hierarchical structure of the model is shown in Fig. 2. The first level is composed of models for the intrinsic and extrinsic components including the mobility, gate-to-channel capacitance, series resistances, parasitic capacitances, SS and drain-induced-barrier-lowering (DIBL) coefficient. The second level has two models: 1) the VS model utilizing the outputs of the first level to generate the thermionic emission current I_{VS} and 2) a semianalytical model for the tunneling current I_{TUNNEL}. The final output drain current is given by $I_{\text{D}} = I_{\text{VS}} + I_{\text{TUNNEL}}$. The details of each part are described below.

A. Models for Intrinsic and Extrinsic Components

1) Mobility (μ): We employ an experimentally corroborated physics-based mobility model for CNTs that applies both to the diffusive and quasi-ballistic transport regimes [34], taking into account the acoustic phonon (AP) and optical phonon (OP) scattering.

$$\mu = \frac{4qL_g}{hn}\sum_i \int_0^\infty \frac{\lambda(E)}{L_g+\lambda(E)}\left(-\frac{\partial f}{\partial E}\right)dE \tag{1a}$$

$$\frac{1}{\lambda} = \frac{1}{\lambda_{\mathrm{AP}}(E,T)} + \frac{1-f\left(E+\hbar\omega_{\mathrm{OP}}\right)}{\lambda_{\mathrm{OP,abs}}(E,T)} + \frac{1-f\left(E-\hbar\omega_{\mathrm{OP}}\right)}{\lambda_{\mathrm{OP,ems}}(E,T)} \tag{1b}$$

where n is the charge density, f is the Fermi–Dirac distribution, i is the summation index over the first and second subbands, $\hbar\omega_{\mathrm{OP}} \approx 0.18$ eV is the OP energy, λ_{AP}, $\lambda_{\mathrm{OP,abs}}$, and $\lambda_{\mathrm{OP,ems}}$ are mean free paths for AP scattering, OP absorption, and emission, respectively, which depend on the energy and the temperature. Low-field mobility at a charge density of $n = 0.01\ \mathrm{nm}^{-1}$ is used in the model. Because λ_{AP}, $\lambda_{\mathrm{OP,abs}}$, and $\lambda_{\mathrm{OP,ems}}$ are proportional to d_{CNT} [34], [35], μ increases when d_{CNT} increases.

2) Gate-to-Channel Capacitance (C_{GC}): Analytical expression of C_{GC}, including the screening effects between multiple CNTs under a single planar gate, has been derived in [36], and the details are presented in the Appendix. C_{GC} is one of the most important factors determining the drive current because it is proportional to the amount of carriers induced by the gate electric field.

3) Series Resistances (R_{S}): The series resistance R_{s} has two components, one being the resistance of the ungated S/D extensions (R_{ext}) [37].

$$R_{\mathrm{ext}} = L_{\mathrm{ext}}/(\lambda_{\mathrm{ext}}G_{\mathrm{1D}}), \quad G_{\mathrm{1D}} = \frac{4q^2}{h}\frac{e^{\Delta/kT}}{1+e^{\Delta/kT}} \tag{2}$$

where $\Delta \equiv E_{\mathrm{FS}} - E_{\mathrm{C}}\ (E_{\mathrm{V}})$ for n-type (p-type) CNFETs, and E_{FS} is the Fermi level at the S/D extensions related to the doping density n_{SD}. When the CNTs are highly doped, $1/G_{\mathrm{1D}} \approx 4q^2/h \equiv R_Q = 6.45\ \mathrm{k}\Omega$ is the quantum resistance for CNTs with two-band degeneracy. The other component is the contact resistance (R_c) between the CNTs and metal contacts [38].

$$R_c = \sqrt{\frac{1}{4}+\frac{\rho_{\mathrm{C}}}{\lambda_c R_Q}}\,R_Q \coth\left(\sqrt{\frac{R_Q}{\rho_c\lambda_c}+\frac{R_Q^2}{4\rho_c^2}}\,L_c\right) \tag{3}$$

where ρ_c is equivalent to the reciprocal of the contact conductance g_c in [38]. Note that ρ_c here is different from the conventional contact resistivity for Si MOSFETs. In the transmission line model, $1/\rho_c$ is the conductance per unit length along the CNT. When L_c is smaller than the transfer length, $R_c \approx R_Q/2 + \rho_c/L_c$. The total parasitic resistance for a single CNT is the sum of these two, that is, $R_{\mathrm{s}} = R_{\mathrm{ext}} + R_c$.

4) Parasitic Capacitances (C_{P}): The parasitic capacitance of a CNFET consists of two components: the outer-fringe capacitance (C_{OF}) between the gate and the CNTs in the S/D extensions, and the gate-to-plug capacitance (C_{GTP}) between the gate and the S/D contact plug [36]. The details are described in the Appendix.

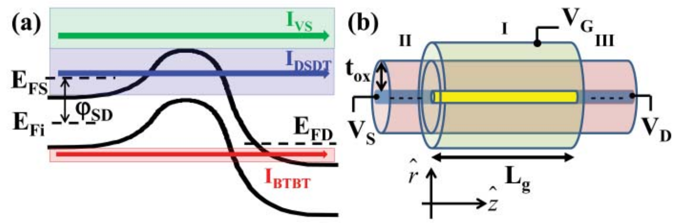

Fig. 3. (a) Band diagram to illustrate the tunneling current. (b) Gate-all-around cylindrical structure used to model the potential profile. The source and drain extensions are highly doped.

5) SS and DIBL Coefficient δ: SS and DIBL coefficient δ are calculated by the ratio of the capacitances coupling to the VS in the channel [39].

$$SS = \ln(10)\frac{kT}{q}\left(\frac{C_{\mathrm{GC}}+C_{\mathrm{S}}+C_{\mathrm{D}}}{C_{\mathrm{GC}}}\right) \tag{4a}$$

$$\delta = C_{\mathrm{D}}/(C_{\mathrm{GC}}+C_{\mathrm{S}}+C_{\mathrm{D}}) \tag{4b}$$

where C_{GC}, C_{S}, and C_{D} are capacitances coupling from the gate, source, and drain to the channel, respectively. The models of C_{S} and C_{D} are verified by Maxwell 3-D [40], and the details are in the Appendix. This model can be easily applied to other structures as long as appropriate models for C_{GC}, C_{S}, and C_{D} are used.

B. VS Model

The VS model is a semiempirical model applicable to short-channel MOSFETs in all regions of operation, from ballistic transport to diffusive velocity saturation [26]. The inputs of the VS model include: v, μ, SS, δ, R_{s}, and C_p. v can be extracted from experimental data and will be discussed in Section III. μ, SS, δ, R_{s}, and C_p are calculated from the models in Section II-A.

There are two fitting parameters in the VS model, α and β, which model the channel charge from weak to strong inversion and the transition from linear to saturation region, respectively. As a start, the values $\alpha = 3.5$ and $\beta = 1.4$, borrowed from Si MOSFETs, are used. More experiments are required to determine the specific α and β for CNFETs.

With all the inputs of the VS model calculated appropriately in Section II-A and the two fitting parameters empirically set, the VS current can be generated.

C. Tunneling Leakage Current

Two tunneling mechanisms are modeled as illustrated in Fig. 3(a): direct source-to-drain tunneling current (I_{DSDT}) from the source conduction band (CB) into the drain CB, and the band-to-band tunneling (BTBT) from the source valence band into the drain CB.

To evaluate the tunneling probability, knowing the band profile along the channel is indispensable. In this paper, we employ a gate-all-around (GAA) cylindrical structure as illustrated in Fig. 3(b) to derive a semianalytical model for the band profile as an estimation of the impact of I_{DSDT}, because a planar CNFET structure like that in Fig. 1 has no analytical solution. The CNT is divided into the channel region and extension regions denoted by I, II, and III in Fig. 3(b). In the subthreshold region, mobile charge is negligible and the surface potential in region I is approximated as the solution to the Laplace's equation in cylindrical coordinates [41].

$$\phi_{\mathrm{I}}(z) \approx J_0(\xi_0)\left[C_1 \exp(z/\Lambda) + C_2 \exp(-z/\Lambda)\right] + V_{\mathrm{CNT}} \tag{5a}$$
$$C_2 = \frac{(V_{\mathrm{bi}} - V_{\mathrm{CNT}})\left(e^{L_g/\Lambda} - 1\right) - V_{\mathrm{DS}}}{2J_0(\xi_0)\sinh\left(L_g/\Lambda\right)}$$
$$C_1 = \frac{V_{\mathrm{bi}} - V_{\mathrm{CNT}}}{J_0(\xi_0)} - C_2$$
$$\frac{Y_0'(\xi_0)}{J_0'(\xi_0)} = \kappa_e \frac{Y_0(\xi_0)}{J_0(\xi_0)} + (1-\kappa_e)\frac{Y_0(\xi_0 + t_{\mathrm{ox}}/\Lambda)}{J_0(\xi_0 + t_{\mathrm{ox}}/\Lambda)} \tag{5b}$$

where J_0 and Y_0 are Bessel functions of the first and second kinds, respectively, $\xi_0 = d_{\mathrm{CNT}}/2\Lambda$, Λ is the scale length given in (5b) to satisfy the continuity of perpendicular component of electric field at the CNT/dielectric interface. $\kappa_e = \varepsilon_{\mathrm{CNT}}/\varepsilon_{\mathrm{OX}}$ is the ratio of the dielectric constant of CNT to the gate oxide. In this paper, $\varepsilon_{\mathrm{CNT}} = 1$ and $\varepsilon_{\mathrm{OX}} = 16$ are chosen. C_1 and C_2 are coefficients determined by the boundary conditions $\phi_{\mathrm{I}}(0) = V_{bi}$ and $\phi_I(L_g) = V_{bi} + V_{\mathrm{DS}}$ and V_{bi} is the built-in potential proportional to $E_{\mathrm{Fi}} - E_{\mathrm{FS}}$. The reference point is chosen at $E_{\mathrm{FS}} = 0$ so that the intrinsic Fermi level is equal to $-q\phi_{\mathrm{I}}(z)$. To account for the mobile charge induced by the gate, V_{CNT} is introduced as the actual voltage dropped on CNTs satisfying

$$V_{\mathrm{GS}} - V_{\mathrm{FB}} = qn/C_{\mathrm{ox}} + V_{\mathrm{CNT}}$$
$$n = n_i \exp\left[\frac{-\phi_I(z_{\max})}{kT/q}\right], \quad z_{\max} = \frac{\Lambda}{2}\ln\frac{C_2}{C_1}$$
$$n_i = 4\sqrt{kT \cdot E_g}/(3\sqrt{\pi}a_{\mathrm{CC}}\gamma)\cdot\exp\left(-E_g/(2kT)\right)$$
$$C_{\mathrm{ox}} = 2\pi\varepsilon_{\mathrm{ox}}/\ln\left[(d_{\mathrm{CNT}} + 2t_{\mathrm{ox}})/d_{\mathrm{CNT}}\right] \tag{6}$$

where V_{GS} and V_{FB} are the gate and flat-band voltages, respectively, and $z_{\max}$ corresponds to the position of the band maximum in the channel. Derivation of the CNT intrinsic carrier density n_i was elucidated in [42].

At the junctions of the channel and the S/D extensions, the electric field does not terminate abruptly but penetrates into the extensions, leading to a tail in the band profile [43] and affects I_{DSDT}. In this paper, we use an exponential function to phenomenologically model the descending potential in the S/D extensions.

$$\phi_{\mathrm{II}}(z) = \left[\phi_{\mathrm{I}}(0) - \frac{\varphi_{\mathrm{SD}}}{q}\right]\exp\left[\frac{\partial\phi_{\mathrm{I}}(0)/\partial z}{\phi_{\mathrm{I}}(0) - \phi_{\mathrm{S}}}z\right] + \frac{\varphi_{\mathrm{SD}}}{q} \tag{7a}$$
$$\phi_{III}(z) = \left[\phi_I(L_{\mathrm{G}}) - \frac{\varphi_{\mathrm{SD}}}{q} - V_{\mathrm{DS}}\right] \exp\left[\frac{\partial\phi_I(L_g)/\partial z}{\phi_I(L_g) - \varphi_{\mathrm{SD}}/q - V_{\mathrm{DS}}}z\right] + \frac{\varphi_{\mathrm{SD}}}{q} + V_{\mathrm{DS}} \tag{7b}$$

where $\varphi_{\mathrm{SD}} = E_{\mathrm{FS}} - E_{\mathrm{Fi}}$, and E_{Fi} is the intrinsic Fermi level. Equation (8) links the band profile in regions I, II, and III smoothly.

Given the potential profile, I_{DSDT} in the ballistic transport regime can be evaluated as [44]

$$I_{\mathrm{DSDT}} = \frac{4q}{h}\int_{E_g/2-\varphi_{\mathrm{SD}}}^{E_g/2-q\phi(z_{\max})} T(E)\left[f(E, E_{\mathrm{FS}}) - f(E, E_{\mathrm{FS}} - qV_{\mathrm{DS}})\right]dE \tag{8}$$

where the prefactor of four arises from the double degeneracy of the first sub-band and electron spin. The tunneling probability $T(E)$ is calculated by the transfer matrix method [45] that takes the band profiles calculated in (6) and (8) as inputs. More details of the calculation of tunneling probability and analytical expressions of band profile will be discussed in a later publication.

BTBT current (I_{BTBT}) is calculated by the Wentzel–Kramers–Brillouin (WKB) method using the triangular barrier approximation [46].

$$I_{\mathrm{BTBT}} \approx \frac{4q}{h}kT \cdot T_{\mathrm{WKB}}\left[\ln\frac{e^{(E+qV_{\mathrm{DS}})/kT} + 1}{e^{E/kT} + 1}\right]_{-qV_{\mathrm{DS}}-\varphi_{\mathrm{SD}}+E_g/2}^{-\varphi_{\mathrm{SD}}-E_g/2}$$
$$T_{\mathrm{WKB}} \approx \exp\left[-\frac{\pi}{4}\cdot\frac{E_g^2}{\hbar v_{\mathrm{F}} qF}\right] \tag{9}$$

where $v_F \sim 10^6$ m/s is the Fermi velocity, F is the electric field in the junction at the drain calculated from $\partial\phi/\partial z$ in (7b). T_{WKB} in (9) is a result of the hyperbolic band structure of CNTs and is different from the bulk semiconductors such as silicon or germanium. It is worth noting that phonon-assisted tunneling [47] is not yet included in the model and remains a subject for future works. Therefore, only when $V_{\mathrm{DS}} > E_g$, can I_{BTBT} be appreciable.

I_{TUNNEL} is simply the sum of I_{DSDT} and I_{BTBT} and is superimposed on I_{VS} obtained in Section II-B by matching the threshold voltage (V_{T}), which is defined as the V_{GS} for which the derivative of transconductance $\partial g_m/\partial V_{\mathrm{GS}}$ is a maximum [48]. Although the device configuration used to derive the tunneling leakage is different from the planar structure in Fig. 1, it provides an efficient and physically logical means to capture the impact of tunneling for the scaled CNFETs.

The modeled I_{DSDT} is compared to an open-source simulator which solves the Poisson and Schrödinger equations self-consistently using the NEGF formalism and calculates the current in ballistic transport regime in CNFETs with a GAA cylindrical geometry and doped S/D extensions [25]. Fig. 4 shows the comparison of the band profile as well as I_{DSDT} obtained from the model and the NEGF simulation. In Fig. 4(a) and (b), the potential tails in the S/D extensions broaden the tunneling barrier width. Good agreement between the modeled I_{DSDT} and the numerical simulation is observed when high-k dielectric is used ($\varepsilon_{\mathrm{ox}} > 8$) as shown in Fig. 4(c) and (d).

III. Model Calibration With Experiments

The CNFET model is fitted to the latest experimental *I–V* characteristics for long-channel ($L_g = 300$ nm and $L_c = 100$ nm) and short-channel ($L_c = 20$ nm, $L_c = 20$ nm and $L_g = 9$ nm, and $L_c = 200$ nm) CNFETs [28], [29].

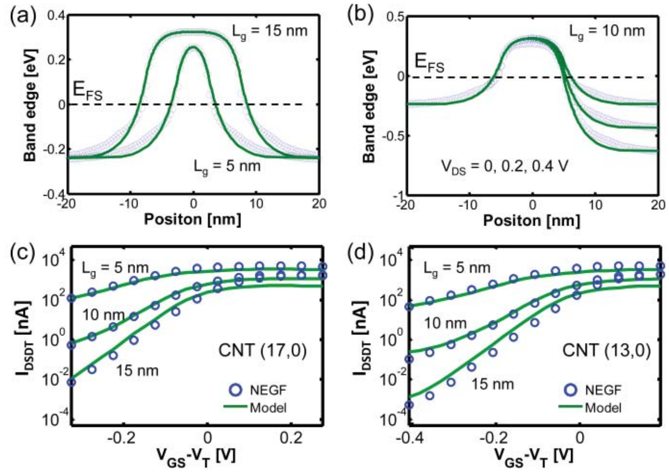

Fig. 4. Comparison of the band profile and direct source-to-drain tunneling current between the semianalytical model and the numerical NEGF simulation. $t_{ox} = 3$ nm, $\varepsilon_{ox} = 16$, and the doping density at the S/D extensions $n_{SD} = 1$ nm^{-1} are used. (a) $V_{DS} = 0$ V. (b) $V_{GS} = 0$ V. (c) CNT chirality (17, 0) corresponding to $E_g = 0.66$ eV. (d) CNT chirality (13, 0) correspoding to $E_g = 0.86$ eV. $V_{DS} = 0.4$ V for both (c) and (d).

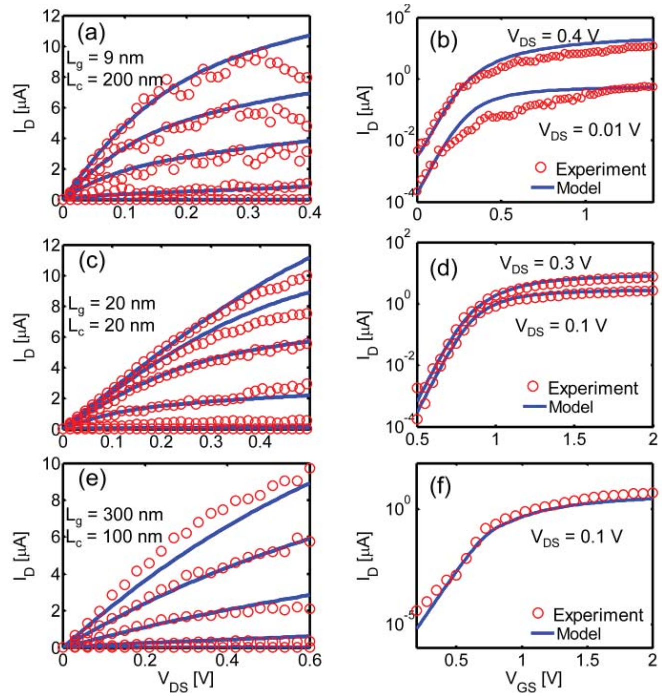

Fig. 5. Comparison of I_D–V_{DS} and I_D–V_{GS} between the experiments and the model. (a) I_D–V_{DS} and (b) I_D–V_{GS} for $L_g = 9$ nm and $L_c = 200$ nm. (c) I_D–V_{DS} and (d) I_D–V_{GS} for $L_g = 20$ nm and $L_c = 20$ nm. (e) I_D–V_{DS} and (f) I_D–V_{GS} for $L_g = 300$ nm and $L_c = 100$ nm.

Tunneling model is not included in the calibration, as the tunneling current is not significant in the experimental data. $d_{CNT} = 1.2$–1.4 nm was observed in all the devices. Thus, an average of $d_{CNT} = 1.3$ nm is used in the model when fitting to the data, which corresponds to $E_g \approx 0.66$ eV. The calibrated I–V curves along with the experimental data are shown in Fig. 5. The signs of V_{GS} and V_{DS} are flipped over to make the device plots n-type-like for convenience. A local bottom gate was utilized to modulate the carriers in the CNTs, which is different from the modeled structure shown in Fig. 1. Thus, the intrinsic capacitance C_{GC} of the back-gated structure is obtained from TCAD Sentaurus [49] and serves as the input. Because of the device structure difference between the experimental device and the model, SS and DIBL are not calculated from (4) and (5) but remain as fitting parameters. To accommodate the notable hysteresis observed in the experiments, the V_T in the I_D–V_{DS} characteristics is shifted by a constant value (≤ 0.2 V) compared with the V_T extracted from I_D–V_{GS} characteristics. Finally, the parasitic resistance is purely the contact resistance, since there are no S/D extensions in the experimental devices.

The VS velocity υ, an empirical parameter to the VS model, and ρ_c and λ_c of the contact resistance model as in (3) are extracted by tuning these parameters to match the experimental data. $\upsilon = 3 \times 10^5$ m/s, $\rho_c = 420$ kΩ·nm, and $\lambda_c = 250$ nm are obtained from the calibration. It is worth noting that the υ is proportional to the saturation current at high V_{GS}, and ρ_c determines how fast the R_c increases with the shrinking L_c. A large ρ_c leads to large R_c and less steep slope in the I_D–V_{DS} characteristics. The diameter-normalized contact resistivity is $\rho_c . d_{CNT} = 546$ kΩ·nm^2, a little higher than the one reported in [28]. Because the devices used for calibration have no extension regions, λ_{ext} cannot be extracted and is assumed to be equal to λ_c. When the technology for CNT doping is better developed, λ_{ext} can be characterized more accurately.

TABLE I
CNFET STRUCTURE PARAMETERS: 22- TO 7-nm NODES

Technology Node	22-nm	14-nm	11-nm	7-nm
L_{pitch} [nm]	80–100	56–70	40–55	30–40
L_g [nm]	25–28	18–20	13–15	10–12
L_c [nm]	26	18	12	10
EOT [nm]	1	0.9	0.8	0.7
H_g [nm]	30	20	20	15
W [nm]	160	112	90	63

IV. IMPACT OF PARASITICS AND TUNNELING

With the model validated by experimental data from $L_g =$ 300 to 9 nm, next, we explore the impact of these nonidealities on the device characteristics of CNFETs for the future technology nodes. Projected device dimensions at each technology node are listed in Table I [50], [51]. The other parameters are: 1) n_{SD} is assumed to be 1 nm^{-1}, corresponding to 0.6% free carriers per carbon atom for the CNTs with diameter ~1.3 nm; 2) V_{DD} is fixed at 0.6 V as a basis for comparison; 3) CNT density is assumed to be $N_{CNT} = 250/\mu$m with equal spacing in order to compete with the Si technology [32]; 4) V_T is designed to achieve tolerable OFF-state leakage current ($I_{OFF} \leq 0.5$ μA/μm at $N_{CNT} = 250/\mu$m defined as I_D at $V_{GS} = 0$ and $V_{DS} = V_{DD}$); 5) to be concise, the S/D contact plugs are assumed to be as high as the gate, that is, $H_c = H_g$. The influence of different H_cs are discussed in [19] and it is shown that C_{GTP} is limited by H_g; and 6) the material is the bulk dielectric, the spacers have dielectric constant $\varepsilon = 3.9$, and a high-k material with $\varepsilon_{ox} = 16$ is used as the gate oxide. A mean value is used for the analysis if the

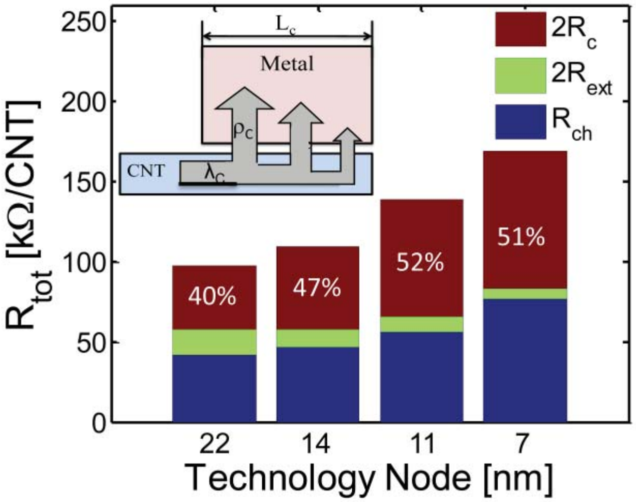

Fig. 6. Composition of the CNFET resistances at different technology nodes. R_c contributes to most of the resistance. Inset: two conduction mechanisms in the CNT/metal contact: carrier injection from CNT to metal characterized by ρ_c and carrier transport in the CNT characterized by λ_c.

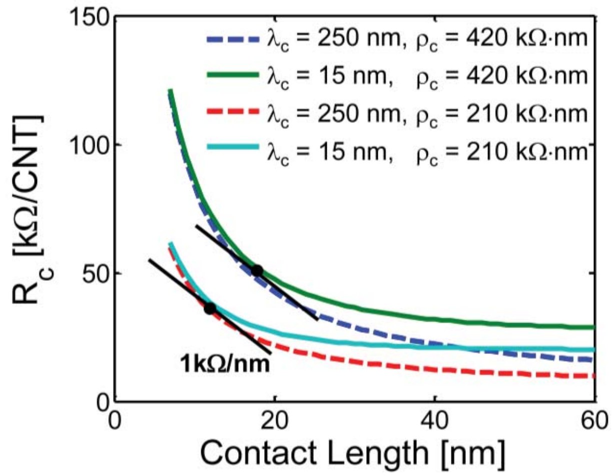

Fig. 7. R_c versus L_c at different λ_c and ρ_c. When $L_c < 20$ nm, R_c increases dramatically as L_c decreases. The starting point of the "short contact regime" is marked at where the $dR_c/dL_c = 1$ kΩ/nm.

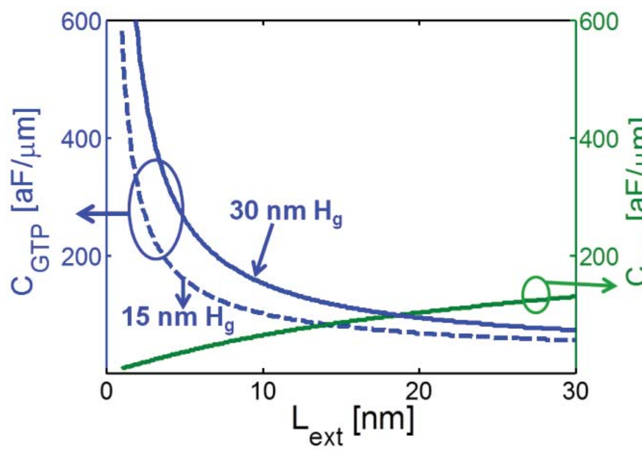

Fig. 8. Parasitic capacitances C_{GTP} and C_{OF} versus L_{ext}. The total parasitic capacitance increases rapidly when $L_{\mathrm{ext}} < 10$ nm. Lowering the height of the gate and contact plugs can reduce C_{GTP} and improve the performance.

projected number in Table I is in a certain range, for example, $L_{\mathrm{pitch}} = 0.5 \times (30 + 40) = 35$ nm for the 7-nm technology node. Following the definition in Fig. 1(a), L_{ext} is equal to $0.5\times$ $(L_{\mathrm{pitch}} - L_c - L_g)$. Section IV-A to IV-C examines the impact of series resistance, parasitic capacitance, and tunneling leakage current on the CNFET's performance, as the feature size is scaled down.

A. Series Resistance

Series resistance increases rapidly with the downscaling of device dimensions and becomes dominant starting from the 11-nm technology node as shown in Fig. 6. The channel resistance is calculated by $R_{\mathrm{ch}} = R_{\mathrm{tot}} - 2R_{\mathrm{ext}} - 2R_c$, where R_{tot} is the total resistance in the on-state, that is, $R_{\mathrm{tot}} = V_{\mathrm{DD}}/I_{\mathrm{ON}}$. R_{ch} increases with the technology nodes, because higher V_{T} is required to keep I_{OFF} low due to increasing SS. Unlike Si MOSFETs in which the parasitic capacitance is the limiting factor for advanced technology nodes [19], today's CNFETs are more limited by the CNT-to-metal contact resistance [52].

As described in Section II, the series resistance is composed of the extension resistance R_{ext} and the contact resistance R_c. R_{ext} is proportional to the ratio of L_{ext} to the mean free path λ_{ext}, while the contact resistance has a more complex dependence on the physical parameters and the contact length. The physics that determine the resistance of the CNT/metal contact are: 1) carrier injection from CNT to metal, whose rate is proportional to $1/\rho_c$, and (2) carrier transport in the CNTs that are covered by the contact metal, which is characterized by λ_c. In the quasi-ballistic regime, $1/\lambda_c$ is the scattering probability in CNTs per unit length and is highly dependent on the CNT growth and doping conditions. A wide range of λ_c from 20 to 380 nm has been reported in [38] and [53]. A pessimistic estimation of $\lambda_c = 15$ nm is used in the following analysis. Because of the distributed nature of the CNT–metal interface, R_c decreases with a hyperbolic cotangent dependence on L_c [54], as shown in Fig. 7, with the lower bound equal to the quantum resistance. The first derivative of R_c with respect to L_c reaches 1 kΩ/nm when $L_c < 20$ nm, demarcating the region where the R_c starts to shoot up. This is a manifestation of the "short contact regime" where R_c starts to increase drastically with decreasing L_c. At 7-nm node with $L_c = 10$ nm, ρ_c has to be reduced to 120 kΩ·nm in order to achieve $2R_c < 0.3R_{\mathrm{tot}}$, around 30% of its original value.

B. Parasitic Capacitance

The ratio of intrinsic capacitance C_{GC} to the parasitic capacitances (C_{OF} + C_{GTP}) decreases from 69% to 60% when scaling from 22-nm node to 7-nm node. Parasitic capacitances impose extra burdens on the device, which not only slow down the switching but also raise the dynamic power consumption. Both capacitances C_{OF} and C_{GTP} are functions of L_{ext} as shown in Fig. 8. As L_{ext} is shortened, C_{GTP} increases reciprocally due to stronger gate-to-plug coupling, while C_{OF} decreases proportionally with L_{ext}. C_{GTP} and C_{OF} intersect around $L_{\mathrm{ext}} = 20$ nm at $H_g = 30$ nm. Beyond

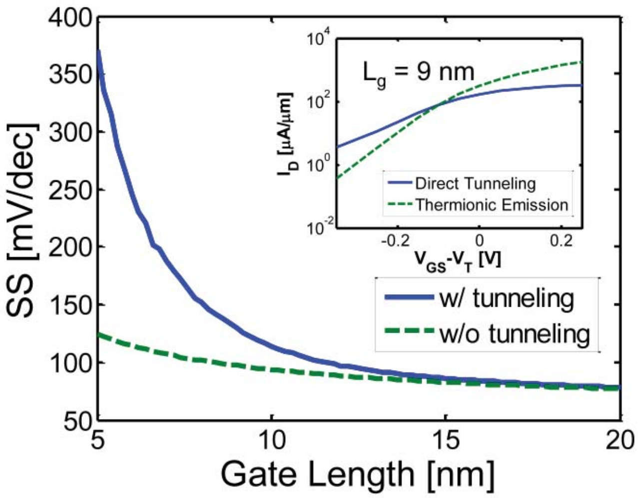

Fig. 9. Inverse subthreshold slope versus gate length. The inset shows the dominance of direct source-to-drain tunneling current in subthreshold region resulting in severe degradation in SS when $L_g < 10$ nm.

this point toward the left, C_{GTP} dominates, and the total parasitic capacitance increases drastically. Reduction in H_g can effectively reduce C_{GTP} and push the intersection of C_{GTP} and C_{OF} toward the left allowing further scaling of L_{ext}. Another benefit of shortening L_{ext} is to reduce one of the series resistances R_{ext}. Therefore, there is a tradeoff between parasitic capacitance and series resistance.

C. Tunneling Leakage Current

Direct source-to-drain tunneling becomes significant when the gate length is very short. As shown in the inset of Fig. 9, I_{DSDT} dominates over thermionic emission current when the gate length is scaled down to 9 nm and beyond. SS is thus deteriorated with decreasing L_g. Note that the calculation of I_{DSDT} in Fig. 9 is based on the GAA cylindrical structure. Whether direct source-to-drain tunneling was appreciable in [29] needs to be further investigated. It has been reported that the metal/CNT contacts also play an important role in the *I–V* characteristics and affect the SS because the contacts are modulated by the bottom gate [55]. Temperature-dependent measurements might be helpful to elucidate the impact of tunneling leakage current [23].

On the other hand, BTBT occurs when the drain bias (V_{DS}) is larger than the bandgap or the barrier is raised so high by the gate voltage that the valence band in the channel is lifted above the CB at the source. To avoid BTBT, CNTs with smaller diameters are preferred due to larger bandgap as well as lower tunneling probability.

V. Design Space and Structure Optimization

The primary driver for technology scaling is to reduce cost by shrinking the device pitch L_{pitch}, which is equal to $(L_c + 2L_{\mathrm{ext}} + L_g)$. The effects of scaling the individual components have been discussed in Section IV: parasitic resistances, capacitances, and tunneling leakage current increase drastically as L_c, L_{ext}, and L_g are scaled down, respectively.

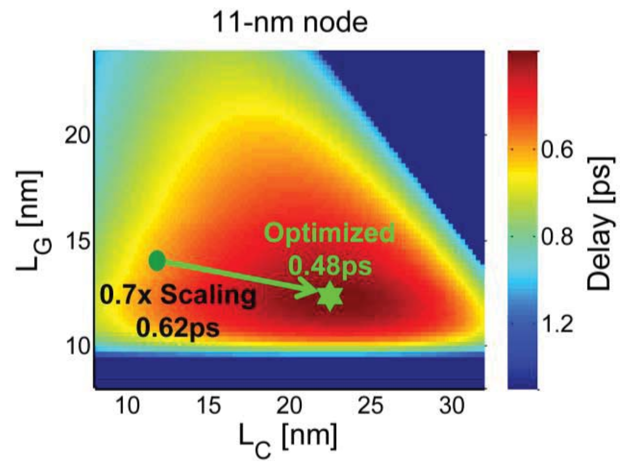

Fig. 10. Optimization at the 11-nm node ($L_{\mathrm{pitch}} = 47.5$ nm). The dark blue regions represent the forbidden designs due to intolerable I_{OFF} (>0.5 μA/μm) or $L_{\mathrm{ext}} < 1$ nm. The delay can be greatly reduced by increasing L_c (or reducing R_c).

It is essential to investigate the tradeoffs between them. In this section, we optimize the ratio of L_c, L_{ext}, and L_g with fixed L_{pitch} for the 11- and the 7-nm technology node to minimize the gate delay as a demonstration of the model's capability. As a metric for the device performance, the gate delay is defined as $\tau = C_{\mathrm{IN}}V_{\mathrm{DD}}/I_{\mathrm{ON}}$, where $C_{\mathrm{IN}} = C_{\mathrm{GC}} + C_{\mathrm{GS}} + 2C_{\mathrm{GD}} = C_{\mathrm{GC}} + 3(C_{\mathrm{OF}} + C_{\mathrm{GTP}})$ including the Miller effect. The threshold voltage V_{T} is determined by maximizing I_{ON} under the constraint of $I_{\mathrm{OFF}} \leq 0.5$ μA/μm at $N_{\mathrm{CNT}} = 250/\mu$m. Using this model, one can, for example, explore the interaction between the nanotube diameter and the leakage current; the interplay between the contact resistivity, contact length, and device pitch; the selection of the proper work function for the gate electrode; and the choice of the power supply voltage. These explorations will be part of a future study to examine the energy–delay tradeoffs for CNFET device/circuit co-optimization.

The CNFET dimensions can be found in Table I. L_{pitch} is restrained at 47.5 nm for the 11-nm node and 35 nm for the 7-nm node. The optimization result and the explored design space for the 11-nm node is shown in Fig. 10. The dark blue regions represent the forbidden designs due to I_{OFF} constraints ($I_{\mathrm{OFF}} > 0.5$ μA/μm) or impractical device structure ($L_{\mathrm{ext}} <$ 1 nm). Compared with conventional $0.7\times$ scaling rules, τ is improved from 0.62 to 0.48 ps for the 11-nm node after the optimization of the ratio of the gate, contact, and extension lengths. For 7-nm node, τ is improved from 0.63 to 0.55 ps (explored design space is not shown here). Note that the optimized L_c is much larger than its original value (L_c = 12–23 nm for the 11-nm node and L_c = 10–15 nm for the 7-nm node), indicating the significance of reducing contact resistances. Assuming that ρ_c could be reduced by half (420–210 kΩ·nm), the optimized τ for the 7-nm node would be further reduced from 0.55 to 0.42 ps.

The major obstacle for L_g scaling is direct source-to-drain tunneling leakage that prevents L_g from scaling below 10 nm. Employing CNTs with a smaller diameter in a conventional CNFET can reduce the tunneling probability due to a larger bandgap at the cost of increasing effective mass. Constraint of

L_g scaling would be more rigorous when the process variation is included, and can also be evaluated by the model and alleviated by a careful design. Another information from the optimization of the 11- and 7-nm nodes is that the minimum gate delay is increased from the 11-nm node to the 7-nm node, contradicting the traditional Dennard-scaling expectation [56]. This occurs mainly because the decrease in the contact length greatly raises the contact resistance and reduces the drive current.

VI. Conclusion

In this paper, we introduced a compact, physical, and intuitive CNFET model capturing both intrinsic and extrinsic device properties, and the model could be implemented in SPICE or VerilogA. The model was calibrated with the latest experimental results from 300-nm down to 9-nm gate lengths. Based on the GAA cylindrical configuration, the irregular potential profile along the channel was modeled semianalytically, providing an efficient path to study the impact of the tunneling leakage current in the ultrascaled devices. Through careful optimization of the device structure, made possible by the use of this compact model, the impact of the extrinsic components could be alleviated, and the projected gate delay could be improved by more than 20%. From the exploration of the design space, we observed that: 1) contact resistance is the key limiter of the CNFET performance. Substantial improvement in delay can be achieved if ρ_c is reduced, showing the importance of improving the CNT–metal interface and 2) direct source-to-drain tunneling limits the downscaling of L_g. This result is believed to be universal in all kinds of FETs suggesting further study in material and device structure to minimize the tunneling current.

Appendix

The intrinsic and extrinsic capacitances are derived in [36]. The gate-to-channel capacitance C_{GC} including screening effects between multiple CNTs under a single planar gate is as shown in (A.1), where $C_{\mathrm{GC\_INF}}$, $C_{\mathrm{GC\_E}}$, and $C_{\mathrm{GC\_M}}$ are C_{GC} for single CNT and for CNTs at the edge and in the middle of the CNT array, respectively; $C_{\mathrm{GC\_SR}}$ is the equivalent series capacitance due to channel screening; s is CNT pitch; k_1 and k_2 are the relative permittivity of the oxide and substrate, respectively; ε_0 is the vacuum permittivity; r is the radius of CNT; and h is the distance between the center of CNT and the gate.

$$\begin{aligned}
C_{\mathrm{GC_E}} &= C_{\mathrm{GC_INF}} \cdot C_{\mathrm{GC_SR}} / (C_{\mathrm{GC_INF}} + C_{\mathrm{GC_SR}}) \\
C_{\mathrm{GC_M}} &= 2C_{\mathrm{GC_E}} - C_{\mathrm{GC_INF}} \\
C_{\mathrm{GC_SR}} &= \frac{4\pi k_1 \varepsilon_0 L_g}{\ln\left[\frac{s^2+2(h-r)(h+\sqrt{h^2-r^2})}{s^2+2(h-r)(h-\sqrt{h^2-r^2})}\right] + \lambda_1 \ln\left[\frac{(h+2r)^2+s^2}{9r^2+s^2}\right] \tanh\left(\frac{h+r}{s-2r}\right)} \\
C_{\mathrm{GC_INF}} &= \frac{4\pi k_1 \varepsilon_0 L_g}{\cosh^{-1}\left[(t_{\mathrm{OX}}+r)/r\right] + \lambda_1 \ln\left[(h+2r)/3r\right]} \\
\lambda_1 &= \frac{k_1 - k_2}{k_1 + k_2}
\end{aligned} \tag{A.1}$$

The outer-fringe capacitance (C_{OF}) between the gate and CNTs in the S/D extensions can be modeled as

$$\begin{aligned}
C_{\mathrm{OF_INF}} &= \pi k_2 \varepsilon_0 L_{\mathrm{ext}} / \cosh^{-1}\left(\sqrt{4h^2 + (0.56L_{\mathrm{ext}})^2}/2r\right) \\
C_{\mathrm{OF_E}} &= \pi k_2 \varepsilon_0 L_{\mathrm{ext}} / \ln\left[\sqrt{4h^2 + (0.56L_{\mathrm{ext}})^2 + s^2}/s\right] \\
&\quad + C_{\mathrm{OF_INF}}/\eta_1 \\
C_{\mathrm{OF_M}} &= (2\alpha/\eta_1) C_{\mathrm{OF_E}} + (1 - 2\alpha/\eta_1)\, C_{\mathrm{OF_INF}} \\
\eta_1 &= \exp\left(\frac{\sqrt{N_{\mathrm{CNT}}^2 - 2N_{\mathrm{CNT}}} + N_{\mathrm{CNT}} - 2}{\tau_1 N_{\mathrm{CNT}}}\right) \\
\alpha &= \exp\left(\frac{N_{\mathrm{CNT}} - 3}{\tau_2 N_{\mathrm{CNT}}}\right)
\end{aligned} \tag{A.2}$$

where $C_{\mathrm{OF\_INF}}$, $C_{\mathrm{OF,E}}$, and $C_{\mathrm{OF,M}}$ are C_{OF} for single CNT and for CNTs at the edge and in the middle of the CNT array, respectively. τ_1 and τ_2 are empirically set as 2.5 and 2, respectively.

The gate-to-plug capacitance (C_{GTP}) between the gate and the S/D contact plug is ($\alpha_{\mathrm{GTP\_SR}}$ is empirically set as 0.7).

$$\begin{aligned}
C_{\mathrm{GTP}} &= \frac{k_2 \varepsilon_0 H_g W}{L_{\mathrm{ext}}} + \frac{\alpha_{\mathrm{GTP_SR}} \pi k_2 \varepsilon_0 W}{\ln[2\pi(L_{\mathrm{ext}} + L_g)/(2L_g + \tau_{\mathrm{BK}} H_g)]} \\
\tau_{\mathrm{BK}} &= \exp\left(2 - 2\sqrt{1 + 2(H_g + L_g)/L_{\mathrm{ext}}}\right).
\end{aligned} \tag{A.3}$$

The capacitances coupling from the source (C_{S}) and drain (C_{D}) to the channel are modeled by conformal mapping [39].

$$\begin{aligned}
C_{\mathrm{S}} + C_{\mathrm{D}} &= (\pi/(2u) - 1)\, C_{\mathrm{GC}} \\
u &= \cos^{-1}(((a - (a^2 - 4)^{0.5})/2)^{0.5}) \\
a &= 2 + b(L_g/2t_{\mathrm{ox}})^2 \\
b &= 1.3 - 3.6\exp(-L_g/1.4d_{\mathrm{CNT}}).
\end{aligned} \tag{A.4}$$

The coefficients in (A.4) are determined by fitting to the numerical simulation results done by Maxwell 3-D [40]. For a CNFET with single CNT, $C_{\mathrm{S}}/C_{\mathrm{D}} = 3.4$ is extracted empirically.

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