nature nanotechnology

Article

https://doi.org/10.1038/s41565-026-02161-w

Scaling nanoribbon transistors with monolayer transition metal dichalcogenides

Received: 31 July 2025

Accepted: 16 March 2026

Published online: 2 June 2026

Check for updates

Tara Peña[1,10] ✉, Anton E. O. Persson[1,2,10] ✉, Andrey Krayev[3], Áshildur Friðriksdóttir[4], Haotian Su[1,5], Yuan-Mau Lee[4], Young Suh Song[1], Kathryn Neilson[1], Zhepeng Zhang[4], Anh Tuan Hoang[1,4], Jerry A. Yang[1], Lauren Hoang[1], Shan X. Wang[1,4,5], Andrew J. Mannix[4,6], Paul C. McIntyre[4,7,8] & Eric Pop[1,4,7,8,9] ✉

Nanoscale transistors demand aggressive scaling of all channel dimensions—length, width and thickness. Two-dimensional semiconductors (2DS) provide the ultimate thickness limit, yet good device performance has largely remained restricted to micrometre-wide channels. Here we report monolayer 2DS nanoribbon transistors with both n- and p-type operation, fabricated by a top-down multipatterning process that includes 'anchored' contacts to limit nanoribbon delamination. This approach achieves channel lengths and widths down to 25–30 nm, with minimal edge degradation confirmed through nanoscale characterization, including tip-enhanced photoluminescence. Integrated with thin high-κ gate dielectrics, the devices deliver on-state currents up to 560, 420 and 130 μA μm^{-1} at a drain-to-source voltage of 1 V for n-type MoS_2, n-type WS_2 and p-type WSe_2, respectively. These results exceed prior single-gated 2DS nanoribbon reports, with WS_2 improving by more than two orders of magnitude, even for normally off (enhancement-mode) operation. Overall, these findings position top-down patterned 2DS nanoribbons as promising building blocks for future nanosheet transistor architectures.

The history of transistors for digital computing has experienced only three major changes in device architecture: the transition from bipolar to metal-oxide semiconductor field-effect transistors (FETs)[1] in the 1970s, the transition to FinFET or tri-gate transistors[2] around 2007, and the present transition to gate-all-around (GAA) nanosheets[3] in 2025. Although silicon-based GAA transistors are expected to scale for at least another decade, it is unclear if the further thickness reduction required below 3 nm to retain electrostatic control is feasible due to the degradation of electrical properties[4–6]. Instead, two-dimensional (2D) semiconductors, like monolayer transition metal dichalcogenides (TMDs), are appealing alternatives due to their good electrical properties (for example, mobility and band gap) in subnanometre thin films[7,8] and their potential in scaled GAA devices[9]. Accordingly, 2D transistors have been recently placed on technology roadmaps[10], with targeted integration by the late 2030s or early 2040s.

The most important building block of GAA nanosheet transistors is the nanoribbon channel, which must be between 10 to 50 nm wide[11] and atomically thin for the best electrostatic gate control[12,13]. Monolayer 2D semiconductors with subnanometre thickness should also enable shorter, sub-5 nm, gates[14,15] than thicker silicon nanosheets[7], making

[1]Department of Electrical Engineering, Stanford University, Stanford, CA, USA. [2]Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden. [3]HORIBA Scientific, Novato, CA, USA. [4]Department of Materials Science & Engineering, Stanford University, Stanford, CA, USA. [5]Geballe Laboratory for Advanced Materials, Stanford University, Stanford, CA, USA. [6]Stanford Institute for Materials and Energy Sciences, SLAC National Accelerator Laboratory, Menlo Park, CA, USA. [7]Stanford Synchrotron Radiation Lightsource (SSRL), SLAC National Accelerator Laboratory, Menlo Park, CA, USA. [8]Precourt Institute for Energy, Stanford University, Stanford, CA, USA. [9]Department of Applied Physics, Stanford University, Stanford, CA, USA. [10]These authors contributed equally: Tara Peña, Anton E. O. Persson. ✉e-mail: tara.pena@stanford.edu; anton.persson@chalmers.se; epop@stanford.edu

https://doi.org/10.1038/s41565-026-02161-w

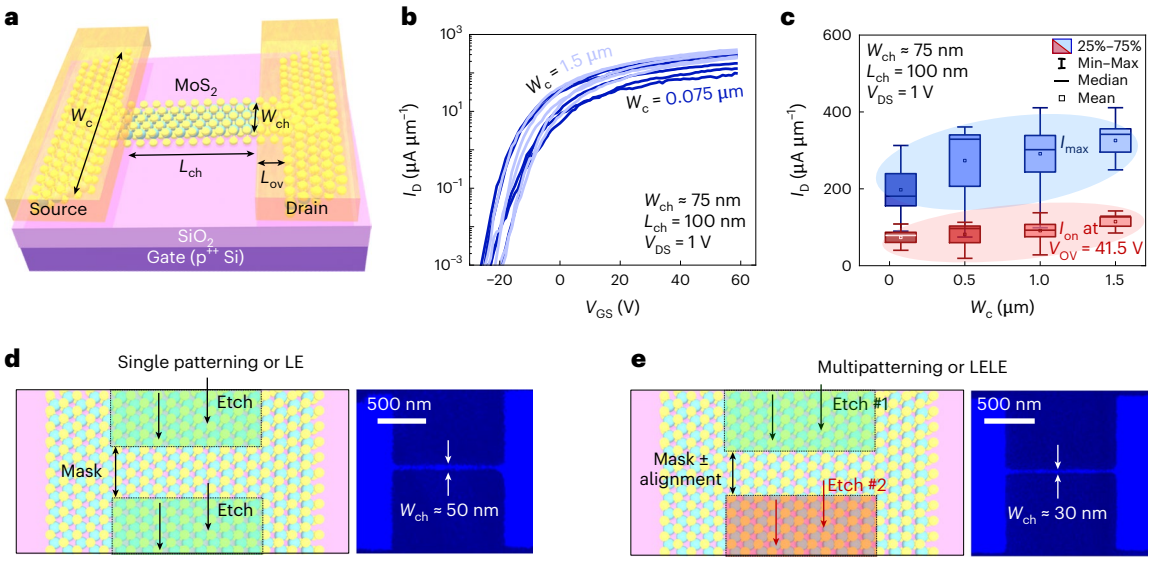


Fig. 1 | Anchored contacts and multipatterning for improved device fabrication. a, Schematic of the dog-bone-shaped back-gated monolayer MoS_2 transistor, defining the channel width (W_{ch}), length (L_{ch}), contact width (W_c) and contact overlap region (L_{ov}). **b**, Transfer characteristics of various short-channel devices (100 nm), displaying larger contact widths in light blue (1.5 µm) and smaller contact widths in dark blue (75 nm). **c**, Box plots of the maximum drain current density (I_{max}) and drain current at fixed gate overdrive (I_{on} at $V_{ov} = V_{GS} - V_T$) for varying contact widths. Each box plot includes five to six devices, totalling 22 tested devices. **d**, Schematic of LE single patterning approach (left), which can define nanoribbon widths down to ~50 nm with reduced e-beam dose. Representative false-coloured SEM image (right) of the resulting nanoribbon. **e**, Schematic of the LELE multipatterning strategy (left; Extended Data Fig. 1 provides more details), used to achieve nanoribbon widths below 50 nm. False-coloured SEM image (right) shows a nanoribbon with ~30 nm width.

them promising for continued scaling and higher device density. However, so far, most demonstrations of good performance in monolayer 2D TMD transistors have used short, sub-100 nm, but micrometre-wide channels. The reasons are manifold but probably include difficulty in fabrication (for example, TMD delamination and lithography limitations), difficulty in making good contacts and mobility degradation due to edge imperfections. Little is known, for example, about how or if charge transport in narrow TMD ribbons changes in channel widths below a micrometre, and there are concerns about magnified edge effects in such devices[16,17].

Here we tackle the challenges mentioned above (adhesion, width scaling, contacts and edge roughness) by realizing n- and p-type monolayer TMD nanoribbons with similar performance as co-fabricated micrometre-wide control devices. A key advance is anchoring the contacts to the substrate during fabrication, which limits nanoribbon delamination and cracking, allowing us to study many such devices. We also introduce a multipatterning approach to achieve nanoribbon widths down to 25 nm. With these advances, we reach a high current density in monolayer MoS_2 nanoribbons, over 600 µA µm^{-1} with a SiO_2 gate dielectric (560 µA µm^{-1} with a HfO_2 dielectric) at a drain-to-source bias of 1 V. We also improve saturation current densities in monolayer WS_2 nanoribbons by over 100× in enhancement mode, in normally off devices. Imaging the nanoribbons and their edges by tip-enhanced photoluminescence (TEPL) and transmission electron microscopy (TEM) suggests that edge disorder is not the limiting factor at these dimensions, indicating that such top-down monolayer TMDs are promising candidates for future nanosheet transistors.

Fabrication of anchored nanoribbons

Due to the lack of out-of-plane chemical bonds, monolayer TMDs adhere to substrates by van der Waals forces, making them prone to delamination during lithography, etching and wet processing. To mitigate this, we designed a dog-bone-shaped structure in which the TMD is narrow only in the channel but expands into wider pads under the source and drain contacts (Fig. 1a). These micrometre-sized regions anchor the nanoribbon to the substrate, thereby increasing the mechanical stability and reproducibility when reducing the nanoribbon widths. The approach is somewhat analogous to the wider source and drain regions used for silicon nanosheets to enable channel release and reduce the contact resistance[18].

We first study MoS_2 nanoribbons on conventional SiO_2 (96 nm) on p^{++} Si substrates, which also serve as back-gates. This allows more rapid process optimization, because the monolayer MoS_2 is grown directly on SiO_2, enabling higher throughput and better adhesion than layer-transferred films. As shown in Fig. 1b, short-channel devices with width $W_{ch} \approx 75$ nm and W_c of either 75 nm or 1.5 µm display nearly identical transfer curves. Encouragingly, we observe a good maximum current density, up to $I_{max} \approx 400$ µA µm^{-1} at $V_{DS} = 1$ V, and off-state currents limited by the measurement noise floor. Figure 1c shows that the current at fixed gate overdrive, I_{on}, at $V_{ov} = V_{GS} - V_T$, remains nearly unchanged, whereas W_c increases by a factor of 20 (V_T is the threshold voltage; Supplementary Fig. 1b.) We attribute this behaviour to two factors: (1) the contact–channel overlap ($L_{ov} > 100$ nm) exceeds the expected current[19] and thermal transfer length of the contacts, and (2) a fabrication process that minimizes patterning damage at sub-100 nm widths, which we discuss below (we estimate the temperature profile along the nanoribbons in Supplementary Fig. 2). Thus, the dog-bone-shaped structure preserves the nanoribbon transistor behaviour, greatly improving our yield due to contact anchoring. Without it, sub-100 nm-wide nanoribbons often delaminate during processing, whereas the anchored contacts enabled >85% yield down to 60 nm widths (Supplementary Fig. 1c). For these reasons, the nanoribbons investigated in the remainder of the manuscript use the wider $W_c = 1.5$ µm, although we note that industrial manufacturing will require alternative yield improvement methods compatible with smaller contact areas[18,20].

Although single-step lithography and etching (LE; Fig. 1d) is commonly used to pattern the 2D channel in academic studies, we wanted to limit the electron-beam (e-beam) exposure dose to reduce the density of lithographically induced defects[21,22]; thus, this method reaches a limit of ~50 nm widths due to the reduced dose and other fabrication trade-offs (Methods). To make narrower ribbons, we use a litho–etch–litho–etch (LELE) multipatterning approach inspired by modern

https://doi.org/10.1038/s41565-026-02161-w

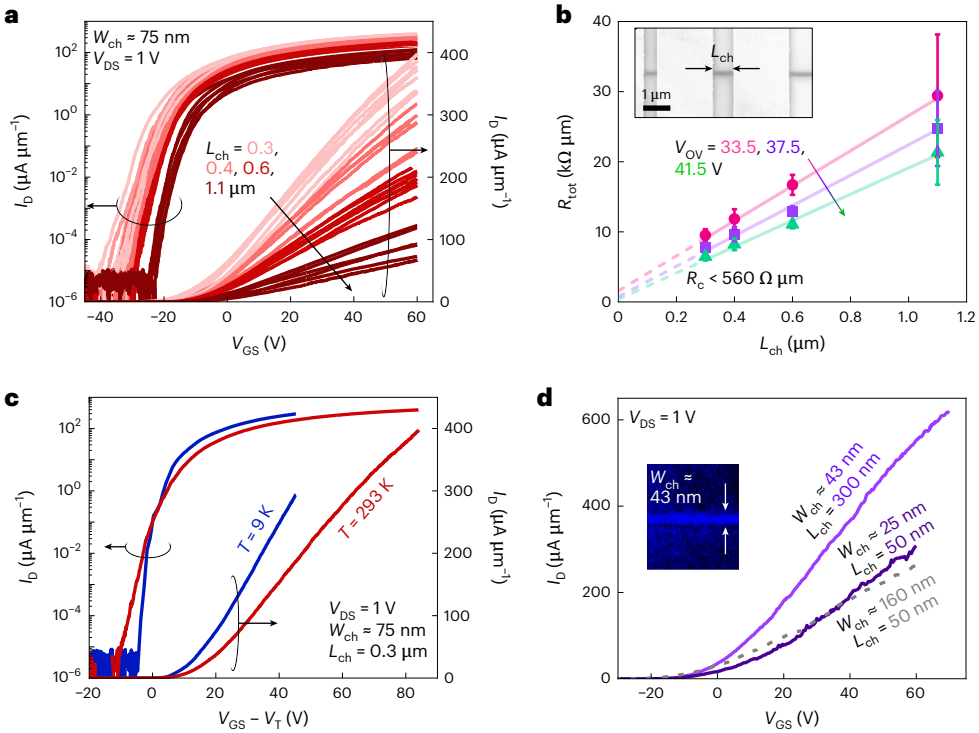


Fig. 2 | Monolayer MoS_2 nanoribbons on SiO_2. a, Transfer characteristics of nanoribbons with four different channel lengths, showing high on-state current density and consistent device behaviour. Between six and ten nanoribbons are measured for each length and 30 devices in total. W_{ch} = 75 nm; W_c = 1.5 µm. **b**, Transfer-length-method analysis of the same devices; each symbol and error bar represent the average and standard deviation of devices with the same channel length, respectively. The contact resistance is comparable with state-of-the-art MoS_2/Au contacts reported[6] in the literature (R_c < 560 Ω µm at the highest V_{ov}). Inset: SEM image of such a transfer-length-method structure. **c**, Transfer characteristics of a nanoribbon device at low temperature (9 K) compared with room temperature, as a function of the V_{GS} − V_T overdrive; V_T is taken at a constant current density of 100 nA µm^{-1}. **d**, Transfer characteristics of other nanoribbons, at V_{DS} = 1 V. The two with 43 nm (LE) and 25 nm (LELE) channel widths reach I_{max} ≈ 620 µA µm^{-1} and ~310 µA µm^{-1}, respectively, some of the highest current densities reported so far for single-gated monolayer TMD nanoribbons at these widths. The 160 nm wide nanoribbon (dashed grey line, also on the LELE chip) has a similar current density as the 25 nm wide device, suggesting that both devices were limited by a higher contact resistance rather than edge disorder. The inset is a false-coloured SEM of the 43 nm wide nanoribbon device.

industrial lithography (Fig. 1e and Extended Data Fig. 1). This enables nanoribbons down to ~25 nm widths and maintains the same overall low dose as the single patterning LE approach (Methods). Achieving sub-25 nm wide nanoribbons should be possible by optimizing the TMD adhesion and anchoring; however, sub-15 nm nanoribbons may not be desirable for GAA transistors due to larger parasitic capacitance[4,23].

Electrical characterization of MoS_2 nanoribbon transistors

We also investigate the effect of contact resistance, by evaluating nanoribbon behaviour as a function of channel length using ten transfer-length-method structures. These nanoribbons have W_{ch} ≈ 75 nm and anchored contacts with W_c ≈ 1.5 µm. As shown in Fig. 2a, the devices exhibit excellent channel length dependence, maintaining stable characteristics and achieving an on-state current density up to ~400 µA µm^{-1} at channel lengths of L_{ch} ≈ 300 nm and V_{DS} = 1 V. Figure 2b displays the total device resistance R_{tot} versus channel length and the linear extrapolation yields a contact resistance of R_c < 560 Ω µm, or 190 ± 370 Ω µm from the linear fit at the highest V_{ov}, comparable with some of the best MoS_2/Au contacts reported so far[6]. We note that R_c and R_{tot} are normalized by the channel width W_{ch}, not by W_c, because the contacts have a non-negligible overlap with the channel (L_{ov} > 100 nm, greater than the expected current transfer length at these contacts[6,19]), as shown in Fig. 1a.

Interestingly, we do not see mobility degradation in nanoribbons (~75 nm wide) compared with much wider devices (~850 nm wide) fabricated on the same chip. As summarized in Supplementary Fig. 3, the field-effect electron mobility μ_{FE} is in the range of 30–60 cm^2 V^{-1} s^{-1} for ten devices at room temperature, with greater device-to-device variation than any apparent width dependence. This is not surprising, because the intrinsic electron mean free path in monolayer MoS_2 is expected[24] to be 3–5 nm, much shorter than the nanoribbon width. Nevertheless, it is reassuring that the edges produced from the top-down patterning process used here do not appear to deteriorate device operation, a topic we return to below. Figure 2c displays the low-temperature measurements of a nanoribbon at ~9-K ambient temperature, revealing that mobility approximately doubles, which suggests that low-temperature transport is ultimately limited by impurities and possibly by the edges (Supplementary Fig. 4).

We also show transfer characteristics of other nanoribbons in Fig. 2d; one has W_{ch} ≈ 43 nm and L_{ch} ≈ 300 nm, using the single-step LE approach, and two others have W_{ch} ≈ 25 nm and 160 nm with L_{ch} ≈ 50 nm, using the LELE multipatterning approach. The first two reach I_{max} ≈ 620 µA µm^{-1} and ~310 µA µm^{-1}, respectively, at V_{DS} = 1 V and similar V_{GS}; the former is one of the highest current densities reported so far in single-gated MoS_2 nanoribbons; the latter is one of the highest values for any monolayer ribbon of such small width. The 25 nm and 160 nm wide nanoribbons on the same LELE chip have similar current densities, suggesting that they are not limited by edge disorder. However, their I_{max} is lower in a shorter channel than the device on the LE chip, which we attribute to the higher contact resistance arising from our chip-to-chip variation (Supplementary Fig. 5). The nanoribbon width estimates have a 3–5 nm uncertainty (Methods), which implies 10%–20% uncertainty in current density.

https://doi.org/10.1038/s41565-026-02161-w

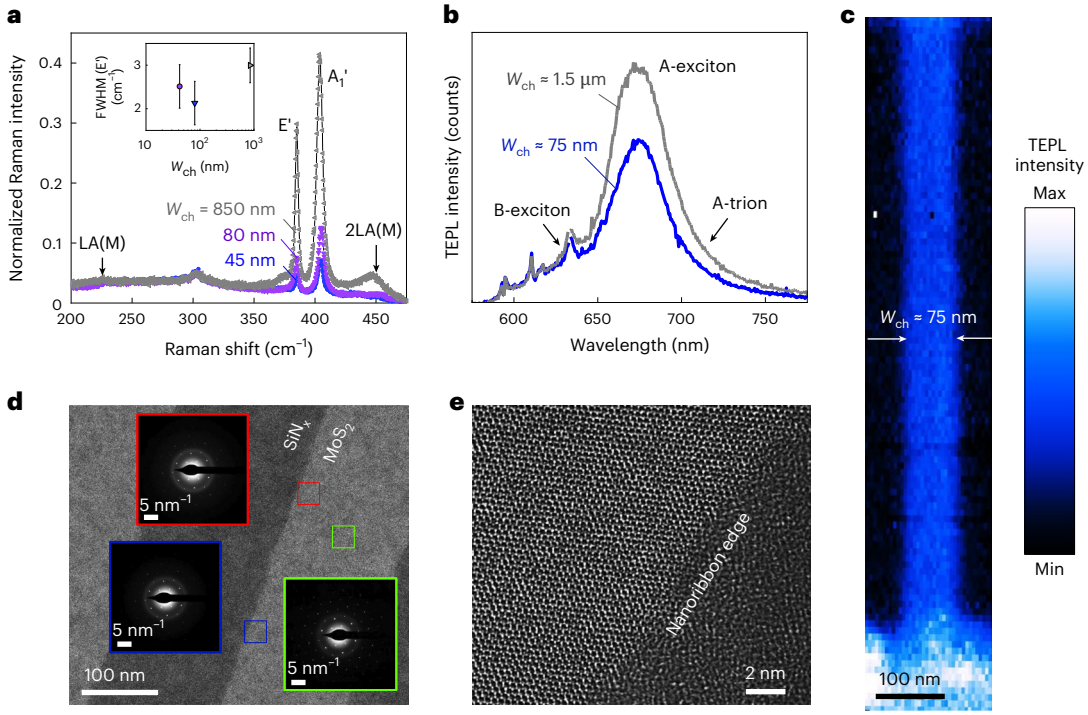


Fig. 3 | Nanoribbon material and edge characterization. a, Raman spectra of monolayer MoS_2 device channels between ~45 nm to 850 nm wide, showing neither discernible broadening of the E′ or A_1′ modes nor contributions from the LA(M) defect-mediated peak. The Raman data are normalized to the Si substrate peak at 520 cm^{-1} (not shown). Inset: full-width at half-maximum (FWHM) of the E′ mode as a function of the channel width. **b**, Averaged TEPL spectra comparing a nanoribbon channel region with the much wider anchor region of the same nanoribbon, showing minimal broadening of the A-exciton peak and a slight increase in the trion-to-exciton intensity ratio. **c**, TEPL intensity map of an entire ~75 nm wide and ~1 µm long nanoribbon, with uniform optical emission along the channel. The black spot in the top third of the nanoribbon is a measurement artefact. **d**, STEM image of two parallel monolayer MoS_2 nanoribbons (from an array transferred onto the SiN_x membrane). Insets: diffraction patterns of three regions, revealing good crystallinity in the channel and near the edge. **e**, Magnified edge region in the TEM mode from the same STEM.

Nanoscale spectroscopic and structural characterization

We next wish to understand the origin of good performance in our nanoribbon devices, thus we turn to materials characterization techniques to further evaluate the fabrication process and the effect of the edges. The Raman spectra shown in Fig. 3a for representative monolayer MoS_2 devices reveal no discernible signs of damage, as the predominant E′ (in-plane) and A_1′ (out-of-plane) phonon modes do not broaden with reduced nanoribbon widths, down to 45 nm. We do not observe defect-mediated phonon modes[25,26] (for example, LA(M) around 227 cm^{-1}) in any of our nanoribbons, suggesting that edge-related defects are not predominant. We also map our nanoribbons with TEPL (Fig. 3b,c), which reveal uniform signal across a long and narrow channel ($L_{ch} \approx 1$ µm, $W_{ch} \approx 75$ nm). The TEPL spectra confirm the quality of the nanoribbons, where the A-exciton does not broaden compared with the wider regions. The nanoribbons do exhibit a slightly larger trion-to-exciton ratio (Supplementary Fig. 6), which potentially suggests doping from the edges (see Extended Data Fig. 4 for more discussion).

To visualize the atomic structure and edge roughness, we performed high-angle annular dark-field scanning transmission electron microscopy (STEM) and monochromated TEM imaging on monolayer MoS_2 nanoribbons transferred onto 10 nm thick SiN_x membranes (Fig. 3d,e). Compared with the nanoribbon transistors, these samples may be subject to some additional damage from the transfer process and the e-beam exposure during imaging. Despite this, the nanoribbon edges appear clean, with edge roughness of at most a few nanometres. The edge termination probably alternates between zigzag and armchair segments, as expected from a top-down patterning process without edge-selective anisotropy. Energy-dispersive X-ray spectroscopy and electron energy loss spectroscopy reveal no discernible accumulation of oxygen or fluorine near the edges in monolayer MoS_2 and WSe_2 (Supplementary Figs. 7–9). These findings suggest that our top-down fabrication approach does not introduce observable disorder or contamination of the nanoribbons and their edges, supporting the lack of degradation seen in electrical characteristics.

High-κ dielectric integration

To reduce the operating voltage of our nanoribbon transistors, we integrate ultrathin high-κ dielectrics into the gate stack. Achieving this involves transferring monolayer TMD films onto prepatterned local back-gates with HfO_2 dielectric (~1.5 nm equivalent oxide thickness) and then applying our optimized nanoribbon process described earlier (Methods). The schematic of the resulting nanoribbon devices is shown in Fig. 4a and confirmed by top-down scanning electron microscopy (SEM) in Fig. 4b.

Here, we expand beyond MoS_2 by also examining monolayer n-type WS_2 and p-type WSe_2 nanoribbons, all patterned down to ~50 nm widths. Raman spectroscopy (Supplementary Fig. 10) indicates that the nanoribbon fabrication steps do not appear to introduce additional damage. Figure 4c compares the transfer characteristics of three such nanoribbon channels that are just 50 nm × 50 nm. Among these, monolayer MoS_2 achieves the highest on-state current density, $I_{max} \approx 460$ µA µm^{-1} at $V_{DS} = 1$ V, although with a negative V_T (that is, a normally on, depletion-mode device). An ~60 nm wide monolayer MoS_2 nanoribbon reaches $I_{max} \approx 560$ µA µm^{-1} at $V_{DS} = 1$ V (Supplementary Fig. 11).

On the other hand, monolayer WS_2 nanoribbons show a desirable positive V_T (that is, a normally off, enhancement-mode device), but still reach $I_{max} \approx 420$ µA µm^{-1} at $V_{DS} = 1$ V (and up to ~460 µA µm^{-1} at

https://doi.org/10.1038/s41565-026-02161-w

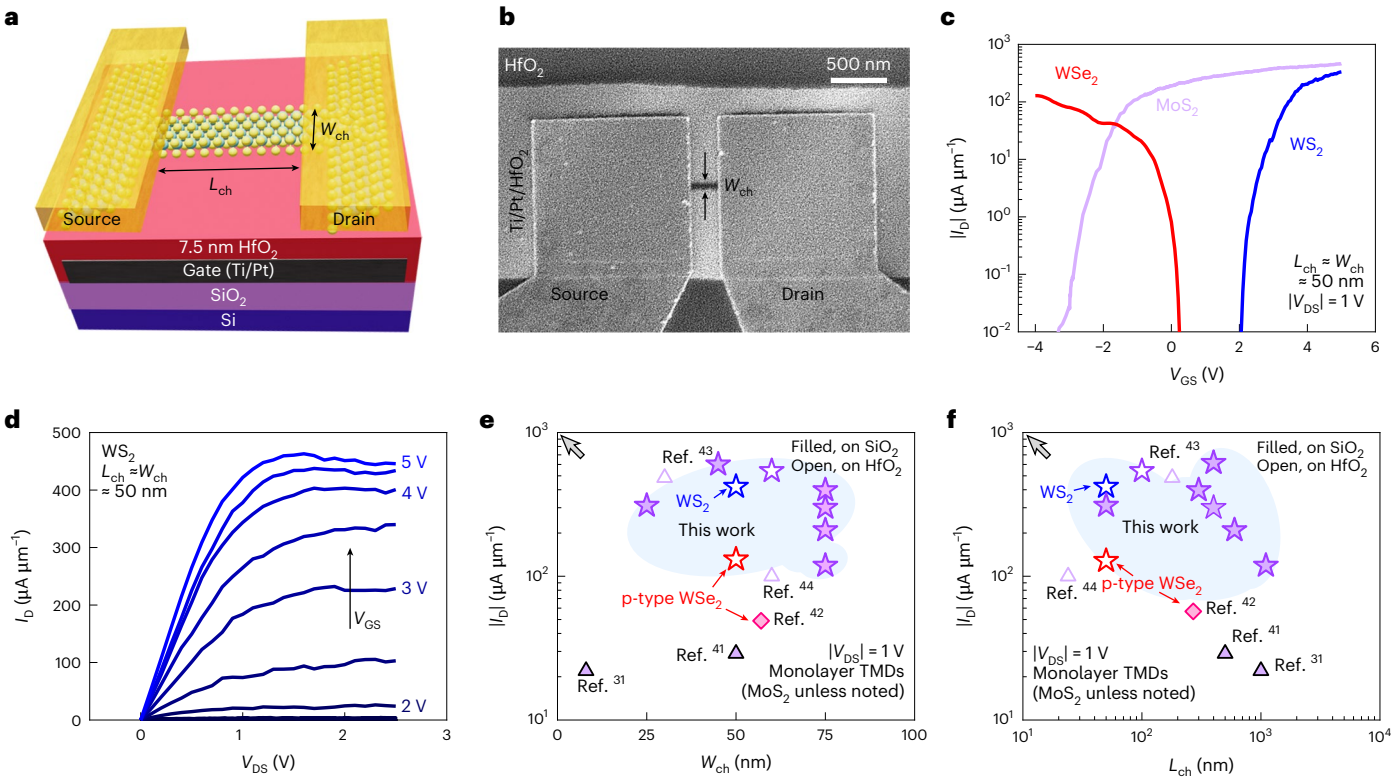


Fig. 4 | Complementary monolayer TMD nanoribbons with a high-κ dielectric. **a**, Schematic of a monolayer nanoribbon including anchored contacts, here with a thin HfO_2 gate dielectric (figure not to scale). **b**, Top-down SEM image of a representative nanoribbon transistor. **c**, Measured transfer characteristics of monolayer MoS_2, WS_2 and WSe_2 nanoribbons with a high-κ dielectric, all with channel lengths and widths of ~50 nm. **d**, Measured output characteristics of monolayer WS_2 nanoribbon, showing well-behaved, normally off (enhancement-mode) operation with high current saturation. **e**, Comparing $|I_{max}|$ of single-gated monolayer TMD nanoribbons versus channel width, at $|V_{DS}| = 1$ V and maximum $|V_{GS}|$. Unlabelled symbols are MoS_2, whereas WS_2 and WSe_2 are labelled. Our devices, marked by star symbols, reach some of the highest current densities reported so far. Our WS_2 (blue star) has the highest $I_{max} \approx 420$ μA μm^{-1} to date (at $V_{DS} = 1$ V) in a monolayer nanoribbon of this 2D semiconductor. Filled markers are on SiO_2 back-gate substrates[31,39–42]; open markers are devices with a high-κ gate dielectric[43,44]. Symbols with the red border are p-type WSe_2 and all others are n type. **f**, Additional benchmarking of single-gated nanoribbon devices, here versus channel length L_{ch}. Block arrows point to the desirable corner in both benchmarking plots.

$V_{DS} = 1.5$ V; Fig. 4d). These WS_2 current densities are some of the highest values reported so far, by >100×, for a nanoribbon of this material, probably due to our fabrication process and our use of stressed Ni/Au contacts[27] with good $R_c \approx 675 \pm 268$ Ω μm (Supplementary Fig. 12). Finally, the p-type WSe_2 nanoribbons reach $|I_{max}| \approx 130$ μA μm^{-1}, an encouraging result given its desirable negative V_T (that is, a normally off, enhancement-mode device) and the historical performance gap between p-type and n-type TMD transistors. Figure 4d shows the output curves of the 50 nm × 50 nm WS_2 nanoribbon, with good current saturation and device turn-off at zero gate voltage, essential for future circuit implementation.

Figure 4e,f compares our results with other single-gate monolayer TMD nanoribbons reported to date, at $|V_{DS}| = 1$ V. Here we benchmark the current density, $|I_{max}|$, rather than mobility or contact resistance, because I_{max} is less prone to measurement error (its greatest uncertainty comes from the nanoribbon width) and because, in principle, the threshold voltage can be adjusted by gate-stack engineering[28,29]. I_{max} also incorporates information about contact resistance and mobility, and it is ultimately responsible for circuit delays, which are inversely proportional to the current density[30]. Our monolayer MoS_2 nanoribbons match or exceed previously reported I_{max} at comparable channel widths, whereas our monolayer WS_2 and WSe_2 nanoribbons exceed existing results, the WS_2 by a factor of >100× (we provide additional output curves, current drive statistics and V_T discussion across 140 devices; Extended Data Figs. 2–4). Although sub 50 nm and even sub-10 nm-wide nanoribbons (monolayer and multilayer) have been demonstrated using bottom-up[31–35] or anisotropic etching techniques[36], such devices have not reached the current densities of our top-down patterned nanoribbons at comparable channel widths.

While we have shown that the on-state of these nanoribbons can be as good as existing micrometre-scale devices, a remaining aspect is to enquire whether the off-state is affected by their edges. To probe this regime, we measured arrays of MoS_2 nanoribbons (Extended Data Fig. 5). These reach I_{max}/I_{min} current ratios of >10^9, limited by the measurement noise floor, also comparable with some of the best-known micrometre-scale devices reported to date. In other words, we conclude that at least down to the channel widths probed here, there is no measurable edge conduction in the off-state, probably due to the mixed character[16,37] of our edges (Fig. 3e). To our knowledge, no previous efforts on parallel nanoribbon arrays have probed the deep off state, although a previous study[38] on random networks composed of narrower (10–30 nm) ribbons also found no evidence of off-state degradation. We provide additional comparisons of monolayer TMD nanoribbons, including some with unconventional geometry or fabrication approaches in Supplementary Table 1.

Conclusions

We have demonstrated both n- and p-type (that is, complementary) nanoribbon transistors with MoS_2, WS_2 and WSe_2 at the ultimate limit of monolayer channel thinness. These achieve high current densities in channels down to ~25 nm widths, with WS_2 nanoribbons in particular showing desirable, normally off (enhancement-mode) behaviour, with good current saturation (~460 μA μm^{-1} at 1.5 V drain-to-source voltage). The nanoribbons were enabled by mechanically robust

anchored contacts that improve yield, a low-dose multipatterning strategy with low-residue resist, and minimal edge degradation, studied by advanced nanoscale imaging, including TEPL. Our work shows that scaling monolayer TMD channels down to ~25 nm widths does not degrade their on- or off-state, and such nanoribbon demonstrations are more technologically relevant than micrometre-wide devices. Looking ahead, the compatibility with high-κ dielectrics, complementary device polarity and good performance across several TMDs position monolayer nanoribbons as important building blocks of future GAA[9] nanosheet transistors.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41565-026-02161-w.

References

1. Kahng, D. Electric field controlled semiconductor device. US patent 3,102,230 (1963).
2. Auth, C. et al. A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors. In *Proc. Symposium on VLSI Technology* 131–132 (IEEE, 2012).
3. Yeap, G. et al. 2 nm platform technology featuring energy-efficient nanosheet transistors and interconnects co-optimized with 3DIC for AI, HPC and mobile SoC applications. In *Proc. IEEE International Electron Devices Meeting* 1091–1094 (IEEE, 2024).
4. Cao, W. et al. The future transistors. *Nature* **620**, 501–515 (2023).
5. Agrawal, A. et al. Silicon RibbonFET CMOS at 6 nm gate length. In *Proc. IEEE International Electron Devices Meeting* 605–608 (IEEE, 2024).
6. English, C. D., Shine, G., Dorgan, V. E., Saraswat, K. C. & Pop, E. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett.* **16**, 3824–3830 (2016).
7. O'Brien, K. P. et al. Process integration and future outlook of 2D transistors. *Nat. Commun.* **14**, 6400 (2023).
8. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
9. Mortelmans, W. et al. Gate oxide module development for scaled GAA 2D FETs enabling SS <75 mV dec^{-1} and record Idmax >900 µA $µm^{-1}$ at Lg <50 nm. In *Proc. IEEE International Electron Devices Meeting* 365–368 (IEEE, 2024).
10. Lockhart de la Rosa, C. J. & Kar, G. S. Introducing 2D-material based devices in the logic scaling roadmap. *Semicond. Dig.* **6**, 17–21 (2024).
11. IEEE International Roadmap for Devices and Systems; https://irds.ieee.org/ (accessed 25 April 2025).
12. Pal, A., Chavan, T., Jabbour, J., Cao, W. & Banerjee, K. Three-dimensional transistors with two-dimensional semiconductors for future CMOS scaling. *Nat. Electron.* **7**, 1147–1157 (2024).
13. Dubey, P. K. et al. Simulation of vertically stacked 2-D nanosheet FETs. *IEEE Trans. Electron Devices* **72**, 1494–1500 (2025).
14. Wu, F. et al. Vertical MoS_2 transistors with sub-1-nm gate lengths. *Nature* **603**, 259–264 (2022).
15. Chen, S. et al. Channel and contact length scaling of two-dimensional transistors using composite metal electrodes. *Nat. Electron.* **8**, 394–402 (2025).
16. Pan, H. & Zhang, Y.-W. Edge-dependent structural, electronic and magnetic properties of MoS_2 nanoribbons. *J. Mater. Chem.* **22**, 7280–7290 (2012).
17. Li, Y., Zhou, Z., Zhang, S. & Chen, Z. MoS_2 nanoribbons: high stability and unusual electronic and magnetic properties. *J. Am. Chem. Soc.* **130**, 16739–16744 (2008).
18. Mochizuki, S. et al. Stacked gate-all-around nanosheet pFET with highly compressive strained $Si_{1-x}Ge_x$ channel. In *Proc. IEEE International Electron Devices Meeting* 19–22 (IEEE, 2020).
19. McClellan, C. J., Yalon, E., Smithe, K. K. H., Suryavanshi, S. V. & Pop, E. High current density in monolayer MoS_2 doped by AlO_x. *ACS Nano* **15**, 1587–1596 (2021).
20. Bourjot, E. et al. Wrap-all-around contact for nanosheet-FET and method of forming same. US patent 10,559,656 (2020).
21. Wu, Z. et al. Defects as a factor limiting carrier mobility in WSe_2: a spectroscopic investigation. *Nano Res.* **9**, 3622–3631 (2016).
22. Neilson, K. *Advancing Two-dimensional Semiconductor Devices Through Growth, Fabrication, And Contact Engineering*. PhD thesis, Stanford Univ. (2025).
23. Ahmed, Z. et al. Introducing 2D-FETs in device scaling roadmap using DTCO. In *Proc. IEEE International Electron Devices Meeting (IEDM)* 465–468 (IEEE, 2020).
24. Wang, M. A. & Pop, E. Monte Carlo simulation of electrical transport with joule heating and strain in monolayer MoS_2 devices. *Nano Lett.* **25**, 6841–6847 (2025).
25. Mignuzzi, S. et al. Effect of disorder on Raman scattering of single-layer MoS_2. *Phys. Rev. B* **91**, 195411 (2015).
26. Wu, J.-B. et al. Monolayer molybdenum disulfide nanoribbons with high optical anisotropy. *Adv. Opt. Mater.* **4**, 756–762 (2016).
27. Hoang, L. et al. Understanding the impact of contact-induced strain on the electrical performance of monolayer WS_2 transistors. *Nano Lett.* **24**, 12768–12774 (2024).
28. Ko, J.-S. et al. Achieving 1-nm-scale equivalent oxide thickness top-gate dielectric on monolayer transition metal dichalcogenide transistors with CMOS-friendly approaches. *IEEE Trans. Electron Devices* **72**, 1514–1519 (2025).
29. Ko, J.-S. et al. Sub-nanometer equivalent oxide thickness and threshold voltage control enabled by silicon seed layer on monolayer MoS_2 transistors. *Nano Lett.* **25**, 2587–2593 (2025).
30. Salman, E. & Friedman, E. G. *High Performance Integrated Circuit Design* (McGraw-Hill, 2012).
31. Li, X. et al. Width-dependent continuous growth of atomically thin quantum nanoribbons from nanoalloy seeds in chalcogen vapor. *Nat. Commun.* **15**, 10080 (2024).
32. Saunders, A. P. et al. Direct exfoliation of nanoribbons from bulk van der Waals crystals. *Small* **20**, 2470348 (2024).
33. Li, X. et al. Nickel particle–enabled width-controlled growth of bilayer molybdenum disulfide nanoribbons. *Sci. Adv.* **7**, eabk1892 (2021).
34. Chowdhury, T. et al. Substrate-directed synthesis of MoS_2 nanocrystals with tunable dimensionality and optical properties. *Nat. Nanotechnol.* **15**, 29–34 (2020).
35. Ma, Z. et al. Lattice-guided growth of dense arrays of aligned transition metal dichalcogenide nanoribbons with high catalytic reactivity. *Sci. Adv.* **11**, eadr8046 (2025).
36. Hoque, M. A. et al. Ultranarrow semiconductor WS_2 nanoribbon field-effect transistors. *Nano Lett.* **25**, 1750–1757 (2025).
37. Davelou, D., Kopidakis, G., Kaxiras, E. & Remediakis, I. N. Nanoribbon edges of transition-metal dichalcogenides: stability and electronic properties. *Phys. Rev. B* **96**, 165436 (2017).
38. Aslam, M. A. et al. Single-crystalline nanoribbon network field effect transistors from arbitrary two-dimensional materials. *npj 2D Mater. Appl.* **6**, 76 (2022).
39. Chen, S. et al. Monolayer MoS_2 nanoribbon transistors fabricated by scanning probe lithography. *Nano Lett.* **19**, 2092–2098 (2019).
40. Jiang, J. et al. Schottky-barrier quantum well in two-dimensional semiconductor nanotransistors. *Mater. Today Phys.* **15**, 100275 (2020).

41. Kotekar-Patil, D., Deng, J., Wong, S. L., Lau, C. S. & Goh, K. E. J. Single layer MoS_2 nanoribbon field effect transistor. *Appl. Phys. Lett.* **114**, 013508 (2019).
42. Chen, S., Zhang, Y., King, W. P., Bashir, R. & van der Zande, A. M. Edge-passivated monolayer WSe_2 nanoribbon transistors. *Adv. Mater.* **36**, 2313694 (2024).
43. Lan, H.-Y. et al. Reliability of high-performance monolayer MoS_2 transistors on scaled high-κ HfO_2. *npj 2D Mater. Appl.* **9**, 5 (2025).
44. O'Brien, K. P. et al. Advancing 2D monolayer CMOS through contact, channel and interface engineering. In *Proc. IEEE International Electron Devices Meeting* 163–166 (IEEE, 2021).

Methods

TMD synthesis and transfer

All monolayer MoS_2 and WS_2 films were grown onto thermal 96nm SiO_2/Si and sapphire substrates, respectively, as described in previous works[45,46]. The chemical vapour deposition grown monolayer WSe_2 on sapphire was purchased from 2D Semiconductors. For devices on HfO_2 (either 5.5 nm or 7.5 nm thick) with local back-gates, all the monolayer films were transferred from their growth substrates by spinning polystyrene (PS) at 1,250 rpm for 60 s onto the growth substrate, followed by baking at 85 °C for 5 min. The TMD/PS stack was then immersed in deionized water to delaminate it from the growth substrate. The TMD/PS stack was then placed onto the chip with local back-gate structures, dried with N_2 and left in a N_2 dry box overnight. The following morning, the chips were heated at 85 °C for 1 h, 150 °C for 1 h and then cooled to room temperature. The chips were then placed in toluene overnight, followed by acetone and isopropanol cleaning (10 min each) to remove the PS from the surface. Before device fabrication, the chips were annealed in vacuum (~10^{-5} torr) at 200 °C for 2 h to promote TMD adhesion to HfO_2.

Fabrication process

For the devices shown in Figs. 1, 2 and 3a, the monolayer MoS_2 films were grown by solid-source chemical vapour deposition directly onto dry thermal SiO_2 (96 nm) on p^{++} Si (resistivity, <5 mΩ cm) substrates and were processed with no transfer, thereby having better adhesion and higher yield. For these devices, e-beam lithography (Raith EBPG 5200+ with 100 kV accelerating voltage) was used to first define coarse probing pads, which consist of e-beam-evaporated SiO_2 (20 nm)/Ti (1 nm)/Pt (15 nm), where SiO_2 is used to limit probing pad leakage to the Si back-gate. To construct the local back-gate samples (Fig. 4a–d), back-gate metals of Ti (1 nm)/Pt (13 nm) are defined by lift-off and then 7.5 nm HfO_2 is deposited by atomic layer deposition at 200 °C.

All nanoribbon channels were then defined using e-beam lithography and etched using XeF_2. A high-resolution AR-P 6200.04 (CSAR 62) resist was spun (3,000 rpm, 60 s) and baked at 120 °C (5 min), yielding an ~50 nm resist thickness. Compared with conventional polymethyl methacrylate recipes, we found that the CSAR 62 resist allows for lower writing doses (here we use 425–475 μC cm^{-2}) and leaves less residue on the TMD surface. The resist was developed in room-temperature xylenes (45 s), followed by a quick isopropanol dip. This procedure would be repeated if implementing the multipatterning (or LELE) approach (Extended Data Fig. 1). We found that a colder or more dilute developer can further improve resolution (even using the single patterning (LE) process), but at the cost of requiring higher doses that risk TMD damage[21,22]. After channel formation, we defined fine source/drain contacts by a third e-beam lithography step and deposited using e-beam evaporation (~10^{-8} torr). For monolayer MoS_2, ~40 nm Au contacts are used, without an adhesion layer[6]. For monolayer WS_2, stressed Ni (10 nm)/Au (20 nm) fine contacts were used, following our previous work[27], to obtain good R_c. For monolayer WSe_2, Pd (10 nm)/Au (20 nm) contacts are utilized to promote hole injection, given the higher work function of Pd. Monolayer WSe_2 devices in this work were immersed in chloroform overnight before measurements, as chloroform has been found to lower R_c for holes[47] in monolayer WSe_2. Extended Data Figs. 2–4 show all three monolayer TMDs with Au (35 nm) contacts and with a 5.5 nm HfO_2 back-gate dielectric, where both the n-type semiconductors experience vacuum annealing and the p-type semiconductor is immersed in chloroform overnight before measurements.

Electrical measurements

Unless otherwise stated, electrical measurements were performed at room temperature using a Janis ST-100 vacuum probe station at ~10^{-4} torr, using a Keithley 4200A semiconductor parameter analyser. All monolayer MoS_2 devices presented in this work were first annealed at 250 °C for 2 h under vacuum inside the probe station, to improve R_c and remove adsorbates from the channel[6]. The monolayer MoS_2 devices are then measured after cooling back to room temperature, without breaking vacuum. The monolayer WS_2 devices shown in Fig. 4 did not undergo any annealing procedures (to retain the strain state from the Ni/Au contacts), whereas the WS_2 devices (Extended Data Figs. 2 and 3) experienced annealing to improve their Au contacts. All monolayer WSe_2 devices presented here did not experience any annealing before electrical testing in vacuum. Cryogenic measurements were conducted using a Lakeshore cryoprobe station under vacuum (~10^{-6} torr) and a Keithley 4200A semiconductor parameter analyser.

Material characterization

Micro-Raman spectroscopy was performed using a Horiba LabRAM instrument with a 532 nm laser with 1,800 spectrometer grating at a laser power of 120 μW. Measurements were performed at room temperature and in ambient conditions. Atomic force microscopy (AFM) was conducted using a Bruker Dimension Icon in the standard tapping mode with a NSC18 Pt probe. Scanning electron microscopy (SEM) was performed using either an FEI Magellan or Helios, with an accelerating voltage of 2 kV and beam current of 43 pA.

After the nanoribbons were visualized by AFM and/or SEM, we extracted the average nanoribbon width across the channel. This channel extraction was systematically conducted using ImageJ analysis software in which an average contrast line profile across the substrate and nanoribbon can be determined. This contrast line profile can be fitted to a Gaussian function in which the nanoribbon width is defined as the full-width at half-maximum of the fitted function. The fitting allows us to simultaneously calculate the uncertainty in our channel width estimates, which was typically 3–5 nm.

High-resolution TEM images were taken at 80 kV using a Thermo Fisher Spectra 300 operated in the monochromated TEM imaging mode. To account for sample drift during acquisition, 80 frames were collected with drift correction enabled. The frames were then aligned and averaged to compensate for drift and improve the signal-to-noise ratio. Imaging was performed using a collection angle of 228 mrad. Final images were processed using a drift-corrected frame integration routine on the Ceta camera, which registers and integrates the aligned frames. A radial Wiener filter was applied to further suppress high-frequency noise and enhance image clarity. Energy-dispersive X-ray spectroscopy was performed in the STEM mode at 80 kV on the same instrument. Electron energy loss spectroscopy measurements were performed in the single-mode high-quality acquisition using the energy-filtered charge-coupled device detector. The microscope was operated with a 50 μm C2 aperture, corresponding to a convergence semi-angle of 21.4 mrad and a camera length of 29 mm. The beam current was set to 0.213 nA. A smaller entrance aperture was used to improve the energy resolution. The zero-loss peak was aligned before acquisition, and the spectrometer was tuned for optimal focus. The final zero-loss peak full-width at half-maximum was 1.05 eV, confirming good energy resolution. The dispersion was set to 0.3 eV per channel, suitable for resolving the C–K, N–K, O–K and F–K edges and maintaining sufficient signal intensity. The monolayer MoS_2 samples for this experiment (Fig. 3d,e) were grown directly onto 300 nm SiO_2 on Si substrates, and then underwent e-beam lithography and dry etching (following the channel definition procedure described above) to produce nanoribbons. The finalized nanoribbons were delaminated using a droplet of deionized water onto a polydimethylsiloxane stamp. The nanoribbons were then dry transferred from the stamp down onto a 10 nm thick SiN_x TEM window (Norcada TA301Z).

TEPL maps were collected on a LabRAM-Nano AFM Raman system (HORIBA Scientific) modified for the concurrent excitation and collection using two lasers simultaneously[48]. Excitation and collection of the Raman signal were done using the side 100×, 0.7-numerical-aperture objective (Mitutoyo) inclined at 25° to the plane of the sample. Laser power on the sample for both 633 nm and 594 nm excitations were

about 150 μW. The TEPL maps were collected using Omni-Access-NC-Au (APPNano) TERS probes in the DualSpec version of the SpecTop mode where in each pixel of the map, the spectra were collected with the tip in direct contact with the sample (near + far field) and in the tapping operation with an amplitude of about 20 nm (far field). The far-field data were subtracted from the combined map to produce the pure near-field response. The monolayer MoS_2 samples for this experiment (Fig. 3b,c) were grown directly onto 300 nm SiO_2 on Si substrates, which then underwent e-beam lithography and dry etching (following the channel definition procedure described above) to complete the nanoribbons. The samples were vacuum annealed at ~10^{-4} torr at 250 °C for 8 h to remove the adsorbates and resist residues before experiments.

Data availability

All data needed to evaluate the conclusions in this paper are present in the Article or its Supplementary Information.

References

45. Smithe, K. K. H., Suryavanshi, S. V., Muñoz Rojo, M., Tedjarati, A. D. & Pop, E. Low variability in synthetic monolayer MoS_2 devices. *ACS Nano* **11**, 8456–8463 (2017).
46. Zhang, Z. et al. Chemically tailored growth of 2D semiconductors via hybrid metal–organic chemical vapor deposition. *ACS Nano* **18**, 25414–25424 (2024).
47. Hoang, L. et al. Low resistance p-type contacts to monolayer WSe_2 through chlorinated solvent doping. *Nat. Commun.* **17**, 718 (2026).
48. Krayev, A. et al. Excitation laser energy dependence of the gap-mode TERS spectra of WS_2 and MoS_2 on silver. *ACS Photonics* **12**, 1535–1544 (2025).
49. Liu, H., Gu, J. & Ye, P. D. MoS_2 nanoribbon transistors: transition from depletion mode to enhancement mode by channel-width trimming. *IEEE Electron Device Lett.* **33**, 1273–1275 (2012).

Acknowledgements

T.P., H.S., L.H. and E.P. were supported by SUPREME, a JUMP 2.0 Centre sponsored by the Semiconductor Research Corporation (SRC) and DARPA. T.P. would like to thank the NSF MPS-Ascend Postdoctoral Fellowship. A.E.O.P. acknowledges the Knut and Alice Wallenberg Foundation (grant number 2022.0374). T.P. and E.P. acknowledge Intel Corporation. K.N. acknowledges the Stanford Graduate Fellowship. J.A.Y. is supported by the Achievement Rewards for College Scientists Foundation. K.N. and J.A.Y. both thank the National Science Foundation Graduate Research Fellowship Program (grant number DGE-1656518). A.T.H. and A.J.M. acknowledge support from TSMC through the SystemX Alliance. Fabrication and characterization in this work were primarily performed at nano@stanford (RRID: SCR_026695). E.P. and A.J.M. acknowledge the NSF Future of Semiconductors (FuSe2) Programs (Award number 2425218). T.P., A.E.O.P. and E.P. acknowledge partial support from Samsung Electronics. We greatly appreciate A. Barnum for guidance with TEM imaging and Z. Han for thermal simulation discussions.

Author contributions

E.P. conceived the project together with T.P. and A.E.O.P. T.P., A.E.O.P. and A.T.H. synthesized the monolayer MoS_2 and Z.Z. grew the monolayer WS_2 samples. T.P. fabricated the devices, with process development guidance from A.E.O.P., K.N. and E.P. H.S., Y.-M.L. and J.A.Y. assisted with various fabrication steps. L.H. led chloroform doping for the monolayer WSe_2 devices, with supervision from A.J.M. T.P. and A.E.O.P. performed all electrical characterization. T.P. acquired the micro-Raman and photoluminescence data, AFM measurements and scanning electron imaging. A.K. conducted all TEPL experiments. Á.F. carried out all TEM experiments, with supervision from P.C.M. Y.S.S. and H.S. performed the thermal simulations, with supervision from S.X.W. and E.P. T.P., A.E.O.P. and E.P. wrote the manuscript, with input from all authors.

Funding

Open access funding provided by Chalmers University of Technology.

Competing interests

The authors declare the following competing financial interest(s): HORIBA Scientific is the manufacturer of the optical spectroscopy equipment used in this study. Collaboration with industry and academia is a part of A.K.'s job responsibilities. The other authors declare no competing interests.

Additional information

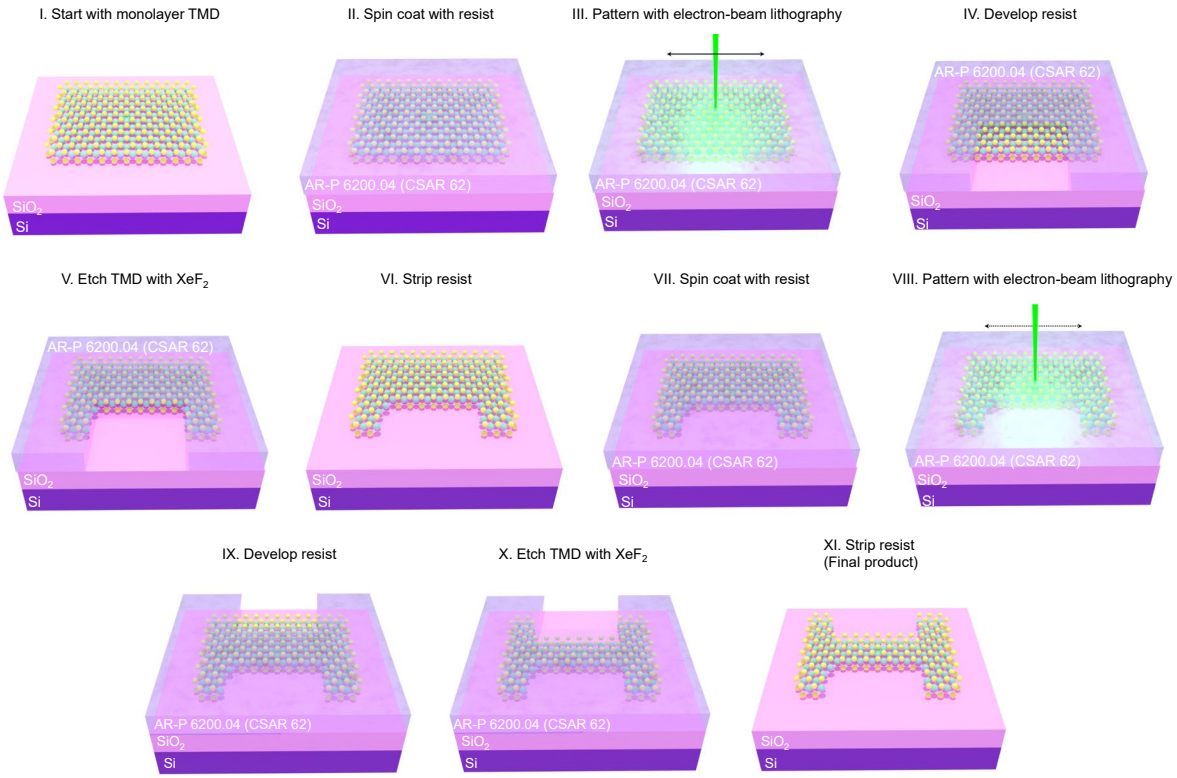
Extended data is available for this paper at https://doi.org/10.1038/s41565-026-02161-w.

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41565-026-02161-w.

Correspondence and requests for materials should be addressed to Tara Peña, Anton E. O. Persson or Eric Pop.

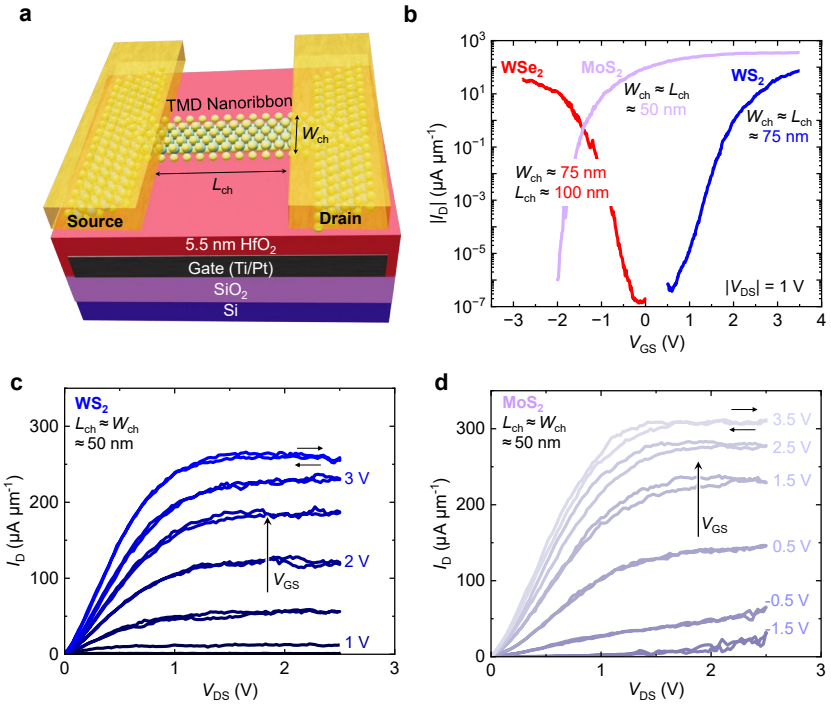
Peer review information *Nature Nanotechnology* thanks Yuan Liu, Peng Zhou and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

https://doi.org/10.1038/s41565-026-02161-w



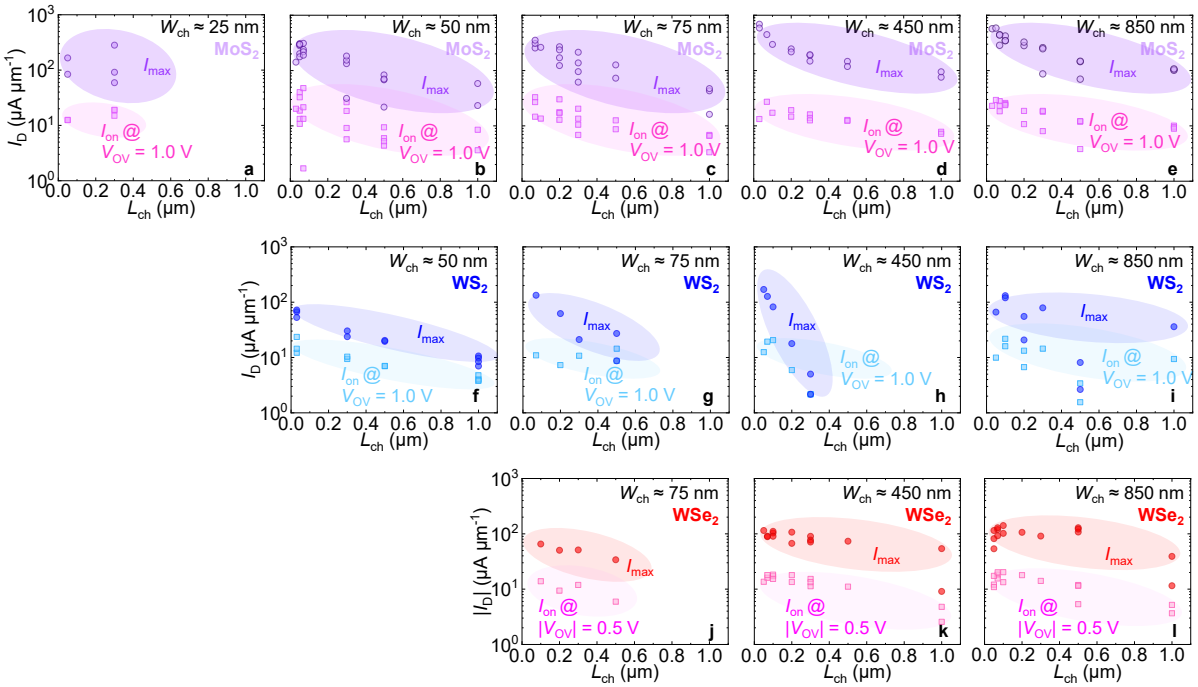
Extended Data Fig. 1 | Litho-etch-litho-etch (LELE) patterning of monolayer TMD nanoribbons. The process involves two sequential e-beam lithography and etch steps. This dual-exposure approach enables sub-30 nm features by overcoming proximity-effect limitations inherent to single-step patterning, while maintaining the same (overall) low dose. See Methods for more information about doses and the low-residue resist used for lithography.

https://doi.org/10.1038/s41565-026-02161-w



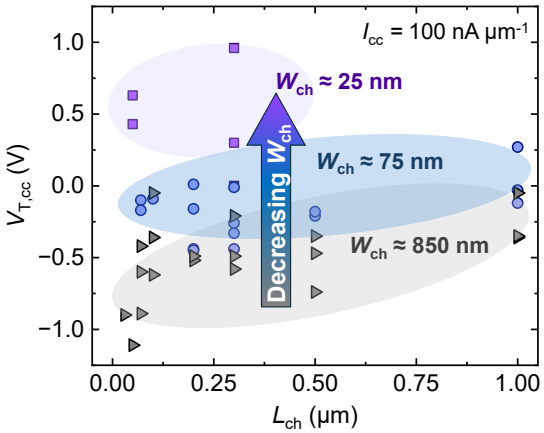
Extended Data Fig. 2 | Off-state current and output characteristics for various monolayer transition metal dichalcogenide (TMD) nanoribbons on 5.5 nm HfO_2 back-gate dielectrics. a, Device schematic, for various TMD nanoribbons with Au contacts on 5.5 nm HfO_2 back-gate dielectric. Note that the HfO_2 dielectric on these test chips was slightly thinner than the 7.5 nm thick HfO_2 used in Fig. 4 of the main text. **b**, Measured transfer characteristics of monolayer MoS_2, WS_2, and WSe_2 nanoribbons with Au source and drain contacts, on local back-gates with high-κ dielectric, including the deep off-state. Note that Au source-drain contacts are optimal for MoS_2 while Ni/Au and Pd/Au are preferable for WS_2 and WSe_2, respectively, explaining the lower on-current densities seen here compared to Fig. 4c in the main text. Nevertheless, these each display I_{max}/I_{min} ratios over 10^8. **c**, Output characteristics of a WS_2 nanoribbon with dimensions and voltages as listed. **d**, Output characteristics of a MoS_2 nanoribbon with dimensions and voltages as listed. Both nanoribbons here had Au source and drain contacts, for direct comparison. (In contrast, WS_2 nanoribbons in main text Fig. 4 had Ni/Au contacts.) Small arrows indicate voltage sweep directions, illustrating small hysteresis. All measurements are at room temperature.

https://doi.org/10.1038/s41565-026-02161-w



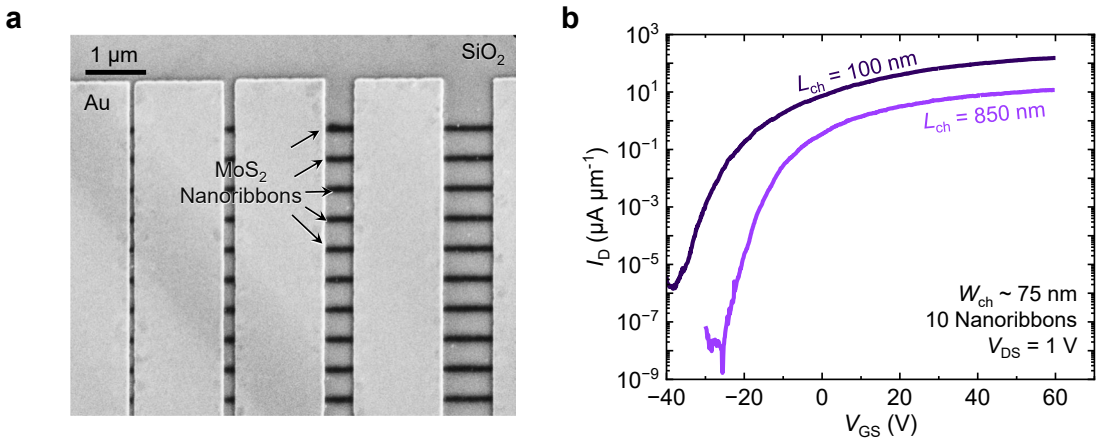
Extended Data Fig. 3 | Width-dependent current density across our monolayer TMDs. Drain current density (I_D) vs. channel length (L_{ch}) for monolayer n-type MoS_2 devices with channel widths (W_{ch}) of approximately **a**, 25 nm, **b**, 50 nm, **c**, 75 nm, **d**, 450 nm, and **e**, 850 nm. Corresponding data for monolayer n-type WS_2 with W_{ch} of approximately **f**, 50 nm, **g**, 75 nm, **h**, 450 nm, and **i**, 850 nm. Corresponding data for monolayer p-type WSe_2 with W_{ch} of approximately **j**, 75 nm, **k**, 450 nm, and **l**, 850 nm. All devices in this figure have Au drain and source contacts, and were fabricated on 5.5 nm HfO_2 with local back-gates (see Extended Data Fig. 2a), measured at $|V_{DS}| = 1$ V. Each panel shows both I_{max} (at maximum $|V_{GS}| = 3$ V for WSe_2 and 3.5 V for the others) and I_{on} at $V_{ov} = |V_{GS} - V_{T,cc}| = 1$ and 0.5 V, for n-type and p-type films respectively, where $V_{T,cc}$ is taken at $I_D = 100$ nA μm^{-1}. Within the device-to-device variability typical of academic nanofabrication, we observe no obvious changes in current density between nanoribbons (left columns) and microribbons (right columns) of a given material, after accounting for V_T changes. The slightly higher I_{max} in wider channels of MoS_2 and WS_2 is due to their lower $V_{T,cc}$ (see Extended Data Fig. 4 for more discussion); accordingly, no obvious nano- vs. microribbon difference is seen in I_{on}. Note, some nanoribbon widths are missing for WS_2 and WSe_2 due to adhesion and yield issues from the layer transfer process onto HfO_2 with local back-gates.

https://doi.org/10.1038/s41565-026-02161-w



Extended Data Fig. 4 | Width-dependent threshold voltage across monolayer MoS_2 nanoribbons. Threshold voltage as a function of channel length and width, for our monolayer MoS_2 devices on HfO_2 from Extended Data Fig. 3a–e. Displayed are devices with channel widths W_{ch} ≈ 850 nm (grey triangles), 75 nm (blue circles), and 25 nm (purple squares). $V_{T,cc}$ is estimated at a constant current of 100 nA μm^{-1}. $V_{T,cc}$ increases as W_{ch} is reduced, causing an apparent decrease of I_{max} for the nanoribbons at maximum V_{GS} (= 3.5 V here on ~5.5 nm HfO_2 back-gate dielectric). Our findings here are consistent with earlier work[49] on thick MoS_2 nanoribbons (~10 layers), which also found increased V_T as W_{ch} is reduced, attributing it to negative charges adsorbed at the edges. Fixed edge charges may arise from fabrication or atmospheric exposure, and are likely below electron energy loss spectroscopy detection limits. On thick back-gate dielectrics (comparable to or thicker than W_{ch}), the relatively higher contribution of fringing fields at the edges could have a competing effect and *decrease* V_T as W_{ch} is reduced, as seen in Supplementary Fig. 3c for devices on 96 nm SiO_2. The analysis here was conducted for the forward-sweep of the transfer curves, however, we note that the hysteresis was quite small for these devices (see Extended Data Fig. 2d), thus rendering the trends here to be robust to either sweep direction.

https://doi.org/10.1038/s41565-026-02161-w



Extended Data Fig. 5 | Electrical performance of monolayer MoS_2 nanoribbon arrays. a, Top-down scanning electron image of the nanoribbon array, showing widths down to ~75 nm and 10 parallel nanoribbons. The devices here are monolayer MoS_2 directly grown and fabricated onto 96 nm SiO_2 on p^{++} Si. In the image, the nanoribbons appear dark, while the lighter large rectangles are the Au contacts. **b**, Measured transfer characteristics of short- and long-channel nanoribbon array devices. The on-state current density is comparable to that of single nanoribbons (see main text Fig. 2a). The off-state current density is one to two orders of magnitude lower than that measured in individual nanoribbons due to the width difference and differences in measurement settings, and comparable to some of the best-known micrometer-scale devices (I_{max}/I_{min} current ratio > 10^9). The short-channel device (100 nm here) exhibits slightly degraded off-state, likely from V_T roll-off and other short-channel effects, on the thicker SiO_2 (96 nm) back-gate oxide.

nature nanotechnology

Supplementary information

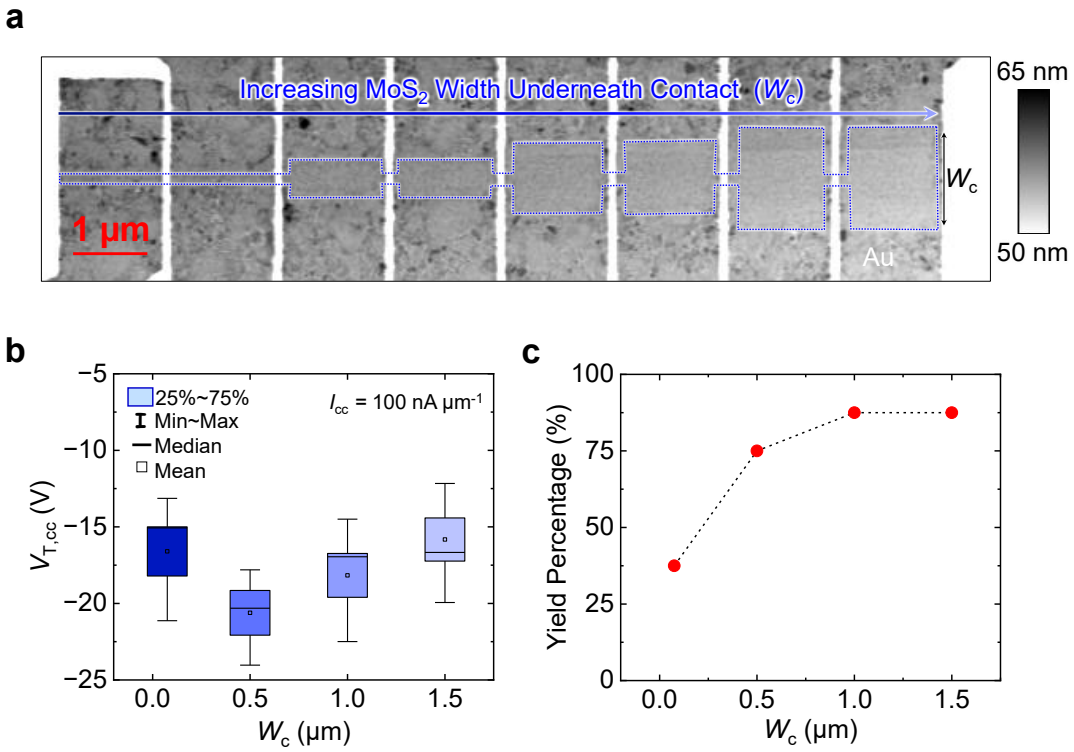
https://doi.org/10.1038/s41565-026-02161-w

Scaling nanoribbon transistors with monolayer transition metal dichalcogenides

In the format provided by the authors and unedited

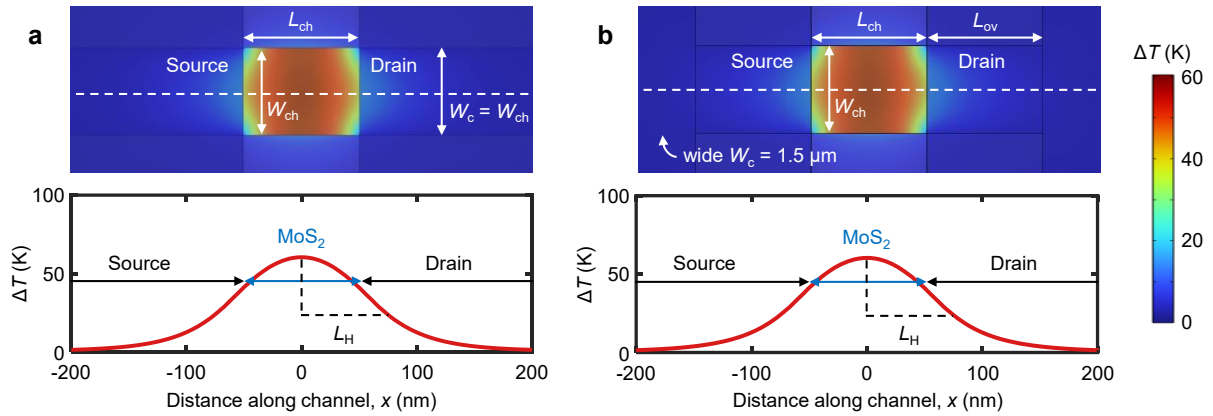
Table of Contents

1. Contact width dependence



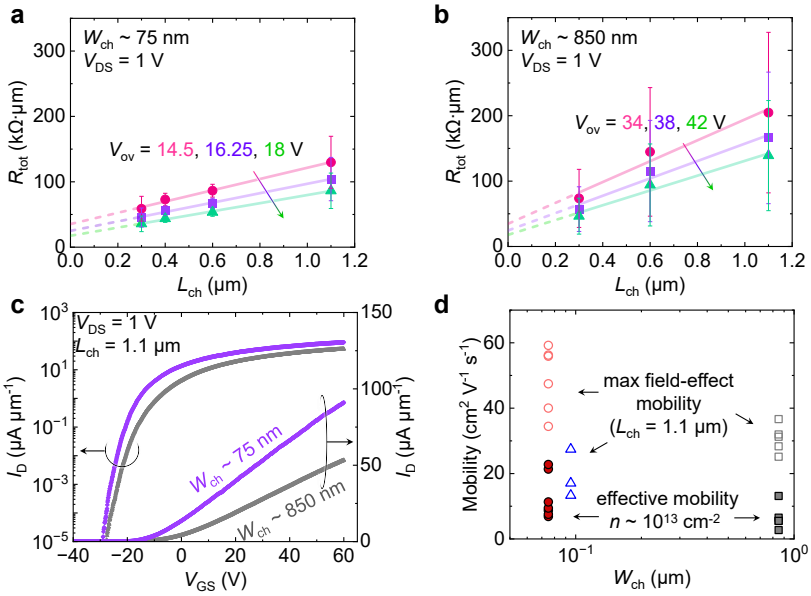
Supplementary Figure 1 | Contact width dependence of monolayer MoS_2 nanoribbon devices. a, Atomic force microscope scan of devices for the contact-width-dependent study on a 96 nm SiO_2 back-gate insulator. Here, only the nanoribbon width is scaled underneath the contacts, from $W_c \approx 75$ nm to 1.5 μm (see blue dotted outline), while the channel width (W_{ch}) and channel length (L_{ch}) are fixed to 75 nm and 100 nm respectively. Note that contacts are the same width in pairs, *i.e.* first two are 75 nm wide (same as nanoribbon channel width, W_{ch}), the next two are 500 nm, and so on. The height or z-axis scale is leveled to emphasize the contact regions, where the Au grains can be visually identified, and the smooth regions indicate where the monolayer MoS_2 is underneath. **b**, Box plot of threshold voltage ($V_{T,cc}$) for the transfer characteristics with varying contact widths (W_c) in main text **Fig. 1b**, extracted at a constant current[1] of I_D = 100 nA μm^{-1}. Each box plot consists of five to six devices. The middle solid line denotes the median value, upper and lower box ranges indicate the higher and lower quartiles, then the upper and lower whiskers highlight the maximum and minimum values. **c,** Yield curve as a function of W_c, for nanoribbons with a $W_{ch} \approx 60$ nm. Here, we employed scanning electron microscopy to visualize the nanoribbons, then documented samples with cracks and delamination as failures. Unless otherwise stated, we use W_c = 1.5 μm for our devices in the rest of the manuscript, because they had the highest yield. We caution that yield in our academic facilities is less indicative of yield in an industrial process, but rather an indication of our ease of fabrication and ability to test multiple (*e.g.,* dozens or hundreds of) devices.

2. Thermal analysis of select nanoribbons



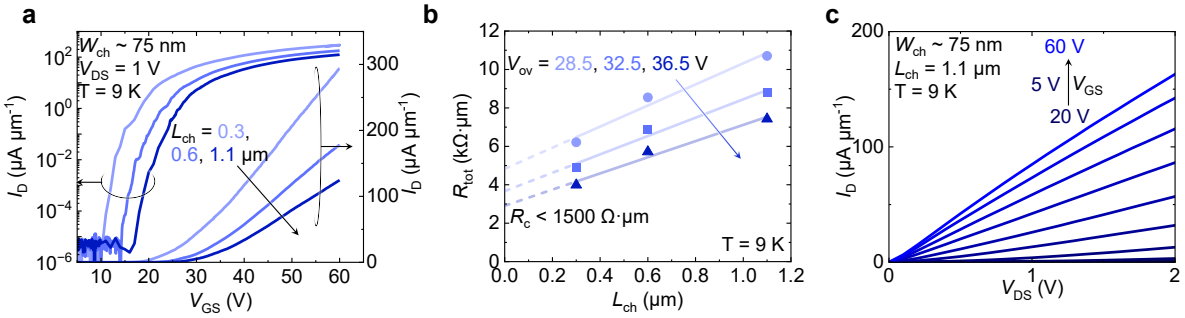
Supplementary Figure 2 | Thermal simulation of monolayer MoS_2 nanoribbon. a, Computed temperature rise (ΔT) for nanoribbon with L_{ch} = 100 nm, W_{ch} = 75 nm on 96 nm SiO_2 thickness, using 'narrow' contact regions, $W_c = W_{ch} = 75$ nm. **b,** Same nanoribbon geometry, but using 'wide' contact regions, W_c = 1.5 μm. Devices correspond to those in **Fig. 1a-c** of the main text, with I_D = 300 μA/μm at V_{DS} = 1 V. Top panels show the temperature distribution map, bottom panels show ΔT along the middle of the channel, dashed line. Heat generation is assumed to be uniform in the channel, and distributed under the contacts with $R_c \approx 1$ kΩ·μm. The power dissipation and ΔT are essentially identical, *i.e.*, the widened W_c does not play an electrical or thermal role. This is largely due to the Au contacts overlapping the nanoribbon channel by $L_{ov} \approx 100$ nm, as in our experimental devices (see main text **Fig. 1a**). The thermal parameters of the simulations are taken from refs.[2,3] and include finite thermal boundary conductance at MoS_2/SiO_2 and MoS_2/Au interfaces. The simulations are insensitive to the 50 nm thick Au contact thermal conductivity in the range 80–120 $Wm^{-1}K^{-1}$, because this is much larger than for the other materials and acts as an efficient heat spreader. The thermal decay length along the nanoribbons is approximately $L_H \approx 78$ nm in both cases.

3. Nanoribbon vs. microribbon monolayer MoS_2 performance comparison



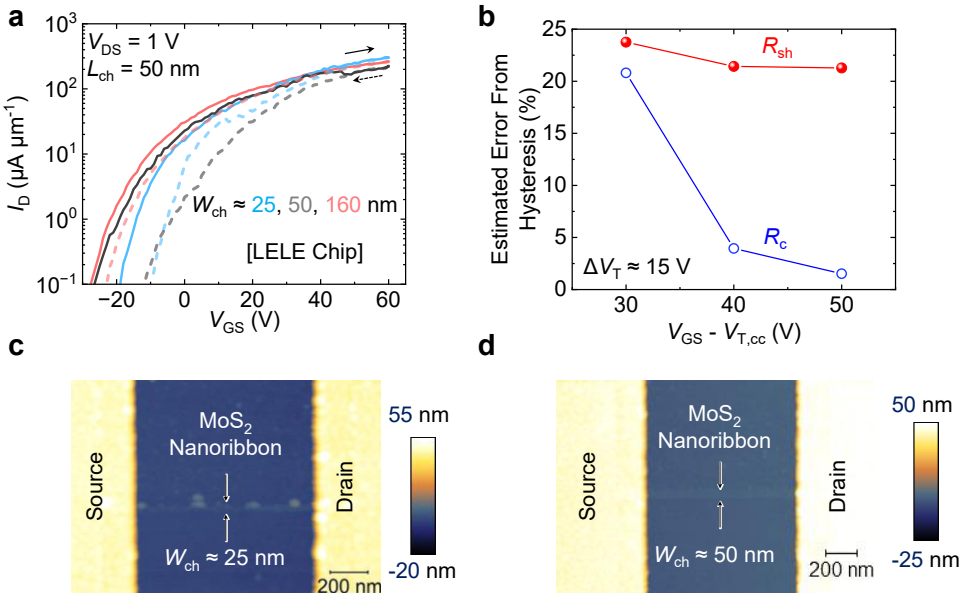
Supplementary Figure 3 | Performance comparison between monolayer MoS_2 nanoribbons and microribbons. Total resistance vs. channel length for **a**, $W_{ch} \approx 75$ nm wide nanoribbons (main text **Fig. 2a-c**) and **b**, wider microribbons on the same chip, with $W_{ch} \approx 850$ nm. Each symbol and error bar represents the average and standard deviation of devices from the same channel length, totaling 30 devices in **a** and 19 devices in **b**. Because W_{ch} of nanoribbons is smaller than the thickness of the back-gate oxide ($t_{ox} \approx 96$ nm here), we account for fringing capacitance using a capacitance per unit area[4] $C_{ox} = \varepsilon_{ox}\left\{\frac{\pi}{\ln[6(t_{ox}/W_{ch}+1)]W_{ch}} + \frac{1}{t_{ox}}\right\}$, where ε_{ox} is the permittivity of SiO_2, and the first term accounts for fringing capacitance while the second term is the typical parallel plate capacitance. This expression reduces to the parallel plate contribution alone when $W_{ch} \gg t_{ox}$. We then estimate the gate-induced carrier density $n \approx C_{ox}(V_{ov} - V_{DS}/2)/q$, where V_{ov} is the gate overdrive ($= V_{GS} - V_T$), V_T is the threshold voltage (estimated at a constant current[1] of $I_D = 0.1$ μA μm^{-1}), and q is the elementary charge. When comparing the total resistance of the nanoribbon vs. microribbon, we find a gate overdrive to match gate-induced carrier densities of 0.8, 0.9, and 1.0 × 10^{13} cm^{-2}. **c**, Measured transfer characteristics of a nanoribbon (purple) and microribbon (gray), here for long-channel devices ($L_{ch} = 1.1$ μm). The same data are shown on log (left) and linear (right) scale. **d**, Estimated mobilities of the nanoribbons vs. microribbons. The field-effect mobility is estimated from long-channel ($L_{ch} = 1.1$ μm) devices, at peak transconductance. The effective mobility is from transfer length method (TLM), estimated at $n \approx 10^{13}$ cm^{-2}. The effective mobility is lower due to the choice of V_T (at constant current) used here. With a linearly extrapolated V_T, the effective mobility would be approximately 20% larger. (See **Supplementary Fig. 5** for additional discussion of uncertainty.)

4. Low-temperature electrical measurements of monolayer MoS_2 nanoribbons on SiO_2



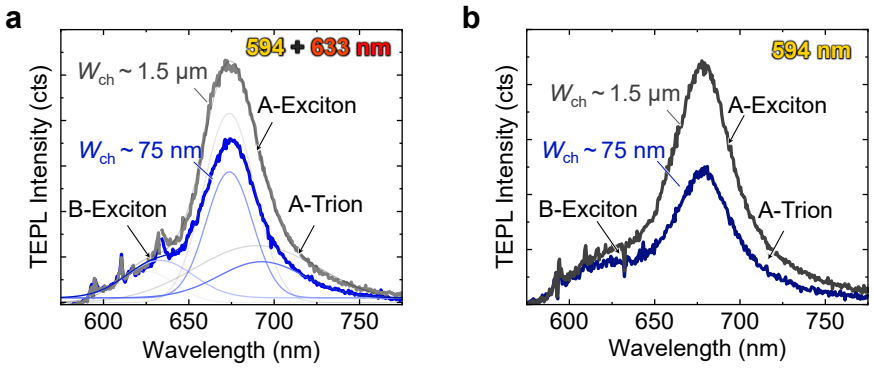
Supplementary Figure 4 | Low temperature measurements of monolayer MoS_2 nanoribbons. a, Transfer characteristics of $W_{ch} \approx 75$ nm wide nanoribbons (main text **Fig. 2a-c**) with varying channel length (L_{ch}, as listed) at $T = 9$ K. **b**, Total resistance vs. channel length for this TLM structure, displaying a contact resistance (R_c) below 1.5 kΩ·µm at the largest gate overdrive. Moreover, we estimate double the mobility (both field-effect and effective) at 9 K compared to room temperature (**Supplementary Fig. 3d**). **c,** Output characteristics of a $W_{ch} \approx 75$ nm wide nanoribbon with $L_{ch} = 1.1$ µm at $T = 9$ K, displaying linear behavior at low bias.

5. Nanoribbon width dependence and hysteresis on multi-patterning (LELE) chip



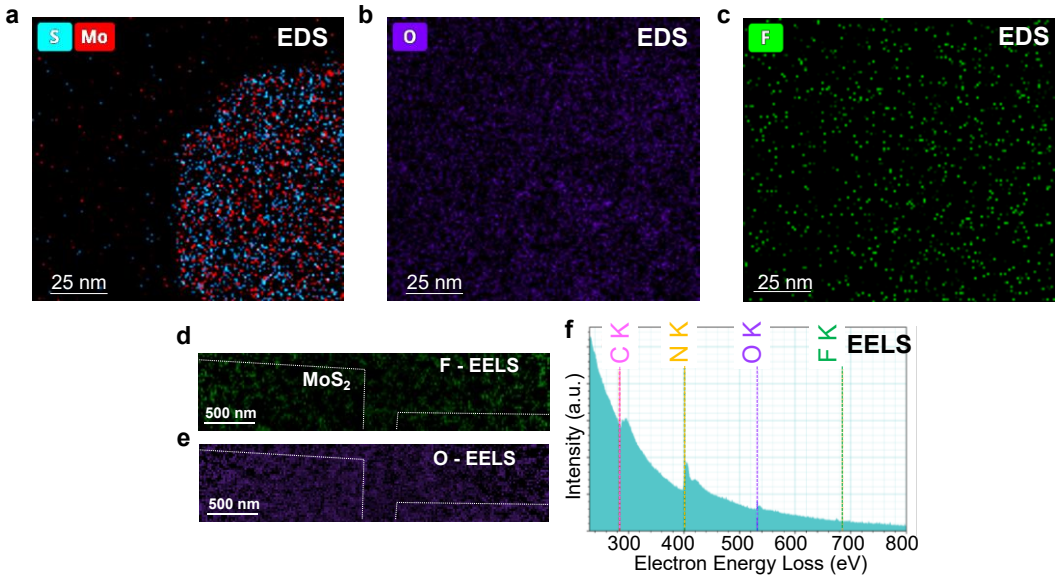
Supplementary Figure 5 | Channel width dependence for monolayer MoS_2 transistors using multi-patterning approach. a, Measured transfer characteristics of nanoribbon devices [main text **Fig. 2d**, multi-patterning or litho-etch-litho-etch (LELE) chip as described in main text **Fig. 1e**] with varying channel width. Here, we do not observe on-state current dependence on the channel width. Instead, signs of variability may arise from contact resistance or monolayer MoS_2 growth variation. Our devices exhibited some clockwise hysteresis[5], as shown in this figure (solid and dashed lines represent forward and backward sweeps respectively). We do not observe a conclusive trend on hysteresis (due to variability) as a function of channel width; however, this hysteresis could impact analysis of R_c and mobility. **b**, Estimated uncertainty for R_c and sheet resistance (R_{sh}) from hysteresis, as a function of gate voltage overdrive, $V_{GS} - V_T$. The estimate is from TLM analysis on a $W_{ch} \approx 50$ nm monolayer MoS_2 channel, where R_c and R_{sh} are calculated from forward and backward sweeps, then the error is their difference divided by their average at the same gate overdrive ($V_{GS} - V_T$). The error from hysteresis reduces at high $V_{GS} - V_T$, as expected, especially for R_c. In other words, hysteresis effects are minimized at high $V_{GS} - V_T \gg \Delta V_T$, rendering conclusions about I_{max} and R_c more robust. The average hysteresis for this structure was $\Delta V_T \approx 15$ V between forward and backward sweeps (at 0.1 μA μm^{-1}), on a 96 nm SiO_2 back-gate dielectric. All transfer curves in this manuscript are the forward sweep, unless otherwise stated. **c**, Atomic force microscopy (AFM) image of 25 nm wide nanoribbon and **d**, AFM of 50 nm wide nanoribbon showing the topography of the devices, both prepared with the multi-patterning approach.

6. Tip enhanced photoluminescence (TEPL) excitation dependence



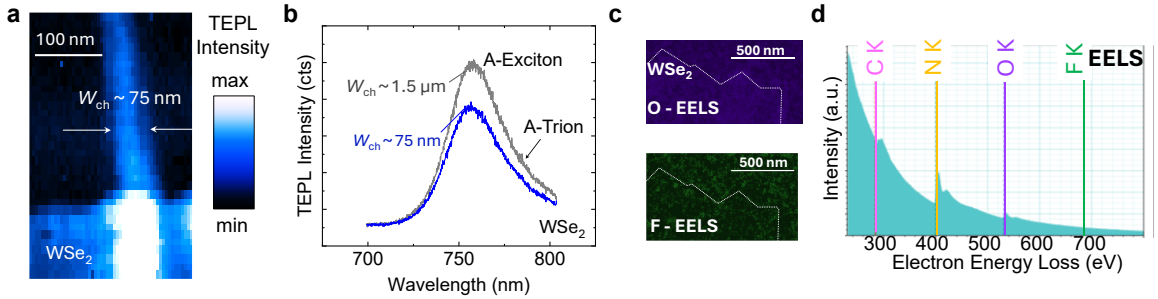
Supplementary Figure 6 | Excitation dependence of tip-enhanced photoluminescence (TEPL) mapping on a 75 nm monolayer MoS_2 nanoribbon. a, Averaged TEPL spectra (thicker line) from **Fig. 3c** in the main text, and corresponding Gaussian peak fittings for the B-exciton, A-exciton, and A-trion (thinner lines). Here, we examine concurrent excitation with both 594 nm and 633 nm lasers. Blue line is taken on the nanoribbon channel ($W_{ch} \approx 75$ nm), gray line is taken for comparison, on a wider region (~1.5 μm). **b**, Averaged TEPL spectra from the same sample, only using the 594 nm excitation laser. We find lower signal-to-noise ratios using only one laser excitation, in addition to a slight change in the peak shapes. The averaging is taken along each respective channel width, from the map in main text **Fig. 3c**.

7. Energy dispersive X-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) at a monolayer MoS_2 nanoribbon corner



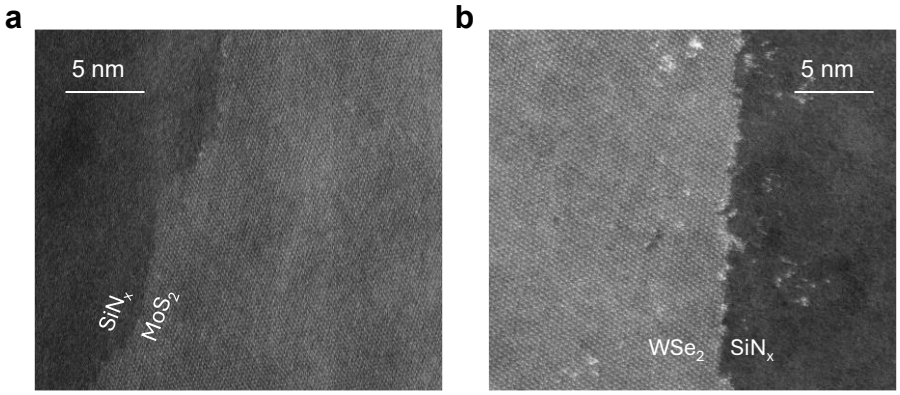
Supplementary Figure 7 | Energy dispersive X-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) of a monolayer MoS_2 nanoribbon corners. a, EDS mapping was conducted in conjunction with scanning transmission electron microscopy experiments. Here, we illustrate a map consisting of the Mo and S atoms, indicating the location of the nanoribbon. The black regions are the thin SiN_x supporting membrane. **b**, EDS mapping of O contribution across the same location as (a), indicating no notable O accumulation on the monolayer MoS_2. **c**, We also examine F signal, suggesting no residual influence along the MoS_2 edges from the etching chemistry. EELS is better suited to examine the presence of low-Z (i.e. low atomic number) elements; therefore, we also examine EELS maps of the **d,** F and **e,** O signals close to two MoS_2 edges (indicated using dotted lines). **f,** Spatially averaged EELS spectrum from the entire map in d-e, showing only weak C, N, O, and F signals altogether.

8. TEPL and EELS analysis on monolayer WSe_2



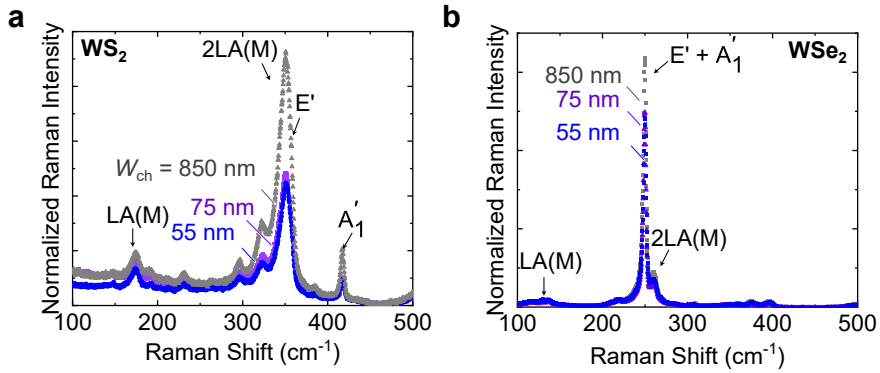
Supplementary Figure 8 | Additional metrology for monolayer WSe_2 nanoribbons and edges. a, TEPL intensity map of a ~75 nm wide WSe_2 nanoribbon, with uniform optical emission along the channel. **b**, Averaged tip-enhanced photoluminescence (TEPL) spectra comparing a nanoribbon channel region to the much wider anchor region of the same WSe_2 nanoribbon, showing minimal broadening of the A-exciton peak and a slight increase in the trion-to-exciton intensity ratio, exactly what is observed for monolayer MoS_2 in **Fig. 3b** in the main text. We note that the TEPL experiments were conducted with both 594 and 633 nm excitation lasers, under the same conditions as **Fig. 3** in the main text. We repeat EELS maps on WSe_2 edges (indicated using dotted lines), displaying the **c,** oxygen and **d,** fluorine signals. **e,** Spatially-averaged EELS spectrum across maps in c-d, showing only weak C, N, O, and F signals.

9. High-angle annular dark-field (HAADF) scanning transmission electron microscopy



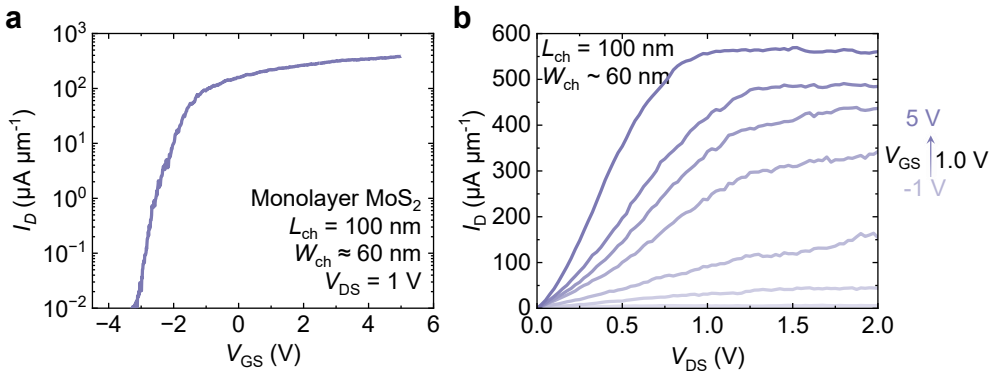
Supplementary Figure 9 | High-angle annular dark-field (HAADF) scanning transmission electron micrograph using an accelerating voltage of 300 kV instead of 80 kV. a, We present another MoS_2 nanoribbon edge, imaged at higher accelerating voltage, demonstrating that the edges are relatively consistent with those presented in **Fig. 3e** of the main text. We note that this imaging configuration is more sensitive to atomic number, thus produces clearer contrast between the monolayer MoS_2 nanoribbon and the SiN_x membrane. Moreover, this nanoribbon edge represents the roughest edge found across the nanoribbon arrays, where the edge roughness here is still a couple of nanometers, as seen in the main text **Fig. 3e**. **b,** HAADF STEM of a monolayer WSe_2 nanoribbon edge, demonstrating that the same processing produces comparable line edge roughness across different TMDs (< 2 nm). The edge quality in these images may be degraded by the layer-transfer process, because the nanoribbons are dry-transferred onto the SiN_x membrane for imaging *after* being patterned (as described in **Methods**). Conversely, for nanoribbon transistors, continuous monolayer films are first grown or transferred onto their substrates *before* being patterned and etched.

10. Micro-Raman spectroscopy on monolayer WS_2 and WSe_2 nanoribbons



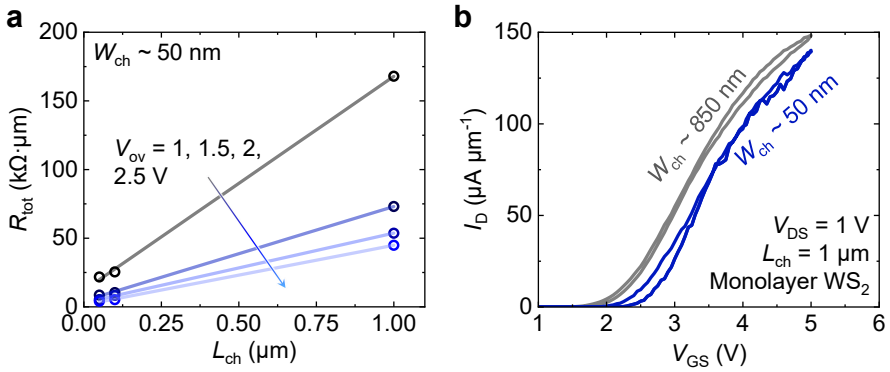
Supplementary Figure 10 | Micro-Raman spectroscopy on monolayer WS_2 and WSe_2 nanoribbons. **a**, Raman spectroscopy on monolayer WS_2 nanoribbons down to 55 nm widths. **b**, Raman spectroscopy on monolayer WSe_2 nanoribbons down to 55 nm widths. We use a 532 nm laser excitation, ~120 μW laser power, and a 1800 l/mm spectrometer grating (same as **Fig. 3a** in the main text). The nanoribbons presented here are from the low equivalent thickness oxide substrates in main text **Fig. 4**, thus continuous monolayer films were transferred onto ~7.5 nm HfO_2 coated SiO_2/Si substrates then patterned into nanoribbons as described in the **Methods** section. We note that the nanoribbons for Raman spectroscopy here were patterned and measured away from the Ti/Pt gate metals. All spectra are normalized to the Si substrate peak at ~520 cm^{-1} (not shown). Importantly, we find that the nanoribbon width does not affect the contribution of defect-mediated peaks[6] [predominantly the LA(M) peaks] across all the 2D monolayers.

11. Output current-voltage characteristics for monolayer MoS_2 nanoribbon on HfO_2



Supplementary Figure 11 | Electrical data of monolayer MoS_2 nanoribbon on thin HfO_2 back-gate dielectric. a, Measured transfer and **b**, output characteristics of the nanoribbon monolayer device on thin HfO_2 (~7.5 nm) back-gate dielectric. The nanoribbon shows current saturation $I_{D,sat} \approx 560$ μA μm^{-1} over a range of voltages $V_{DS} \geq 1$ V, the highest on-state current we observed for monolayer MoS_2 on thin HfO_2 substrates. The device geometry is shown in main text **Figs. 4a-b**. This nanoribbon is slightly wider ($W_{ch} \approx$ 60 nm) than the others shown in **Fig. 4** ($W_{ch} \approx 50$ nm), where all three TMDs are compared.

12. Contact resistance estimate for WS_2 nanoribbons and comparison to microribbons



Supplementary Figure 12 | Pseudo transfer length method analysis of monolayer WS_2 back-gated devices. a, Total resistance vs. channel length (mean values across 15 individual devices with different channel lengths[7]), where we estimate R_c = 675 ± 268 Ω·µm at V_{ov} = 2.5 V. (Extrapolated to L_{ch} = 0 and dividing R_{tot} by two.) These devices are back-gated on ~7.5 nm HfO_2, as shown in main text **Fig. 4a-b**. **b**, Transfer characteristics of microribbon vs. nanoribbon monolayer WS_2 with long channels (L_{ch} = 1 µm), demonstrating similar maximum current density, i.e. no indication of mobility or contact resistance degradation, after accounting for the threshold voltage shift, V_T (the two curves are essentially parallel). We also observe slightly increased V_T with reduced channel width for monolayer MoS_2 nanoribbons on HfO_2, see **Extended Data Fig. 4**.

13. Benchmarking Single-Gate Monolayer TMD Semiconductor Nanoribbons

Ref. #	TMD (all *n*-type if not noted)	W_{ch} (nm)	L_{ch} (nm)	$\|V_{DS}\|$ (V)	$\|I_{max}\|$ (μA/μm)	Mobility @ 293 K ($cm^2V^{-1}s^{-1}$)	Gate Dielectric (all single-gated)	Processing Notes
[8]	MoS_2	30	160	1	2.5	8.5	285 nm SiO_2	Scanning Probe Lithography + XeF_2 etch
[9]	MoS_2	50	500	0.1	2	/	~21 nm hBN	Electron Beam Lithography + SF_6 etch
[10]	MoS_2	50	160	1	29	50	300 nm SiO_2	Electron Beam Lithography + SF_6 etch
[11]	MoS_2	8	1000	1	20	/	SiO_2	Nanoparticle assisted growth
[12]	MoS_2	40	135	0.75	65	/	50 nm SiO_2 1 nm AlO_x + 10 nm HfO_2 Capping	N/A
[13]	MoS_2	60	24	0.95	200	/	~8.5 nm HfO_2	Electron Beam Lithography + etch
[14]	MoS_2	30-40	180	1	485	/	~6 nm HfO_2	Electron Beam Lithography + Cl_2O_2 etch
[15]	WSe_2 (*p*-type)	56	270	1	57	53	285 nm SiO_2	Scanning Probe Lithography + Passivated WO_x edges
[16]	WS_2	20 ± 10 (array)*	10^4	1	0.5	/	300 nm SiO_2	Organic nanostructure mask + O_2 plasma etch
This work	MoS_2	25	100	1	310	/	96 nm SiO_2	Electron Beam Lithography + XeF_2 etch
	MoS_2	43	300	1	620	/	96 nm SiO_2	〃
	MoS_2	75	300	1	400	58	96 nm SiO_2	〃
	MoS_2	75 (array)	100	1	210	/	96 nm SiO_2	〃
	MoS_2	60	50	1	560	/	~7.5 nm HfO_2	〃
	WS_2	50	50	1	420	/	~7.5 nm HfO_2	〃
	WSe_2 (*p*-type)	50	50	1	130	/	~7.5 nm HfO_2	〃

Table S1: Reported $|I_{max}|$ for single-gated monolayer TMD nanoribbons with W_{ch} < 100 nm. Data are shown at highest $|V_{GS}|$ reported and at the V_{DS} as listed (typically 1 V, sometimes less). All nanoribbons were *n*-type except two WSe_2 reports are *p*-type. All measurements were on single nanoribbons except two marked "array" (*for ref. [16] we estimate 10 nanoribbons in the array). The gate dielectric material and thickness, channel dimensions, and some process details are summarized in the table. Our WS_2 (*n*-type) and WSe_2 (*p*-type) channels in the last two rows represent the highest $|I_{max}|$ reported to date for all monolayer nanoribbons of these materials. All three TMD nanoribbons reported here have the highest $|I_{max}|$ to date among single-gate devices. The nanoribbon I_{max} can be further improved with gate-all-around geometry[17,18].

References

1. Ortiz-Conde, A., García Sánchez, F. J., Liou, J. J., Cerdeira, A., Estrada, M. & Yue, Y. A review of recent MOSFET threshold voltage extraction methods. *Microelectron. Reliab.* **42**, 583–596 (2002).
2. Yalon, E., McClellan, C. J., Smithe, K. K. H., Muñoz Rojo, M., Xu, R. L., Suryavanshi, S. V., Gabourie, A. J., Neumann, C. M., Xiong, F., Farimani, A. B. & Pop, E. Energy Dissipation in Monolayer MoS_2 Electronics. *Nano Lett.* **17**, 3429–3433 (2017).
3. Gabourie, A. J., Köroğlu, Ç. & Pop, E. Substrate-dependence of monolayer MoS_2 thermal conductivity and thermal boundary conductance. *J. Appl. Phys.* **131**, 195103 (2022).
4. Liao, A. D., Wu, J. Z., Wang, X., Tahy, K., Jena, D., Dai, H. & Pop, E. Thermally Limited Current Carrying Ability of Graphene Nanoribbons. *Phys. Rev. Lett.* **106**, 256801 (2011).
5. Urban, F., Giubileo, F., Grillo, A., Iemmo, L., Luongo, G., Passacantando, M., Foller, T., Madauß, L., Pollmann, E., Geller, M. P., Oing, D., Schleberger, M. & Di Bartolomeo, A. Gas dependent hysteresis in MoS_2 field effect transistors. *2D Mater.* **6**, 045049 (2019).
6. Mignuzzi, S., Pollard, A. J., Bonini, N., Brennan, B., Gilmore, I. S., Pimenta, M. A., Richards, D. & Roy, D. Effect of disorder on Raman scattering of single-layer MoS_2. *Phys. Rev. B* **91**, 195411 (2015).
7. Smithe, K. K. H., Suryavanshi, S. V., Muñoz Rojo, M., Tedjarati, A. D. & Pop, E. Low Variability in Synthetic Monolayer MoS_2 Devices. *ACS Nano* **11**, 8456–8463 (2017).
8. Chen, S., Kim, S., Chen, W., Yuan, J., Bashir, R., Lou, J., van der Zande, A. M. & King, W. P. Monolayer MoS_2 Nanoribbon Transistors Fabricated by Scanning Probe Lithography. *Nano Lett.* **19**, 2092–2098 (2019).
9. Jiang, J., Doan, M.-H., Sun, L., Ghimire, M. K., Kim, H., Yun, S. J., Yang, H., Duong, D. L. & Lee, Y. H. Schottky-barrier quantum well in two-dimensional semiconductor nanotransistors. *Mater. Today Phys.* **15**, 100275 (2020).
10. Kotekar-Patil, D., Deng, J., Wong, S. L., Lau, C. S. & Goh, K. E. J. Single layer MoS_2 nanoribbon field effect transistor. *Appl. Phys. Lett.* **114**, 013508 (2019).
11. Li, X., Wyss, S., Yanev, E., Li, Q.-J., Wu, S., Sun, Y., Unocic, R. R., Stage, J., Strasbourg, M., Sassi, L. M., Zhu, Y., Li, J., Yang, Y., Hone, J., Borys, N., Schuck, P. J. & Harutyunyan, A. R. Width-dependent continuous growth of atomically thin quantum nanoribbons from nanoalloy seeds in chalcogen vapor. *Nat. Commun.* **15**, 10080 (2024).
12. Panarella, L., Kaczer, B., Smets, Q., Tyaginov, S., Saraza Canflanca, P., Vici, A., Verreck, D., Schram, T., Lin, D., Knobloch, T., Grasser, T., Lockhart de la Rosa, C., Kar, G. S. & Afanas'ev, V. Evidence of contact-induced variability in industrially-fabricated highly-scaled MoS_2 FETs. *Npj 2D Mater. Appl.* **8**, 44 (2024).
13. O'Brien, K. P., Dorow, C. J., Penumatcha, A., Maxey, K., Lee, S., Naylor, C. H., Hsiao, A., Holybee, B., Rogan, C., Adams, D., Tronic, T., Ma, S., Oni, A., Gupta, A. S., Bristol, R., Clendenning, S., Metz, M. & Avci, U. Advancing 2D Monolayer CMOS Through Contact, Channel and Interface Engineering. in *2021 IEEE International Electron Devices Meeting* (2021). doi:https://doi.org/10.1109/IEDM19574.2021.9720651.
14. Lan, H.-Y., Yang, S.-H., Kantre, K.-A., Cott, D., Tripathi, R., Appenzeller, J. & Chen, Z. Reliability of high-performance monolayer MoS_2 transistors on scaled high-κ HfO_2. *Npj 2D Mater. Appl.* **9**, 5 (2025).
15. Chen, S., Zhang, Y., King, W. P., Bashir, R. & van der Zande, A. M. Edge-Passivated Monolayer WSe_2 Nanoribbon Transistors. *Adv. Mater.* **36**, 2313694 (2024).
16. Aslam, M. A., Tran, T. H., Supina, A., Siri, O., Meunier, V., Watanabe, K., Taniguchi, T., Kralj, M., Teichert, C., Sheremet, E., Rodriguez, R. D. & Matković, A. Single-crystalline nanoribbon network field effect transistors from arbitrary two-dimensional materials. *Npj 2D Mater. Appl.* **6**, 76 (2022).
17. Jaikissoon, M., Buragohain, P., Mortelmans, W., Oguz, K., Rogan, C., Lux, J., Kitamura, A., Engel, C., Vreeland, R. F., Barnett, H., Brooks, Z., Harlson, S., Pinnepalli, S. S. K., Gillispie, E., Toku, K., Wilson, T., Oni, A., Penumatcha, A. V., Dorow, C. J., Kavrik, M., Kozhakhmetov, A., Maxey, K.,

Arefin, N., Kevek, J., Tronic, T., Metz, M., Clendenning, S. B., O'Brien, K. P. & Avci, U. Record PMOS WSe_2 GAA Performance Using Contact Planarization, and Systematic Exploration of Manufacturable, High-Yield Contacts. in *2025 Symposium on VLSI Technology and Circuits* (2025). doi:10.23919/VLSITechnologyandCir65189.2025.11075202.

18. Mortelmans, W., Buragohain, P., Kitamura, A., Dorow, C. J., Rogan, C., Siddiqui, L., Ramamurthy, R., Lux, J., Zhong, T., Harlson, S., Gillispie, E., Wilson, T., Toku, R., Oni, A., Penumatcha, A., Kavrik, M., Jaikissoon, M., Maxey, K., Kozhakhmetov, A., Cheng, C.-Y., Lin, C.-C., Lee, S., Vyatskikh, A., Arefin, N., Kencke, D., Kevek, J., Tronic, T., Metz, M., Clendenning, S. B., O'Brien, K. P. & Avci, U. Gate Oxide Module Development for Scaled GAA 2D FETs Enabling SS<75mV/d and Record I_{dmax}>900μA/μm at L_g<50nm. in *2024 IEEE International Electron Devices Meeting* (2024). doi:https://doi.org/10.1109/IEDM50854.2024.10873417.