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Effect of Carbon Nanotube Network Morphology on Thin Film Transistor Performance

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ABSTRACT

The properties of electronic devices based on carbon nanotube networks (CNTNs) depend on the carbon nanotube (CNT) deposition method used, which can yield a range of network morphologies. Here, we synthesize single-walled CNTs using an aerosol (floating catalyst) chemical vapor deposition process and deposit CNTs at room temperature onto substrates as random networks with various morphologies. We use four CNT deposition techniques: electrostatic or thermal precipitation, and filtration through a filter followed by press transfer or dissolving the filter. We study the mobility using pulsed measurements to avoid hysteresis, the on/off ratio, and the electrical noise properties of the CNTNs, and correlate them to the network morphology through careful imaging. Among the four deposition methods thermal precipitation is found to be a novel approach to prepare high-performance, partially aligned CNTNs that are dry-deposited directly after their synthesis. Our results provide new insight into the role of the network morphologies and offer paths towards tunable transport properties in CNT thin film transistors.

KEYWORDS

Carbon nanotube network, thin film transistor, morphology, mobility, image processing, hysteresis

1. Introduction

Carbon nanotube networks (CNTNs) are a unique class of materials demonstrating great potential for thin film transistor (TFT) applications with electrical characteristics that exceed those of amorphous Si and organic semiconductors. TFTs based on single-walled CNTNs have achieved a competitive position among flexible electronics, showing the potential to become ubiquitous for a broad range of applications such as low-cost lightweight and flexible displays, smart materials, and radio-frequency identification tags [1–3]. These macroelectronic applications benefit from the outstanding intrinsic properties of single-walled carbon

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nanotubes (CNTs) within the network. However, low temperature and cost-effective device manufacturing processes are still required for their utilization in commercial products.

Numerous CNT synthesis methods have been reported, yet no single method has emerged to realize industrial-scale production of flexible CNT macroelectronics. Substrate-supported chemical vapor deposition (CVD) synthesis of CNTs enables architecture and structure control [4, 5], but it is not compatible with plastic substrates due to high temperature processing (~900 °C). Solution depositions of CNTNs onto arbitrary substrates are beneficial for applications in flexible electronics, allowing the fabrication of semiconductor-enriched single-walled CNT samples [6–12]. However, such techniques suffer from challenges in deposition efficiency and uniformity due to the aggregation of CNTs and time-consuming process steps. Solution processing can also reduce individual CNT lengths and degrade intrinsic CNT properties due to solvent and surfactant contamination. In contrast, we have recently demonstrated a low-temperature deposition technique of pristine CNTs using an aerosol (floating catalyst) CVD method. This approach allows direct dry printing of single-walled CNTs grown in the gas-phase onto any substrate at room temperature without additional process steps [3, 13, 14]. The technique could enable many CNTN applications [3, 14, 15], but to date there have been few studies on the effect of CNTN morphology on the electrical characteristics of CNT TFTs [16, 17]. Rouhi et al. [16] have investigated the effects of CNT density on the performance of TFTs fabricated from purified semiconducting CNT solutions, and Sangwan et al. [17] have examined the effects of CNTN density and device length on TFT performance using mixed networks of metallic and semiconducting CNTs grown by CVD directly on SiO_2. Other studies related to the optimization of transistor performance by tuning CNT alignment [18–20] suggest that the ability to understand and engineer the CNT arrangement within the network is important to control the performance of CNT TFTs.

In this study we investigate the impact of CNTN morphology on TFT performance using as-synthesized aerosol single-walled CNTs. We define morphology to include CNT density, arrangement of CNTs within the network or network layout (e.g. curliness/alignment), and CNT–CNT junction density, all of which are expected to affect transport in the CNTN. We control the network morphology by using four different deposition methods of the CNTs, keeping the deposition time and synthesis conditions the same. Importantly, the single-walled CNTs within the CNTNs have similar overall quality, type and structural properties, allowing us to compare the four deposition techniques and specifically understand the effect of morphology on TFT performance. Our results indicate that controlling the morphology via the CNT deposition method allows tuning of the performance of CNT TFTs.

2. Experimental

The single-walled CNTs used in this study were synthesized by an atmospheric pressure aerosol CVD technique, as described in detail elsewhere (see the Methods section for additional information) [21], and they were collected onto a substrate held at room temperature immediately following growth. We employed four different techniques to deposit CNTN material onto SiO_2/Si substrates for TFT fabrication, as illustrated in Fig. 1. The first method is a dry deposition technique which guides aerosol-synthesized CNTs in an electric field directly to the substrate using an electrostatic precipitator (ESP). An ESP is a highly efficient collection device widely used in aerosol sampling, which was recently employed for CNT collection [13, 22]. Figure 1(a) schematically illustrates the ESP-based deposition method.

Our second CNT deposition technique requires a thermal precipitator (TP), previously used for nanoparticle collection [23]. Our work is the first to demonstrate that a TP can be successfully employed for direct CNT deposition onto any substrate. Figure 1(b) shows the TP-based deposition method in more detail. The basis for the TP method is thermophoresis, i.e. the diffusion of aerosol particles in a temperature gradient from high- to low-temperature zones of the gas [24]. The TP method uses a heated element (T = 393 K) and a cooled surface (T = 283 K) onto which the CNTs are deposited. This is an effective technique for

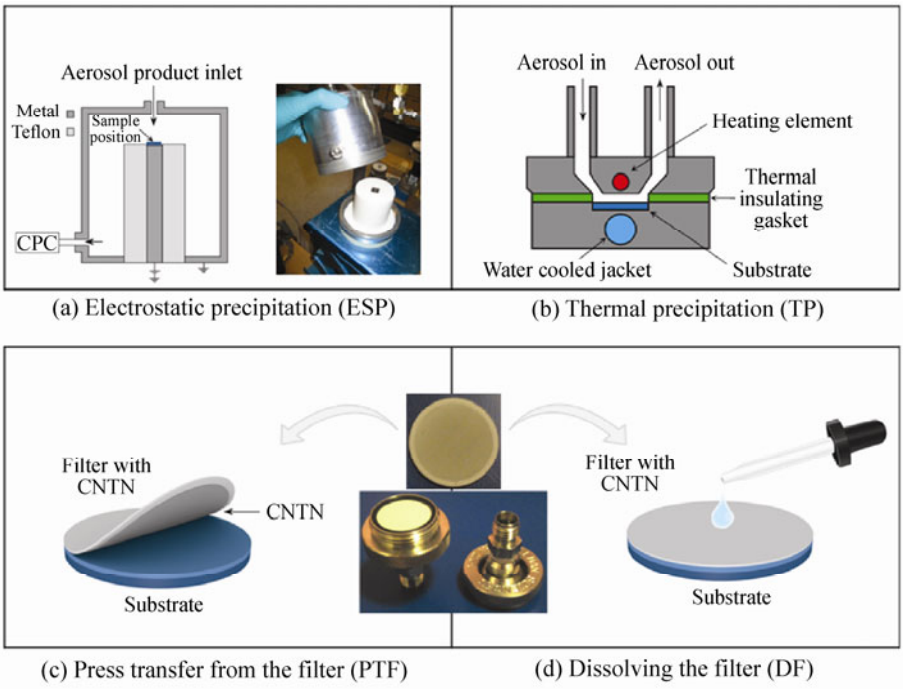

Figure 1 Schematic illustration of the four CNTN deposition methods used in this study, which largely define the morphology of the network: (a) electrostatic precipitation (ESP); (b) thermal precipitation (TP); (c) press transfer from the filter (PTF); (d) dissolving the filter (DF)

dry deposition of CNTs directly downstream from the synthesis reactor, enabling the use of flexible temperature-sensitive substrates.

The other two CNTN deposition methods are based on capturing CNTs directly from the gas-phase by flow filtration and subsequently transferring the CNTN onto the receiving substrate of interest. We use nitrocellulose membrane filters as collection media for CNTNs. The networks are transferred to a substrate at room temperature either by simple press transfer from the filter (PTF) or by dissolving the filter (DF) in acetone [3, 14]. Both of these deposition techniques are schematically shown in Figs. 1(c) and 1(d), respectively. In the former method the CNTN is simply pressed (with a pressure on the order of 10^3 Pa) and transferred to practically any material due to the poor CNTN adhesion to the nitrocellulose filter [14]. In the latter method, we place the filter onto the substrate and transfer the CNTN by dissolving the filter on the substrate surface with an acetone bath [3]. Both methods are simple, versatile, and economical means of CNTN preparation on various substrates with no dispersion or purification steps required prior to the transfer (see Fig. S-1 in the Electronic Supplementary Material (ESM)).

We collect all the CNTNs on the same CNT synthesis day, using the same CNT synthesis conditions. This approach ensures the consistency of individual single-walled CNT structural properties. No additional CNT processing, CNTN modification, or wafer treatment prior to nanotube deposition is employed. The density of the CNTN for all deposition methods can be adjusted by varying the CNT collection time. We have used the same CNT deposition time of 10 s, resulting in comparable CNTN densities amongst all the collection methods as verified later.

3. Results and discussion

3.1 Electrical properties

CNT TFT characteristics are typically evaluated and compared by their field-effect mobility (the average charge carrier drift velocity per unit electric field, μ_{FE}) and I_{ON}/I_{OFF} ratio (the ratio between device "on" state current, I_{ON}, and "off" state current, I_{OFF}) [25], with the

goal of achieving larger values for these performance metrics simultaneously.

To understand how CNTN morphology affects the electrical properties of CNTN-based devices, we fabricated bottom-gated TFTs on 100 nm of SiO_2, as shown in Fig. 2. These devices allow electrical measurements as well as careful imaging of the network morphology, as we show in Section 3.2. We used CNT TFTs with the same width and length ($W = L = 50$ μm), comprised of randomly distributed individual single-walled CNTs and small bundles (2–7 single-walled CNTs per bundle from transmission electron microscopy (TEM) observations). The average tube diameter was ~1.3 nm based on optical absorption measurements (see Fig. S-2 (in the ESM)). We measured the transfer characteristics (I_D–V_{GS}) of our CNT TFTs at a constant drain-to-source bias, $V_{DS} = -1$ V. All such devices exhibit hysteresis between the forward and reverse DC gate-voltage sweeps (Fig. 2(b) and Fig. S-3 (in the ESM)) due to charge trapping in the supporting dielectric and adsorbed water molecules [26, 27]. However, the hysteresis is almost completely eliminated by using pulsed characterization techniques as shown in Fig. 2(b) [27, 28]. Here, we extract the carrier mobility using both the forward and reverse DC voltage sweeps, as well as a pulsed gate voltage technique. The mobility is $\mu_{FE} = g_m L/(WC_{OX}V_{DS})$, where $C_{OX} = 3.45 \times 10^{-8}$ F/cm^2 is the gate capacitance per unit area calculated from the parallel plate model and g_m is the peak transconductance (dI_D/dV_{GS}). We note the parallel plate capacitance results in an underestimation of μ_{FE} for low density CNTNs and a more accurate approach would be to directly measure the gate capacitance of CNT TFTs under investigation [2, 29, 30].

To calculate the I_{ON}/I_{OFF} ratio, we use I_{ON} at a constant gate-voltage overdrive from the forward sweep (V_{GS}–$V_{TH,FWD} = -5$ V) and take I_{OFF} as the minimum I_D from the same transfer curve. This approach allows

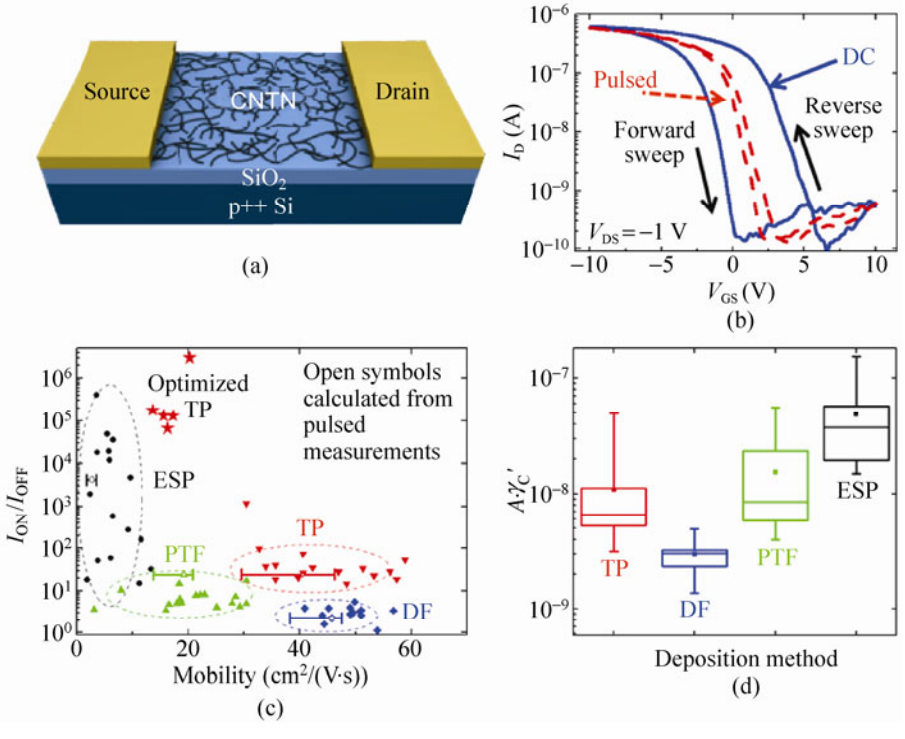

Figure 2 (a) Schematic view of a typical CNT TFT device. (b) Typical I_D–V_{GS} characteristics of ESP-deposited CNTN devices using DC and pulsed characterization under ambient conditions. (c) Comparison of mobility and I_{ON}/I_{OFF} ratio of CNT TFT devices, where the transistor channel is comprised of a random CNTN, grown under the same CNT synthesis conditions and deposited by the four methods directly after synthesis. The star symbols indicate TP-deposited devices optimized under a different collection time (see ESM, Fig. S-9). Error bars highlight the effect of hysteresis on mobility calculations (right side-forward sweep, left side-reverse sweep). (d) 1/*f* noise amplitude distribution normalized by CNTN fill factor (γ_C') reported in Table 1. The whiskers of the box plot represent the minimum and maximum of the data

for a better comparison of device performance across deposition techniques, as it compares all devices at similar charge densities and reduces variability due to V_{TH} shift.

Figure 2(c) shows the calculated μ_{FE} of CNT TFTs from the forward sweep DC transfer characteristics (solid symbols and right side error bars) for the different deposition techniques. We note the forward sweep DC measurement overestimates μ_{FE} compared to the reverse sweep and pulsed measurements (left side error bar and open symbols, respectively), similar to previous work on individual CNT devices [27]. Nevertheless, using the forward sweep DC transfer curve and the parallel plate C_{OX} allows for direct comparison of our devices with other reports in the literature [3, 8]. However, we suggest that in future studies the community should adopt pulsed measurement methods when hysteresis cannot be eliminated during fabrication, in order to correctly extract the intrinsic mobility of such CNTNs [28].

Our results demonstrate that the electrical properties of CNT TFTs vary significantly with the CNTN deposition method used. Devices fabricated from CNTNs deposited by ESP exhibit the best performance in terms of I_{ON}/I_{OFF} (up to ~5×10^5) but typically have lower $\mu_{FE} \approx 2$–13 cm^2/(V·s). CNT TFTs fabricated using the PTF deposition method typically have higher $\mu_{FE} \approx$ 3–30 cm^2/(V·s) and lower $I_{ON}/I_{OFF} \approx 6$–20 in comparison with ESP devices. The DF deposition method results in CNT TFTs with low $I_{ON}/I_{OFF} \approx 2$–8, but high $\mu_{FE} \approx$ 40–50 cm^2/(V·s). We also report the first measurements of CNTN devices fabricated using direct deposition of CNTs by TP. These devices show good potential for further development with high $\mu_{FE} \approx 30$–60 cm^2/(V·s), comparable to DF-deposited devices, and higher I_{ON}/I_{OFF} ratio ≈ 20–1100 (for optimized densities $I_{ON}/I_{OFF} \approx 10^5$–$10^6$ and $\mu_{FE} \approx 15$–20 cm^2/(V·s) concurrently, as discussed further). We note that μ_{FE} of CNT TFTs with different CNTN morphologies display similar temperature dependent behavior in the range between 80–300 K; however further investigation and detailed modeling are needed to fully understand the temperature dependence of mobility in CNTNs (Fig. S-4 in the ESM).

Figure 2(d) shows the analysis of the noise spectrum, and specifically 1/*f* noise behavior of our CNT TFTs fabricated using various CNTN deposition methods. The 1/*f* noise level is measured by first DC biasing the devices in series with a current amplifier. The output from the amplifier is then measured by a spectrum analyzer which provides the voltage noise spectral density S_V. The 1/*f* noise level is further separated from the thermal noise by measuring a control device. Values of both the noise amplitude (S_V) and the exponent (α) are calculated from $S_V/V^2 = A/f^{\alpha}$ [31]. For almost all of the CNTN devices measured, $\alpha \approx 0.9$–1.1 (very close to 1). However, A varies significantly for different types of network morphologies, as shown in Fig. 2(d) and Fig. S-5 (in the ESM). It has been shown that 1/*f* noise in CNTNs depends strongly on various parameters such as device dimensions and nanotube density [32, 33]. Therefore, the significant variation in A, especially between ESP and DF networks, is likely a result of different network properties. Interestingly, after normalizing A with respect to the CNTN area fill factor, representative of network density (as described below and in the Methods section), the A values are still different, despite the same device dimensions. This indicates that the different morphologies of the networks play a significant role in determining both the resistance and noise levels of the device. Indeed, values of A normalized by corresponding device resistance R (which include both the density and morphology effects) are very similar for different types of deposition methods (Fig. S-5 (in the ESM)).

3.2 Network characterization

A CNTN is comprised of randomly distributed conduction pathways that percolate from the transistor source to drain. Earlier studies have revealed that the overall network conductivity is mainly controlled by the junctions between CNTs or between CNT bundles [34–38]. Previous investigations of CNT TFT transport have shown the importance of keeping the number of tube-to-tube junctions along the percolation paths to as few as possible by increasing alignment and using longer CNTs, while at the same time preserving a small level of misalignment within the network, to achieve the highest TFT network performance [18, 20, 39]. CNT TFTs in our study have an average CNT bundle length $L_{CNT} \approx 5.4$ μm (Fig. S-2 (in the ESM)). This is achieved by fixing the CVD reactor conditions during the single-walled CNT synthesis, as recently demons-

trated by *in situ* sampling experiments [40]. Despite the same synthesis conditions, the resulting CNTNs possess very different morphology after subsequent deposition onto the substrates by one of the four methods previously described.

We analyze the CNTN morphology by scanning electron microscopy (SEM) and atomic force microscopy (AFM), aided by image analysis software (MATLAB and Gwyddion) [41, 42]. Figure 3 shows SEM images of the morphologies obtained after the four CNT deposition methods; these clearly yield different arrangement of CNTs and CNT bundles within the network, deeply influencing the electrical properties summarized in Fig. 2. We then assess the morphology by analyzing the CNTN density or device area fill factor (γ_C), CNT bundle density, CNTN junction area fill factor (γ_J), and CNT alignment, similar to a previous study [43]. Figure 4 shows our morphology analysis for the TP deposition method as an example (for additional information, see the Methods section and Figs. S-6–S-8 (in the ESM)). Figure 4(a) gives a SEM image of a CNTN from TP deposition, and its inset shows the thresholded area coverage of the network [43]. These figures allow us to estimate γ_C, i.e. the area occupied by CNTs within the TFT channel. Further, we can extract a more realistic fill factor value (γ_C'), correcting for the CNT diameter overestimation under SEM (see the Methods section for more information) [43]. The CNT diameter distribution from AFM analysis of our samples is given in Fig. 4(b), with d_{avg} = 3.9 nm ± 1.8 nm for TP-deposited CNTN (see also Figs. S-6–S-8 (in the ESM)). The large values can be attributed to CNT bundling, as verified by SEM and TEM. Consequently, we determine an average $\gamma_C' \approx$ 0.0155 of TP-deposited CNTNs, obtained from several SEM images of the measured devices, to account for slight density variations across the sample. Dividing the area of the CNTN, $A_C = \gamma_C' \cdot A$ (where A is the device channel area), by the average area of a CNT bundle, $A_{CNT} = d_{avg} \cdot L_{CNT}$, provides an estimate for the total number of CNT bundles in the CNTN. This parameter is more readily used in numerical simulations of CNTN transport [44].

Figure 4(c) highlights the CNT junctions for the

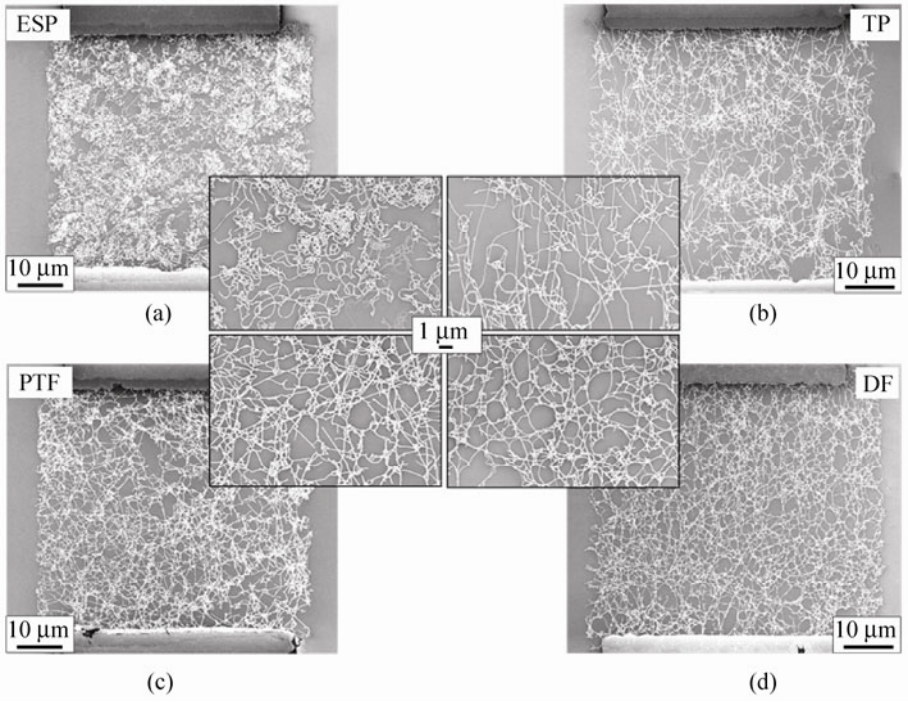

Figure 3 SEM images showing the morphology of CNTNs in a transistor channel ($W = L$ = 50 μm) formed on a SiO_2/Si substrate by four different CNTN deposition techniques: (a) CNTN deposited by electrostatic precipitation (ESP); (b) CNTN deposited by thermal precipitation (TP); (c) CNTN deposited by press transfer from a filter (PTF); (d) CNTN deposited after dissolving the filter (DF). Insets in the center show higher magnification SEM images corresponding to each deposition technique

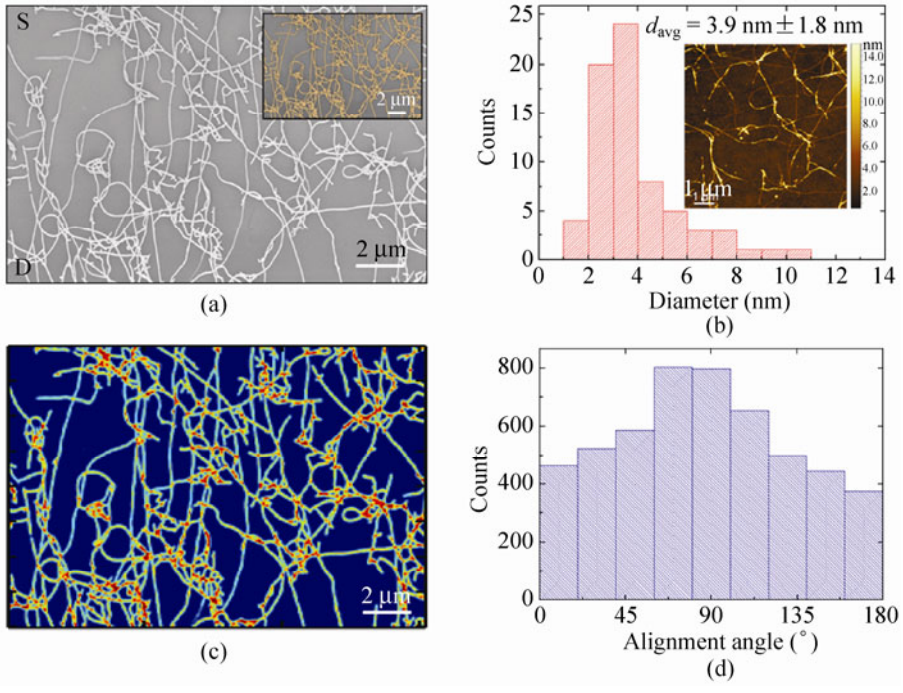

Figure 4 Image analysis of CNTN morphology after thermal precipitation (TP) deposition. (a) SEM image of a TP-deposited channel. Inset: intensity thresholding performed with image analysis software highlighting the CNTN. (b) Diameter distribution of 70 randomly selected CNTs in a TP-deposited CNT TFT from AFM analysis. Inset: AFM image of CNTN deposited by TP. (c) Junction analysis of TP-deposited CNTN. (d) Angle distribution of several TP-deposited CNTNs analyzed using image analysis software

TP-deposited CNTN, with the junctions appearing in bright red. These selected junctions allow us to calculate the junction area fill factor (γ_J) relative to the area covered by the CNTN. The CNT or bundle junctions are known to be the most resistive parts of a CNTN [37], especially due to Schottky barriers formed at junctions between metallic and semiconducting CNTs [45]. From Fig. 4(c) we estimate $\gamma_J = 0.066 \pm 0.041$, as a conservative overestimate due to the spatial resolution of the SEM image as well as processing techniques (see the Methods section for more information). Furthermore, Fig. 4(d) gives the alignment angle distribution for the TP-deposited CNTN, with 0° and 90° corresponding to the rightward and upward directions of Fig. 4(a), respectively. The upward direction (90°) corresponds to the transistor channel orientation along the direction of the aerosol flow in TP. The distribution has a mean near 90°. Nevertheless, the standard deviation (σ) is a better metric of the overall alignment, as the mean alignment value will depend on the position of the SEM electron beam relative to the sample. We find the TP-deposited CNTN has the smallest standard deviation $\sigma_{TP} = 47.3°$, being the most highly aligned of all the CNTNs deposited by the four methods (see Fig. 5(a) and the ESM). Higher CNTN alignment levels correspond to fewer CNT junctions, leading to higher network conductivity, and charge carrier mobility in CNT TFTs. Table 1 summarizes the CNTN morphology analysis of all the four deposition methods.

After contrasting the morphology of CNTNs and electrical characteristics of network transistors, we discuss how CNT arrangement within the network influences the device performance. We find that TP-deposited CNTs result in a higher degree of alignment in the direction of the aerosol flow as compared to other deposition techniques. This is also evident in Fig. 5, which presents the CNT alignment distributions for all the four deposition techniques (Fig. 5(a)) and relates μ_{FE} to γ_J (Fig. 5(b)). We find that higher alignment of conductive pathways along the TFT channel and fewer junctions along the current flow paths improve the performance of TP-deposited CNT TFTs (up to $\mu_{FE} \approx 60$ cm^2/(V·s)) relative to those deposited with other methods. Furthermore, decreased bundle diameter of

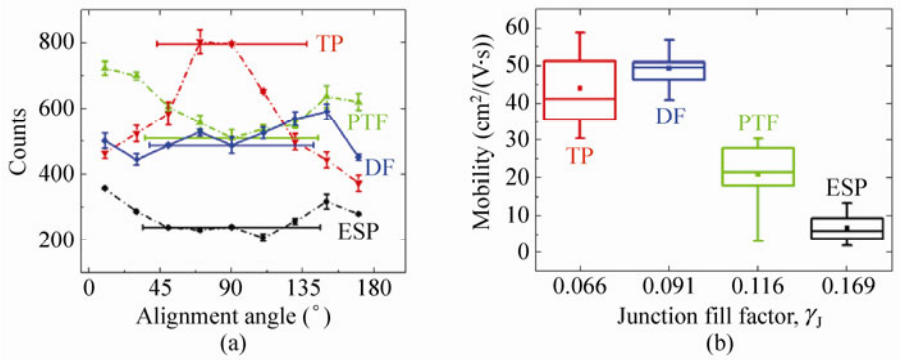

Figure 5 (a) CNTN alignment distributions for all deposition techniques. The data are the ensemble of several different SEM scans, which also give the error bars in the count number. Error bars in the alignment angle correspond to the standard deviation of each distribution, a strong indicator of overall network alignment. TP-deposited CNTNs have the highest alignment, followed by DF, PTF, and ESP. (b) Mobility as a function of junction fill factor (γ_J) showing that CNTNs with higher junction density have lower mobility. The whiskers of the box plot represent the minimum and maximum of the data

Table 1 Comparison of CNTN morphologies as-deposited by the four different methods

CNTN deposition method	Average bundle diameter (nm)	CNTN fill factor, γ_C'	Angle (°)	Junction fill factor, γ_J	Bundle density (#/μm^2)
Thermal precipitation (TP)	3.9 ± 1.8	0.0155	97.1 ± 47.3	0.066 ± 0.041	0.74
Electrostatic precipitation (ESP)	4.4 ± 1.9	0.0278	89.3 ± 55.9	0.169 ± 0.024	1.17
Press transfer from the filter (PTF)	5.2 ± 2.0	0.0256	88.1 ± 54.6	0.116 ± 0.062	0.91
Dissolving the filter (DF)	5.5 ± 2.7	0.0251	92.2 ± 51.7	0.091 ± 0.033	0.84

as-deposited CNTs can also contribute to lower junction resistance, increasing the overall CNTN conductivity [37]. These results demonstrate that TP is a preferred method for direct and dry CNTN deposition for TFT applications.

In contrast, CNTs and CNT bundles deposited directly onto the substrate by ESP under the influence of an applied electrical potential tend to exhibit rings, loops and curled morphology, that can be attributed to electrically driven bending instability and/or a mechanical buckling effect [46, 47]. Such a unique morphology of ESP-deposited CNTNs results in enhanced electron scattering processes than in the other methods and renders more diffusive transport. The rings, which are mostly made of CNT bundles (see Fig. S-9 (in the ESM)) are bridging straight and curled CNTs, therefore introducing more Schottky barriers in the path of the current flow. When rings are contacted by many CNTs their electrostatic potential may not be uniform which then introduces a certain degree of disorder in the scattering potential. Moreover, due to curled morphologies, ESP deposition produces a slightly higher density of CNTs which are in contact with the substrate. This enhances coupling with surface polar phonons from the SiO_2 substrate degrading the mobility by an order of magnitude [48]. These overall effects can explain the lower mobilities (not exceeding ~13 cm^2/(V·s)) of ESP-deposited CNTNs than that of the other three deposition methods. The peculiar orientation of the ESP-deposited CNTs also causes higher device-to-device variation, evidenced by the wide distribution of I_{ON}/I_{OFF} ratio in Fig. 2(c) (~20–5 × 10^5). The higher I_{ON}/I_{OFF} ratio for some (but not all) of the ESP-deposited networks could be due to curvature-induced strain which is known to open small band gaps in metallic single-walled CNTs [49–51].

Both PTF and DF techniques employ a membrane filter for the deposition of CNTNs, which are then transferred to the receiving substrates. CNTNs deposited by the PTF method preserve the morphology of as-deposited random films formed by flow filtration directly after gas-phase synthesis. CNTNs deposited by the DF method exhibit a unique morphology due to curvature induced by liquid droplet meniscus

evaporation. This leads to an increased tube-to-tube contact area [52, 53]. Both PTF and DF methods show no preferential alignment and an increased amount of CNT bundling, as measured by the larger average CNT diameter (see Table 1 and the ESM). However, the lack of curvature in the CNT links between junctions as compared to ESP results in increased network conductivity. The morphology of DF-deposited CNTs is especially interesting due to the increased number of Y-type tube-to-tube junctions rather than X-type [3]. Y-type junctions have a larger junction area which results in a lower inter-nanotube resistance, in accordance to previous experimental studies [3, 37].

Lastly, we return to the $1/f$ characteristic of the devices from Fig. 2(d) and Fig. S-5 (in the ESM). Higher values of A and R for ESP devices imply that connectivity between nanotube bundles in these devices might not be as efficient as in the other networks. The relatively high percentages of junctions compared to the nanotube coverage (as reported in Table 1) also confirm this hypothesis. On the other hand, DF networks seem to have fewer resistive junctions and therefore lower A and R values. The similar values of A/R across all of the networks observed confirm that individual tube and bundle properties in CNTNs prepared with different methods are not affected significantly (Fig. S-5 (in the ESM)).

When assembling as-synthesized single-walled CNTs into a random network configuration, the ability to accurately control the density and arrangement of nanotubes within the network is an important feature for effective CNTN deposition, especially when used for CNT TFT applications [12, 16, 17]. The CNTN deposition time for each method used in this study can be further optimized to achieve the highest CNT TFT performance with larger μ_{FE} and I_{ON}/I_{OFF} ratio concurrently, accounting for morphology effects on network performance. For instance, TFTs based on TP-deposited CNTNs with optimized network densities demonstrated high performance of both metrics simultaneously (e.g. I_{ON}/I_{OFF} ratio of 3×10^6 and a mobility $\mu_{FE} \approx 20$ cm^2/(V·s)) (see Fig. 2(c) and Fig. S-10 in the ESM). The results reported in this study are significant for the practical application of CNTNs with different morphologies fabricated by dry processes directly after synthesis. These methods are garnering interest due to high resulting device performance, efficiency, scalability, and low fabrication costs, all of which are important for large scale flexible macroelectronics.

4. Conclusions

In this work we explored the effect of CNTN morphology on the electrical characteristics of CNT TFTs. We fabricated CNT TFTs with consistent structural properties of as-grown CNTs themselves and various CNT arrangements within the network. CNTN morphologies were reproducibly altered by using four different CNTN deposition methods, applied directly after the single-walled CNT synthesis in the vertical aerosol (floating catalyst) CVD reactor. We found that there is a close relationship between the morphology of CNTNs and the electrical performance of TFTs based on these networks. We also demonstrated a novel technique for the CNTN deposition based on thermophoresis (TP), making it possible to prepare high-performance nanotube networks with higher I_{ON}/I_{OFF} and μ_{FE}, concurrently. Our results emphasize the important role of CNTN morphology on the realization of high-performance, CNTN-based macroelectronic devices.

5. Methods

5.1 CNT synthesis

The single-walled CNTs used in this study were synthesized by an atmospheric-pressure floating-catalyst (aerosol) CVD technique. The growth process is based on thermal decomposition of ferrocene vapor ($Fe(C_5H_5)_2$, 99%, Strem Chemicals) in a carbon monoxide (CO) atmosphere at an elevated temperature (reactor temperature at 880 °C), as described in detail elsewhere [21]. Ferrocene is vaporized at room temperature by passing CO (with a flow rate of 300 cm^3/min) through a cartridge filled with ferrocene powder. The flow containing ferrocene vapor (0.7 Pa) is then introduced into the high temperature zone of the ceramic tube reactor (internal diameter of 22 mm) through a water-cooling probe and mixed with an additional CO flow (100 cm^3/min). The outlet of the

water-cooling probe is located at the wall temperature of around 700 °C, which is needed for fast heating of the vapor–gas mixture and production of catalyst particles. Single-walled CNTs, grown from the surface of catalyst particles suspended in gas, are carried downstream of the reactor by CO flow where they are instantaneously collected onto a substrate at room temperature.

5.2 CNT TFT fabrication and measurement

CNT TFTs were fabricated on SiO_2 (100 nm)/Si substrates where the highly boron-doped Si (resistivity 0.01–0.05 Ω·cm) also serves as a back-gate. An Al layer (200 nm) was sputtered on the back-side of the wafer to insure a better contact for the bottom-gate electrode. We used ESP, TP, PTF, and DF deposition techniques to collect CNTNs onto device substrates. Source and drain electrodes (Ti/Au, 3/45 nm) were patterned by standard photolithography, electron-beam evaporation (e-beam evaporator IM9912) and lift-off processes (AZ 5214 Photoresist). Photolithography and oxygen plasma etching (Oxford 80+ reactive ion etcher) were used to define the CNTNs channels. Electrical characterization was carried out using an HP 4155A semiconductor parameter analyzer (DC characterization) and a Keithley 2612A dual source-measurement unit (pulsed characterization) [27, 28]. 1/*f* characterization was carried out using a Keithley 2612 dual source meter, a SRS 570 low-noise current amplifier, and an HP 35665A Dynamic Signal Analyzer.

5.3 CNTN density

To characterize the CNTN density we analyzed the device area fill factor (γ_C) as previously described [43]. In brief, we used image analysis software [41] to measure the area of the CNTN in SEM images through intensity thresholding, and used the projected area of the highlighted CNTN, A_C, to calculate γ_C. From γ_C, we calculated the CNTN length, L_C, by choosing an average CNT diameter measured under SEM, $\langle d_{SEM} \rangle \approx$ 50 nm. We note this provides a significant overestimate of the true areal coverage γ_C' as CNT bundle diameters appear much larger under SEM. However, after calculating L_C we obtain γ_C' by using the real CNT bundle diameter (d) averaged from AFM analysis.

5.4 Image processing

Using Adobe Photoshop CS3, we adjusted the grayscale pixel histograms from the SEM images taken of each CNTN deposition method. In this process, we set the background pixels to black and the CNT-related pixels to white, improving contrast. We note that this process is qualitative, since the contrast within the SEM images changes due to exposure, beam energies, and other factors. However, we have provided the original images in the figures and the ESM for clarity. These modified images are saved in RGB format and converted to grayscale within MATLAB.

5.5 Junction area

After the images were contrast-enhanced, we filtered them with a two-dimensional finite impulse response (FIR) filter that averages adjacent pixels. This filter suppresses sharp edges that are pixilation artifacts (i.e. edges at 45°, 90°, and 135°) while passing all other edges. In the process, the number of pixels assigned to a CNT increased negligibly. Our filter selects CNT junctions, as they are the cumulative sum of many neighboring pixels. We consider pixels with RGB values greater than 200 (out of 255) to be CNT junctions. The junction area percentage is the number of junction pixels divided by the number of CNT pixels. We assign the CNT pixel number as the overall mean of pixels within the image that are greater than the background, which has a pixel value less than 3.

5.6 Alignment distribution extraction

From the contrast-enhanced image, we find the boundaries of the CNTN using a Moore–Neighbor tracing algorithm modified by Jacob's stopping criteria [54]. This boundary tracing is only effective when the CNTs have high contrast with their background, namely, when the CNTs are white (255 value) and the background is black (0 value). After tracing the outer boundary of the image (highlighted in red), we iterate through the inner boundaries of the CNTN until the entire network is traversed. Many CNTs within the CNTN share the same number of pixels for a small distance (5–10 pixels). Using these equivalent values for every pixel construes the alignment angle distribution to be peaked at {0°, 45°, 90°, 135°, 180°} and is not

physical. Thus, we only sample every 25th pixel and take angles for distances between (i, j) and (i + 25, j + 25). The alignment angle is defined by $\theta = \tan{-1}(\Delta y/\Delta x)$, where Δy and Δx are the distances between these adjacent 25th pixels. When $\theta < 0$, we renormalize it to the range (0, 180°) by the transformation $\theta' = \theta + \pi$.

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Electronic Supplementary Material: Supplementary material (additional results related to CNTN morphology analysis, i.e. SEM images of dry-transferred CNTN on polymer and quartz substrates (Fig. S-1), optical absorption spectra and TEM images of aerosol-synthesized single-walled CNTs and CNT bundles (Fig. S-2), current–voltage (I_D–V_{GS}) transfer characteristics of a representative CNT TFT deposited via four different methods and measured using pulsed sweep method (Fig. S-3), temperature dependent variation of TFT mobility based on CNTNs deposited by four different methods (Fig. S-4), 1/f noise amplitude distribution in various networks (Fig. S-5), image analysis of CNTN morphology after electrostatic precipitation, press transfer from the filter and dissolving the filter depositions (Figs. S-6–S-8), AFM images of ESP-deposited CNTNs (Fig. S-9), transfer characteristics of TFT based on TP-deposited CNTN with optimized density (Fig. S-10)) is available in the online version of this article at http://dx.doi.org/10.1007/s12274-012-0211-8.

References

[1] Snow, E.; Novak, J.; Campbell, P. M.; Park, D. Random networks of carbon nanotubes as an electronic material. *Appl. Phys. Lett.* **2003**, *82*, 2145–2147.

[2] Cao, Q.; Kim, H. S.; Pimparkar, N.; Kulkarni, J. P.; Wang, C.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **2008**, *454*, 495–500.

[3] Sun, D. M.; Timmermans, M. Y.; Tian, Y.; Nasibulin, A. G.; Kauppinen, E. I.; Kishimoto, S.; Mizutani, T.; Ohno, Y. Flexible high-performance carbon nanotube integrated circuits. *Nat. Nanotechnol.* **2011**, *6*, 156–161.

[4] Kumar, M.; Ando, Y. Chemical vapor deposition of carbon nanotubes: A review on growth mechanism and mass production. *J. Nanosci. Nanotechnol.* **2010**, *10*, 3739–3758.

[5] Wei, B. Q.; Vajtai, R.; Jung, Y.; Ward, J.; Zhang, R.; Ramanath, G.; Ajayan P. M. Organized assembly of carbon nanotubes. *Nature* **2002**, *416*, 495–496.

[6] Artukovic, E.; Kaempgen, M.; Hecht, D. S.; Roth, S.; Grüner, G. Transparent and flexible carbon nanotube transistors. *Nano Lett.* **2005**, 5, 757–760.

[7] Engel, M.; Small, J. P.; Steiner, M.; Freitag, M.; Green, A. A.; Hersam, M. C.; Avouris, P. Thin film nanotube transistors based on self-assembled, aligned, semiconducting carbon nanotube arrays. *ACS Nano* **2008**, *2*, 2445–2452.

[8] Wang, C.; Zhang, J.; Ryu, K.; Badmaev, A.; De Arco, L. G.; Zhou, C. Wafer-scale fabrication of separated carbon nanotube thin-film transistors for display applications. *Nano Lett.* **2009**, *9*, 4285–4291.

[9] Ha, M.; Xia, Y.; Green, A. A.; Zhang, W.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. Printed, sub-3V digital circuits on plastic from aqueous carbon nanotube inks. *ACS Nano* **2010**, *4*, 4388–4395.

[10] Lee, S. Y.; Lee, S. W.; Kim, S. M.; Yu, W. J.; Jo, Y. W.; Lee, Y. H. Scalable complementary logic gates with chemically doped semiconducting carbon nanotube transistors. *ACS Nano* **2011**, *5*, 2369–2375.

[11] Miyata, Y.; Shiozawa, K.; Asada, Y.; Ohno, Y.; Kitaura, R.; Mizutani, T.; Shinohara, H. Length-sorted semiconducting

carbon nanotubes for high-mobility thin film transistors. *Nano Res.* **2011**, *4*, 963–970.

[12] Rouhi, N.; Jain, D.; Burke, P. J. High-performance semiconducting nanotube inks: Progress and prospects. *ACS Nano* **2011**, *5*, 8471–8487.

[13] Zavodchikova, M. Y.; Kulmala, T.; Nasibulin, A. G.; Ermolov, V.; Franssila, S.; Grigoras, K.; Kauppinen, E. I. Carbon nanotube thin film transistors based on aerosol methods. *Nanotechnology* **2009**, *20*, 085201.

[14] Kaskela, A.; Nasibulin, A. G.; Timmermans, M. Y.; Aitchison, B.; Papadimitratos, A.; Tian, Y.; Zhu, Z.; Jiang, H.; Brown, D. P.; Zakhidov, A., et al. Aerosol-synthesized SWCNT networks with tunable conductivity and transparency by a dry transfer technique. *Nano Lett.* **2010**, *10*, 4349–4355.

[15] Nasibulin, A. G.; Kaskela, A.; Mustonen, K.; Anisimov, A. S.; Ruiz, V.; Kivistö, S.; Rackauskas, S.; Timmermans, M. Y.; Pudas, M.; Aitchison, B., et al. Multifunctional free-standing single-walled carbon nanotube films. *ACS Nano* **2011**, *5*, 3214–3221.

[16] Rouhi, N.; Jain, D.; Zand, K.; Burke, P. J. Fundamental limits on the mobility of nanotube based semiconducting inks. *Adv. Mater.* **2010**, *23*, 94–99.

[17] Sangwan, V. K.; Behnam, A.; Ballarotto, V. W.; Fuhrer, M. S.; Ural, A.; Williams, E. D. Optimizing transistor performance of percolating carbon nanotube networks. *Appl. Phys. Lett.* **2010**, *97*, 043111.

[18] LeMieux, M. C.; Sok, S.; Roberts, M. E.; Opatkiewicz, J. P.; Liu, D.; Barman, S. N.; Patil, N.; Mitra, S.; Bao, Z. Solution assembly of organized carbon nanotube networks for thin-film transistors. *ACS Nano* **2009**, *3*, 4089–4097.

[19] Kocabas, C.; Pimparkar, N.; Yesilyurt, O.; Kang, S.; Alam, M. A.; Rogers, J. Experimental and theoretical studies of transport through large scale, partially aligned arrays of single-walled carbon nanotubes in thin film type transistors. *Nano Lett.* **2007**, *7*, 1195–1202.

[20] Pimparkar, N.; Kocabas, C.; Kang, S. J.; Rogers, J.; Alam, M. A. Limits of performance gain of aligned CNT over randomized network: theoretical predictions and experimental validation. *IEEE Electr. Device Lett*. **2007**, *28*, 593–595.

[21] Moisala, A.; Nasibulin, A. G.; Brown, D. P.; Jiang, H.; Khriachtchev, L.; Kauppinen, E. I. Single-walled carbon nanotube synthesis using ferrocene and iron pentacarbonyl in a laminar flow reactor. *Chem. Eng. Sci.* **2006**, *61*, 4393–4402.

[22] Zavodchikova, M. Y.; Nasibulin, A. G.; Kulmala, T.; Grigoras, K.; Anisimov, A. S.; Franssila, S.; Ermolov, V.; Kauppinen, E. I. Novel carbon nanotube network deposition technique for electronic device fabrication. *Phys. Status Solidi B* **2008**, *245*, 2272–2275.

[23] Gonzalez, D.; Nasibulin, A. G.; Baklanov, A. M.; Shandakov, S. D.; Brown, D. P.; Queipo, P.; Kauppinen, E. I. A new thermophoretic precipitator for collection of nanometer-sized aerosol particles. *Aerosol Sci. Technol.* **2005**, *39*, 1064–1071.

[24] Hinds, W. C. *Aerosol Technology: Properties, Behavior, and Measurement of Airborne Particles;* Wiley-Interscience: New York, 1982.

[25] Bao, Z. Materials and fabrication needs for low-cost organic transistor circuits. *Adv. Mater.* **2000**, *12*, 227–230.

[26] Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. Hysteresis caused by water molecules in carbon nanotube field-effect transistors. *Nano Lett.* **2003**, *3*, 193–198.

[27] Estrada, D.; Dutta, S.; Liao, A.; Pop, E. Reduction of hysteresis for carbon nanotube mobility measurements using pulsed characterization. *Nanotechnology* **2010**, *21*, 085702.

[28] Liu, Z.; Qiu, Z. J.; Zhang, Z. B.; Zheng, L. R.; Zhang, S. L. Mobility extraction for nanotube TFTs. *IEEE Electr. Device Lett.* **2011**, *32*, 913–915.

[29] Cao, Q.; Xia, M. G.; Kocabas, C.; Shim, M.; Rogers, J. A.; Rotkin, S. V. Gate capacitance coupling of singled-walled carbon nanotube thin-film transistors. *Appl. Phys. Lett.* **2007**, *90*, 023516.

[30] Wang, C.; Chien, J. -C.; Takei, K.; Takahashi, T.; Nah, J.; Niknejad, A. M.; Javey, A. Extremely bendable, high-performance integrated circuits using semiconducting carbon nanotube networks for digital, analog, and radio-frequency applications. *Nano Lett.* **2012**, *12*, 1527–1533.

[31] Hooge, F. N. 1/*f* noise is no surface effect. *Phys. Lett. A* **1969**, *29*, 139–140.

[32] Snow, E. S.; Novak, J. P.; Lay, M. D.; Perkins, F. K. 1/*f* noise in single-walled carbon nanotube devices. *Appl. Phys. Lett.* **2004**, *85*, 4172–4174.

[33] Soliveres, S.; Gyani, J.; Delseny, C.; Hoffmann, A.; Pascal, F. 1/*f* noise and percolation in carbon nanotube random networks. *Appl. Phys. Lett.* **2007**, *90*, 082107.

[34] Stadermann, M.; Papadakis, S. J.; Palvo, M. R.; Novak, J.; Snow, E.; Fu, Q.; Liu, J.; Fridman, Y.; Boland, J. J.; Superfine, R., et al. Nanoscale study of conduction through carbon nanotube networks. *Phys. Rev. B* **2004**, *69*, 201402(R).

[35] Kodama, Y.; Sato, R.; Inami, N.; Shikoh, E.; Yamamoto, Y.; Hori, H.; Kataura, H.; Fujiwara, A. Field-effect modulation of contact resistance between carbon nanotubes. *Appl. Phys. Lett.* **2007**, *91*, 133515.

[36] Blackburn, J. L.; M. Barnes, T. M.; Beard, M. C.; Kim, Y. H.; Tenent, R. C.; McDonald, T. J.; To, B.; Coutts, T. J.; Heben, M. J. Transparent conductive single-walled carbon nanotube networks with precisely tunable ratios of semiconducting and metallic nanotubes. *ACS Nano* **2008**, *2*, 1266–1274.

[37] Nirmalraj, P. N.; Lyons, P. E.; De, S.; Coleman, J. N.; Boland, J. J. Electrical connectivity in single-walled carbon nanotube networks. *Nano Lett.* **2009**, *9*, 3890–3895.

[38] Lee, E. J. H.; Balasubramanian, K.; Burghard, M.; Kern, K. Spatially resolved potential distribution in carbon nanotube cross junction devices. *Adv. Mater.* **2009**, *21*, 2720–2724.

[39] Hecht, D.; Hu, L.; Grüner, G. Conductivity scaling with bundle length and diameter in single walled carbon nanotube networks. *Appl. Phys. Lett.* **2006**, *89*, 133112.

[40] Anisimov, A. S.; Nasibulin, A. G.; Jiang, H.; Launois, P.; Cambedouzou, J.; Shandakov, S. D.; Kauppinen, E. I. Mechanistic investigations of single-walled carbon nanotube synthesis by ferrocene vapor decomposition in carbon monoxide. *Carbon* **2010**, *48*, 380–388.

[41] Necas, D.; Klapetek, P.; Anderson, C. *Gwyddion 2.20*; Brno: Czech Republic, 2009.

[42] MATLAB, 7.8.0347 (R2009a), MathWorks, Inc.: Natick, MA, 2009.

[43] Estrada, D.; Pop, E. Imaging dissipation and hot spots in carbon nanotube network transistors. *Appl. Phys. Lett.* **2011**, *98*, 073102.

[44] Alam, M. A.; Pimparkar, N.; Kumar, S.; Murthy, J. Theory of nanocomposite network transistors for macroelectronics applications. *MRS Bull.* **2006**, *31*, 466–470.

[45] Fuhrer, M. S.; Nygård, J.; Shih, L.; Forero, M.; Yoon, Y. -G.; Mazzoni, M. S. C.; Choi, H. J.; Ihm, J.; Louie, S. G.; Zettl, A., et al. Crossed nanotube junctions. *Science* **2000**, *288*, 494–497.

[46] Han, T.; Reneker, D. H.; Yarin, A. L. Buckling of jets in electrospinning. *Polymer* **2007**, *48*, 6064–6076.

[47] Reneker, D. H.; Yarin, A. L. Electrospinning jets and polymer nanofibers. *Polymer* **2008**, *49*, 2387–2425.

[48] Perebeinos, V.; Rotkin, S. V.; Petrov, A. G.; Avouris, P. The effects of substrate phonon mode scattering on transport in carbon nanotubes. *Nano Lett.* **2008**, *9*, 312–316.

[49] Ding, J. W.; Yan, X. H.; Cao, J. X.; Wang, D. L.; Tang, Y.; Yang, Q. B. Curvature and strain effects on electronic properties of single-wall carbon nanotubes. *J. Phys.: Condens. Matter* **2003**, *15*, L439.

[50] Yoon, Y.; Guo, J. Analysis of strain effects in ballistic carbon nanotube FETs. *IEEE Trans. Electron Dev.* **2007**, *54*, 1280–1287.

[51] Wahab, M. A.; Khosru, Q. D. M. Strain effects on the performance of zero-Schottky-barrier double-walled carbon nanotube transistors. *J. Appl. Phys.* **2010**, *108*, 034301.

[52] Li, Q.; Zhu, Y. T.; Kinloch, I. A.; Windle, A. H. Self-organization of carbon nanotubes in evaporating droplets. *J. Phys. Chem. B* **2006**, *110*, 13926–13930.

[53] Zeng, H.; Kristiansen, K.; Wang, P.; Bergli, J.; Israelachvili, J. Surface-induced patterns from evaporating droplets of aqueous carbon nanotube dispersions. *Langmuir* **2011**, *27*, 7163–7167.

[54] Gonzalez, R. C.; Woods, R. E.; Eddins, S. L. *Digital Image Processing using MATLAB;* Pearson Education: India, 2004.

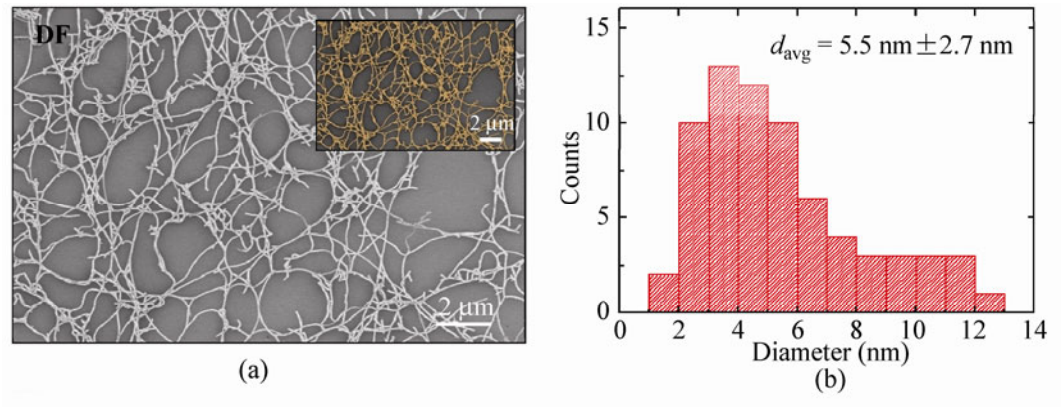

Figure S-8 Image analysis of CNTN morphology after dissolving the filter (DF) deposition. (a) SEM image of a DF-deposited channel. Inset: intensity thresholding performed with image analysis software highlighting the CNTN. (b) Diameter distribution of 70 randomly selected CNTs in a DF-deposited CNT TFT. (c) Junction analysis of DF-deposited CNTN. (d) Angle distribution of several DF-deposited CNTNs analyzed using image analysis software

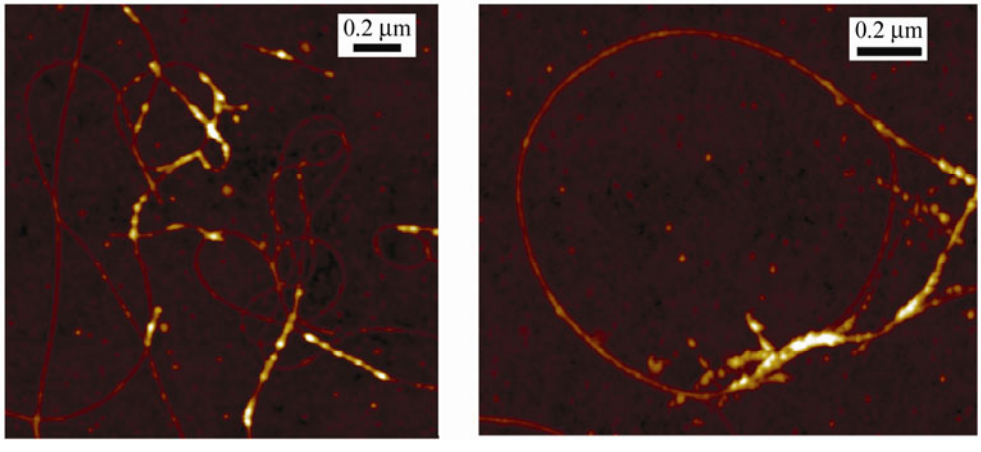

Figure S-9 AFM images of ESP-deposited CNTN

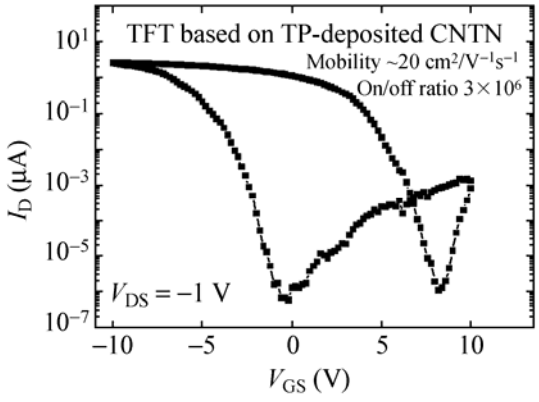

Figure S-10 Current–voltage (I_D–V_{GS}) transfer characteristics of a TFT based on CNTN deposited via thermal precipitation (TP) with optimized network deposition time (i.e. 5 s). The mobility of this network μ_{FE} is ~20 $cm^2/(V{\cdot}s)$ and the I_{ON}/I_{OFF} ratio ~3×10^6