Investigating bias temperature instability and threshold voltage shifts in indium tin oxide (ITO) transistors

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ABSTRACT

Ultrathin amorphous oxide semiconductors are emerging materials being considered for transistors in memory and various back-end-of-line applications, but their stability remains a concern. Here, we report on both positive and negative bias temperature stability of top-gated indium tin oxide (ITO) transistors whose ultrathin, ~4 nm, channel was deposited with three oxygen compositions (10%, 14%, and 18% O_2 partial pressure). No correlation between mobility and stability of such ITO transistors is apparent at room temperature, as we achieve highly stable (~10 mV threshold voltage shift) devices with good mobility (~38 $cm^2\ V^{-1}\ s^{-1}$). We also investigate the time-dependent stability of such ITO transistors at elevated temperatures (85 and 120 °C). We discuss the interplay of multiple physical mechanisms and uncover the effect of processing conditions, leading to oxygen-related defects in the channel and gate dielectric, causing the subsequent instability.

Relatively low-temperature fabrication (e.g., below 400 °C) of field-effect transistors (FETs) based on amorphous oxide semiconductors is promising for heterogeneous three-dimensional (3D) integration of electronics, enabling greater memory and logic capacity.[1] Indium-based metal oxide transistors can demonstrate good electron mobility even in an amorphous material, due to the overlap of large indium 5s orbitals creating effective electron conduction paths.[2] Recently, In_2O_3 transistors[3] have shown ~3 mA/μm drive currents but with low on/off current ratio $<10^2$, whereas indium gallium zinc oxide (IGZO) transistors[4] have reported high ($\sim10^{12}$) on/off current ratio, but with lower drive current. Among this class of materials, ultrathin (≤4 nm) indium tin oxide (ITO) transistors have shown good performance, with both high on-state and low off-state currents.[1,5–7] However, oxygen vacancy defects in such oxide semiconductor channels act as electron donors, leading to threshold voltage (V_T) instability.[8–11]

Increasing metal dopant concentrations in the channel can improve stability by suppressing the oxygen vacancies. As a result, metal dopants with high oxygen bond dissociation energy (e.g., Ga, Zn, Sn, W, and Si)[12–15] are introduced to the oxide composition to form ternary or quaternary channels but often at the cost of lower mobility. Post-deposition treatments, such as oxygen annealing[11,16,17] and fluorine anion incorporation,[18] have also been investigated to improve stability.

A better understanding of the stability degradation mechanism in oxide semiconductor transistors is essential to ensure reliable device performance at elevated circuit operating temperatures. Although many studies have examined bias temperature instability in oxide FETs, most focus on relatively thick or un-passivated channels and report the conventional positive V_T shifts under positive bias stress.[19,20] Some works have observed anomalous V_T shift at high temperature[11] and attributed them to hydrogen-related defect migration from the gate dielectric to the channel,[13,15,21,22] to the formation of peroxide states based on oxygen interstitials,[23] to charge trapping at the gate metal–dielectric interface, or to dipoles induced by charge migration in the gate dielectric.[24] However, these

studies typically emphasize positive bias stress or report opposite shift directions under positive and negative stress.[13,15,25] The wide range of reported behaviors indicates that device structure, gate dielectric process, channel composition, and fabrication sequence strongly influence V_T stability and can even reverse the shift direction. Without a systematic study that spans both positive and negative bias stress, multiple temperatures, and controlled oxygen composition within the same material system, these effects cannot be fully understood.

In this work, we provide a comprehensive investigation of the V_T shifts in indium tin oxide (ITO) transistors by studying both positive and negative bias stress stability at room temperature and high temperatures (85 and 120 °C), comparing the stress and relaxation of top-gated (TG) devices with different oxygen compositions in the channel. We explore the effects of oxygen vacancy and oxygen interstitial defects of the gate dielectric and channel oxides on bias temperature instability, for different channel oxygen contents.

Figure 1 shows the schematic of a top-gated (TG) transistor, a top-view optical image of a fabricated device, and the fabrication process flow. We vary O_2 partial pressure (10%, 14%, and 18%) during ITO sputtering[9] to study the influence of oxygen content in the channel. Figure 2(a) shows the effect of oxygen incorporation into the ITO channel, noting expectedly more positive V_T, extracted by both linear extrapolation and at constant current of $(W/L) \times 10$ nA, with higher O_2 flow during sputtering. This occurs because oxygen vacancies in amorphous oxide channel transistors act as electron donors, and additional oxygen can passivate these vacancies causing more positive V_T values. Figure 2(b) shows the decrease in field-effect mobility (μ_{FE}), extracted at maximum transconductance, with more oxygen incorporation. This decreasing trend is attributed to the dominance of hopping-based transport over band transport, as the Fermi energy in the channel is lowered with fewer electrons.[26] For the 18% O_2 ITO channel, V_T is positive, but the field-effect mobility, μ_{FE}, is very low (~0.1 $cm^2\ V^{-1}\ s^{-1}$), due to excess vacancy passivation and creation of oxygen interstitial defects. Despite the lower mobility, we study these devices to understand the effect of channel "doping" and mobility on the bias temperature stability of ITO transistors. The representative I_D vs V_{GS} characteristics and transconductance, g_m vs V_{GS} curves for all three O_2 sputtering conditions are shown in Figs. 2(c) and 2(d), respectively.

First, we perform positive and negative gate bias stress (PBS and NBS) measurements on our top-gated ITO transistors at room temperature. Figures 3(a), 3(c), and 3(e) show the I_D vs V_{GS} characteristics of our devices with ITO channel formed using 10%, 14%, and 18% O_2 partial pressure, respectively, under PBS ($V_{GS,stress}$ = 2 V). The same plots for NBS ($V_{GS,stress}$ = −2 V) are shown in

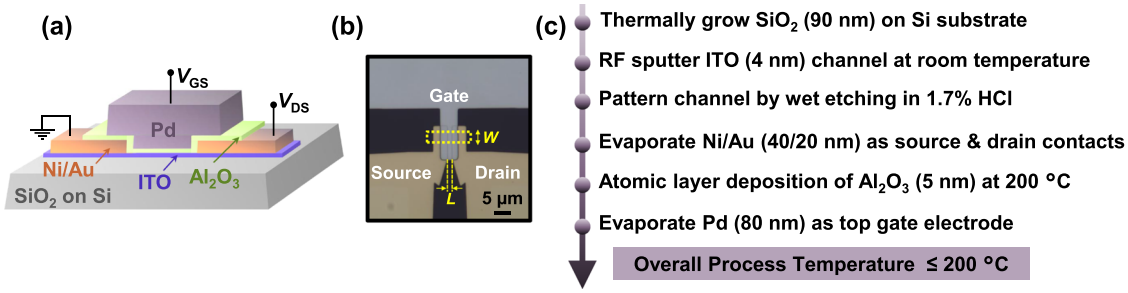


FIG. 1. (a) Schematic of a top-gated (TG) ITO transistor. (b) Top-view optical image of a completed TG device, fabricated in this study. Here, W and L denote the channel width and length, respectively. The ITO channel thickness is ~4 nm here, with $W \approx 5$ μm and $L \approx 2$ μm. (c) Detailed fabrication process flow for our devices. Ozone-based atomic layer deposition is used for Al_2O_3 deposition. Optical lithography is used for all patterning.

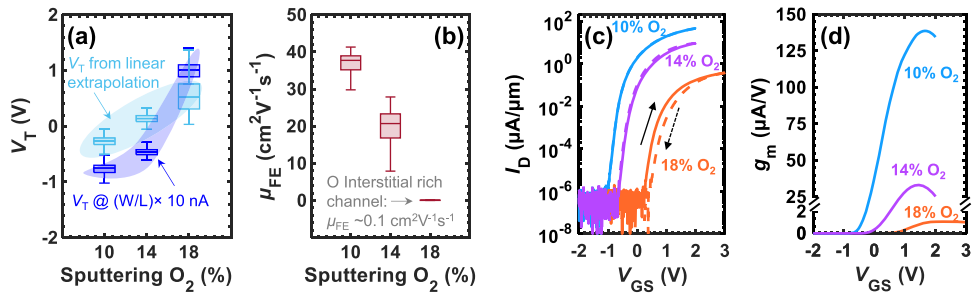


FIG. 2. Observed (a) threshold voltage (V_T) and (b) field-effect mobility (μ_{FE}) as a function of varying O_2 flow during ITO sputtering. Data are from ≥20 devices in each case, extracted from ~2 μm long top-gated ITO transistors. The error bars in (a) and (b) illustrate the spread of data in the box plots. Representative (c) I_D vs V_{GS} characteristics and (d) transconductance, g_m vs V_{GS} curves for 10%, 14%, and 18% O_2 ITO channel transistors. The solid and dashed curves in (c) mark sweep directions, as indicated by small arrows. The transconductance in (d) is shown for the forward gate voltage sweep. Note that the 18% O_2 channel has much lower transconductance and is shown zoomed-in, on the lower portion of the vertical axes (0–2 μA/V) in panel (d). Here, channel width, W and length, L are 5 μm and 2 μm, respectively, for all devices, measured at V_{DS} = 1 V.

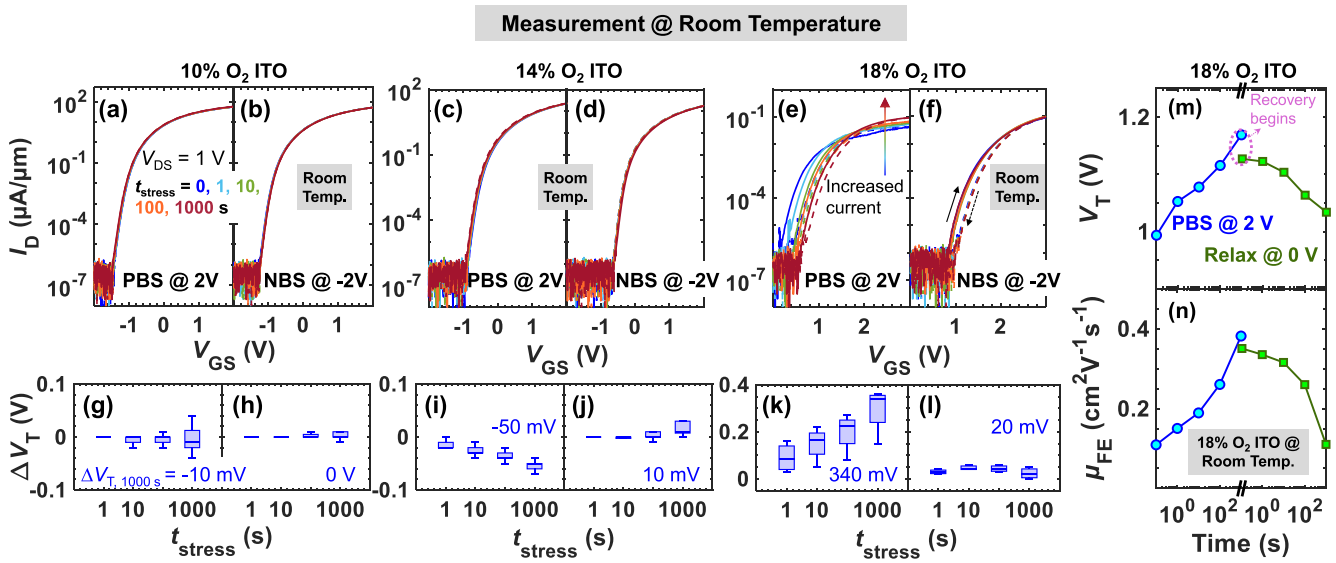


FIG. 3. Measured I_D vs V_{GS} of our top-gated ITO transistors under (a), (c), and (e) positive and (b), (d), and (f) negative bias stress, **measured at room temperature**. Devices with [(a) and (b)] 10%, [(c) and (d)] 14%, and [(e) and (f)] 18% O_2 flow during ITO sputtering. The solid and dashed curves mark sweep directions, as indicated. [(g)–(l)] Evolution of stress-induced V_T shift, ΔV_T with stress time, t_{stress}, corresponding to the panels (a)–(f), with *median* ΔV_T after 1000 s stress denoted in each panel. ΔV_T is the difference between unstressed V_{T0} and stressed V_T after 1000 s stress: $\Delta V_T = V_{T,\,1000\,s} - V_{T0}$. Here, V_T is extracted at constant current = (W/L) × 10 nA. In all panels, each box-and-whisker group represents data from 10 to 20 devices. The error bars in (g)–(l) illustrate the spread of data in the box plots. All devices are ~2 μm long. Evolution of (m) threshold voltage (V_T) and (n) field-effect mobility (μ_{FE}) with time under stress (curves with blue circles) and relaxation (curves with green squares) at $V_{GS,stress}$ = +2 and 0 V, respectively, for an **18% O_2 ITO** device measured at **room temperature**, showing recoverable stress-induced shift in V_T and μ_{FE}.

Figs. 3(b), 3(d), and 3(f). The corresponding trends of ΔV_T (i.e., change in V_T) vs stress time (t_{stress}) are plotted in Figs. 3(g)–3(l).

We observe median ΔV_T = −10, −50, and +340 mV for 10%, 14%, and 18% O_2 ITO transistors, respectively, under PBS at room temperature. Typically, a positive V_T shift is expected upon PBS, due to electron trapping in the gate dielectric or channel/dielectric interface.[27] However, here, we observe a slightly negative ΔV_T for 10% and 14% O_2 ITO. Because the top gate dielectric oxide is likely to be more oxygen-deficient due to the channel and dielectric deposition sequence, this abnormal shift could be attributed to the top dielectric scavenging weakly bonded oxygen from the channel. Such oxygen scavenging creates oxygen vacancies in the channel, donating free electrons in the process. Our prior work using different top dielectric materials highlighted the critical role of the dielectric/channel interface, particularly its oxygen content, in determining V_T stability.[16] Through x-ray photoelectron spectroscopy (XPS) depth profiling, we further showed that post-fabrication oxygen annealing reduces oxygen deficiency in the top gate dielectric oxide, suppresses oxygen scavenging from the channel, and thereby improves V_T stability.[16]

Such negative ΔV_T could also be explained by hydrogen migration into the channel from the top gate dielectric,[13,15,28] as they have similar effects of releasing electrons in the channel and causing a negative ΔV_T. Notably, purely bottom-gated FETs show a positive ΔV_T under PBS at room temperature,[8–10] which suggests different oxygen and/or hydrogen contents in bottom vs top dielectrics due to processing. The difference in $|\Delta V_T|$ between the 10% and 14% O_2 ITO channels indicates a key role of the channel/dielectric interface, compared to the gate/dielectric interface.

The 18% O_2 ITO channel with the same top dielectric should also demonstrate similar negative ΔV_T under PBS, but multiple mechanisms can co-exist and likely counteract each other.[28] As such, the stability of such an oxygen-rich (18%) channel is dominated by the positive V_T shift due to electron trapping in the channel oxygen interstitials (forming peroxide states, i.e., acceptor-like traps).[29,30] All samples show negligible $|\Delta V_T| \leq 20$ mV under NBS. Notably, the 10% O_2 ITO devices are highly stable with good mobility (~38 $cm^2\ V^{-1}\ s^{-1}$), thus exhibiting no correlation between mobility and stability at room temperature.[2] The 18% O_2 ITO transistor shows increasing drive current despite positive ΔV_T [Fig. 3(e)], suggesting the passivation of channel oxygen interstitial defects by electron trapping, which increases mobility and current,[17] as shown in Fig. 3(n). Channel oxygen interstitials are shallow acceptor-like defects, as both V_T and μ_{FE} fully recover after the relaxation cycle [Figs. 3(m) and 3(n)].

Second, the temperature stability is investigated by measuring top-gated 10% O_2 ITO transistors at 85 and 120 °C in N_2 ambient, which reveals negative ΔV_T = −120 mV (between 25 and 120 °C) without gate bias stress (Fig. 4). This negative shift in V_T [Fig. 4(b)] is attributed to the thermal ionization of oxygen vacancies and is recoverable upon cooling.[11] Such thermally activated carrier transport also leads to an increasing trend in mobility,[26] as shown in Fig. 4(c).

Figure 5 shows positive and negative bias stress measurements at 120 °C, with I_D vs V_{GS} curves in Figs. 5(a)–5(f) and corresponding

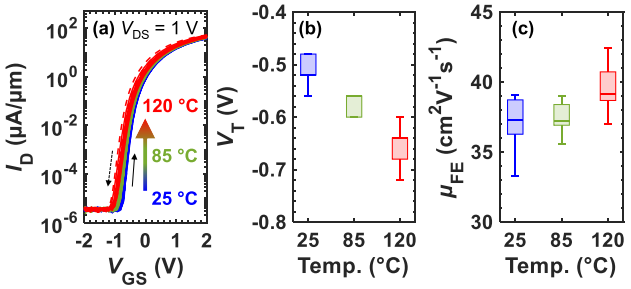


FIG. 4. (a) Measured I_D vs V_{GS} of top-gated 10% O_2 ITO transistors at different temperatures (25, 85, and 120 °C). The solid and dashed curves mark sweep directions, as indicated. Observed (b) threshold voltage (V_T) and (c) field-effect mobility (μ_{FE}) of 10 devices as a function of measurement temperature. The error bars in (b) and (c) illustrate the spread of data in the box plots. Here, V_T is extracted at constant current = (W/L) × 10 nA, and μ_{FE} is extracted at maximum transconductance.

ΔV_T evolution in Figs. 5(g)–5(l). At such elevated temperature, 10% and 14% O_2 ITO transistors show $\Delta V_T < 0$, regardless of the gate stress voltage polarity. The pronounced negative ΔV_T under PBS at higher temperature could be due to enhanced oxygen scavenging or thermal ionization of oxygen vacancies releasing electrons.[11] The 18% O_2 ITO transistors show positive ΔV_T under PBS, with the anomalously increasing drive current, suggesting the same oxygen interstitial-dominated trapping mechanism[17,29,30] as at room temperature. All devices show negative ΔV_T under NBS, which can be attributed to the (i) thermal release of electrons due to oxygen vacancy ionization[11] or (ii) de-trapping of electrons[31,32] from deep dielectric traps, both also explaining the negligible NBS effect at room temperature.

Figure 5(m) plots ΔV_T at 120 °C of all top-gated transistors after 1000 s stress, for different stress voltages. All samples show increased $|\Delta V_T|$ with increasing PBS voltage but have weak dependence on NBS voltage magnitude, mainly due to the flat electric field in the middle of the channel, once the channel is fully depleted.[33] The 10%, 14%, and 18% O_2 ITO transistors (blue circles, purple squares, and orange diamonds, respectively) attain this full-depletion state at slightly different negative biases, due to their different turn-on voltages.

Figures 6(a) and 6(b) show the stress-relaxation of our top-gated 10% O_2 ITO transistors under PBS and NBS respectively, with both the stress and relaxation measured at 85 and 120 °C, for 1000 s. The PBS shows slow evolution of ΔV_T in the positive direction during the relaxation stage at 0 V gate voltage. Due to the negative V_T of the 10% O_2 ITO channel devices, this relaxation field is not applied at the off state of the transistor. However, during NBS (i.e., voltage applied at the off-state), the devices continue to show a negative V_T shift trend, which suggests that the high-temperature stability degradation mechanism is not reversible by the application of an electric field of opposite polarity. Similar behavior is observed for the 14% O_2 ITO transistors in Figs. 6(c) and 6(d). Figures 6(e) and 6(f) show the same plots for 18% O_2 ITO devices, revealing a recoverable process, dominated by electron trapping in channel oxygen interstitials. Due to the oxygen-rich channel, free electron release by thermal ionization of neutral oxygen vacancies is suppressed here.

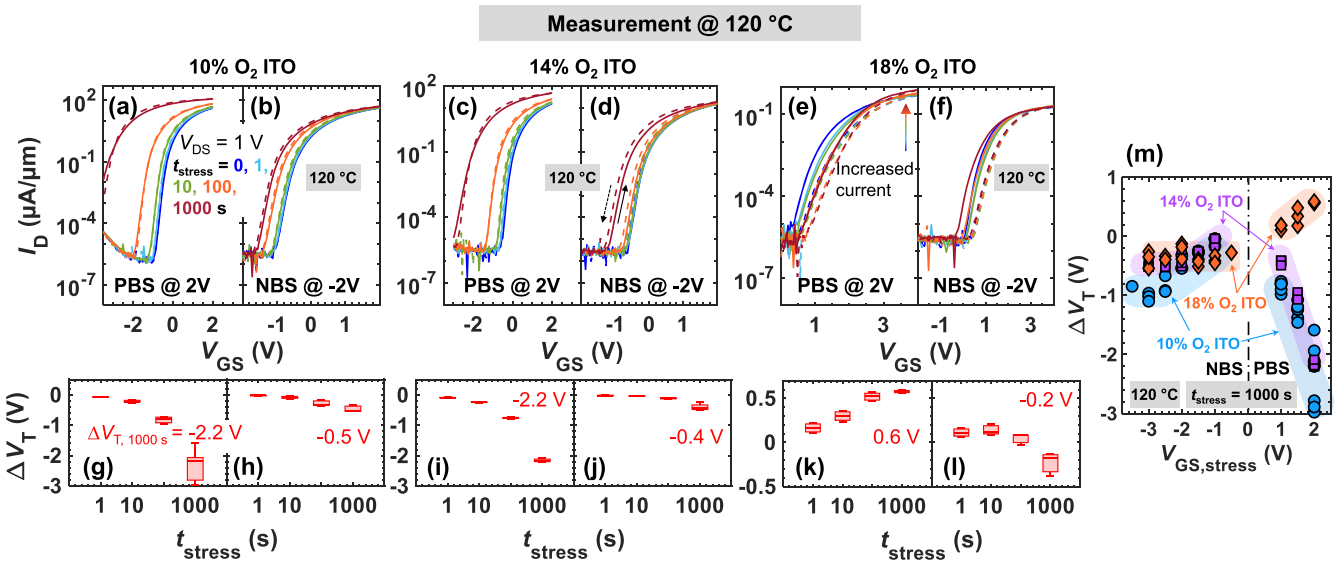


FIG. 5. Measured I_D vs V_{GS} of top-gated ITO transistors under (a), (c), and (e) positive and (b), (d), and (f) negative bias stress, **measured at 120 °C**. Devices with [(a) and (b)] 10%, [(c) and (d)] 14%, and [(e) and (f)] 18% O_2 flow during ITO sputtering. The solid and dashed curves mark sweep directions, as indicated. [(g)–(l)] Evolution of stress-induced V_T shift, ΔV_T with stress time, t_{stress}, corresponding to the panels (a)–(f), with *median* ΔV_T after 1000 s stress denoted in each panel. ΔV_T is defined as the difference between unstressed V_{T0} and stressed V_T after 1000 s stress: $\Delta V_T = V_{T,\ 1000\ s} - V_{T0}$. Here, V_T is extracted at constant current = (W/L) × 10 nA. Each box-and-whisker group represents data from 3 to 9 devices. The error bars in (g)–(l) illustrate the spread of data in the box plots. All devices are ~2 μm long. (m) V_T shift, ΔV_T after 1000 s stress vs gate bias stress voltage, $V_{GS,stress}$ for top-gated ITO transistors at 120 °C. PBS $|\Delta V_T|$ increases with increasing stress voltage, and NBS voltage has no effect on ΔV_T once the channel is fully depleted.

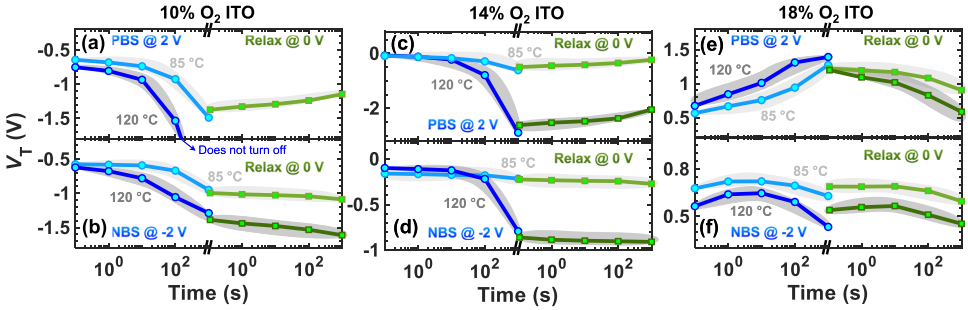


FIG. 6. Evolution of V_T with time under stress (curves with blue circles) and relaxation (curves with green squares) for top-gated [(a) and (b)] 10%, [(c) and (d)] 14%, and [(e) and (f)] 18% O_2 ITO transistors, measured at high temperature (85 °C, 120 °C), using pulsed measurement. Panels [(a), (c), and (e)] and [(b), (d), and (f)] are for PBS and NBS, respectively. All devices are ~2 μm long. The light and dark gray shaded areas in all panels illustrate the data trends at 85 and 120 °C, respectively.

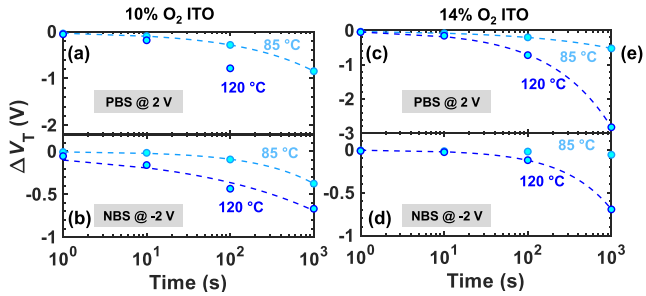
For 10% and 14% O_2 ITO channels, the degradation of V_T under stress seems to follow a systematic time- and temperature-dependent trend, which can be modeled as $\Delta V_T = At_{stress}^n \exp(-E_A/k_BT)V_{GS,stress}^m$, where A, n, E_A, m are a proportionality constant, the time exponent, activation energy, and voltage exponent, respectively. The fitted curves are shown in Figs. 7(a)–7(d) with dashed lines. With A = 1.2 and m = 1, the extracted values of n and E_A are listed in Fig. 7(e).

Both 10% and 14% O_2 ITO channels show similar activation energies under PBS at 85 °C, but the slightly higher n for the 10% O_2 ITO (0.47 vs 0.41) indicates that with increased oxygen vacancies in the channel, the degradation kinetics become more diffusion-limited. At 120 °C, the 14% O_2 ITO also exhibits a higher time exponent ($n \approx 0.60$) together with a similar activation energy ($E_A \approx 0.14$ eV compared to 0.13 eV at 85 °C), indicating a shift toward more diffusion-limited behavior, likely due to increased vacancy generation at elevated temperature.

Under NBS, the two channels exhibit distinct temperature-dependent degradation mechanisms. At 85 °C, the 10% O_2 ITO shows measurable degradation with relatively high n and E_A, indicating diffusion-assisted defect kinetics, whereas the 14% O_2 ITO shows negligible shift, suggesting that the dominant NBS pathway is suppressed in the more oxygen-rich channel. At 120 °C, the 14% O_2 ITO activates a thermally assisted vacancy pathway, leading to diffusion-like behavior ($n > 0.5$), while the 10% O_2 ITO transitions to more dispersive, trap-limited kinetics, likely due to competing recovery and redistribution processes at elevated temperature. Since relaxation after PBS or NBS is negligible in these channels, their behavior cannot be adequately described by Arrhenius-like degradation models.

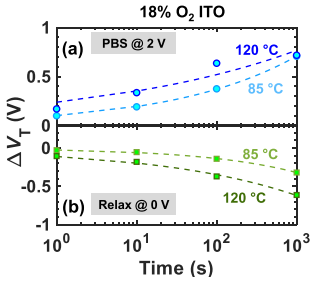
For the most oxygen-rich channel (18% O_2 ITO), PBS induces a mostly recoverable V_T shift. Accordingly, fitting an Arrhenius-type model (Fig. 8) yields $n < 0.5$ and low $E_A \approx 0.1$ eV, consistent with predominantly reversible, shallow trapping or de-trapping dynamics rather than irreversible defect generation, as seen in the lower oxygen composition (10% and 14% O_2 ITO) channels. The NBS response of the 18% O_2 ITO is non-monotonic, showing an initial increase in V_T followed by partial reversal at longer times [Fig. 6(f)], indicating competing reversible trapping and relaxation processes. As a result, this behavior cannot be captured by a simple Arrhenius-type degradation model.

Although our discussion primarily focuses on oxygen-related defects induced by temperature and processing conditions, the migration of hydrogen defects between the channel and dielectric,[13,28] or charge trapping at the gate-to-dielectric interface[34] could also partially contribute to the observed effects. A more



Channel	Stress	Temp.	n	E_A (eV)
10% O_2 ITO	PBS	85 °C	0.47	0.13
		120 °C	N/A	N/A
	NBS	85 °C	0.61	0.19
		120 °C	0.28	0.11
14% O_2 ITO	PBS	85 °C	0.41	0.13
		120 °C	0.60	0.14
	NBS	85 °C	N/A	N/A
		120 °C	0.75	0.22

FIG. 7. Plot of threshold voltage shift (ΔV_T) vs stress time (t_{stress}), modeled by Arrhenius law (dashed lines) for top-gated [(a) and (b)] 10% and [(c) and (d)] 14% O_2 ITO transistors, measured at high temperature (85 °C, 120 °C), using pulsed measurement. Panels [(a) and (c)] and [(b) and (d)] are for PBS and NBS, respectively. All devices are ~2 μm long. (e) Extracted values of the time exponent, n, and activation energy, E_A, for different temperature and stress conditions. The "N/A" indicates cases where the ΔV_T is negligible or beyond the measurement limit.



(c)

Channel	Stress	Temp.	n	E_A (eV)
18% O_2 ITO	PBS	85 °C	0.28	0.10
		120 °C	0.17	0.08
	PBS Relax	85 °C	0.37	0.12
		120 °C	0.25	0.08

FIG. 8. Plot of threshold voltage shift (ΔV_T) vs stress time (t_{stress}), modeled by Arrhenius law (dashed lines) for top-gated 18% O_2 ITO transistors under (a) positive bias stress (PBS) and (b) subsequent relaxation, measured at high temperature (85 °C, 120 °C), using pulsed measurement. All devices are ~2 μm long. (c) Extracted values of the time exponent, n, and activation energy, E_A, for stress and relax conditions at different temperatures.

targeted investigation of hydrogen-related effects, including deuterium annealing[35] or hydrogen-free process integration, together with additional modeling and characterization studies, is needed to differentiate between these potential mechanisms.

In conclusion, we studied positive and negative bias temperature stability of top-gated ITO transistors with different oxygen compositions in the channel. From time-dependent stress and relaxation measurements, we explored the physical mechanisms of stability degradation at high temperature and associated them with process-dependent defects generated in the dielectric or channel layer. Such understanding based on different processing conditions provides important insight for reliable operation of oxide channel transistors.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Sumaiya Wahid: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **Alwin Daus**: Conceptualization (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **Eric Pop**: Conceptualization (equal); Investigation (equal); Methodology (equal); Resources (equal); Software (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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