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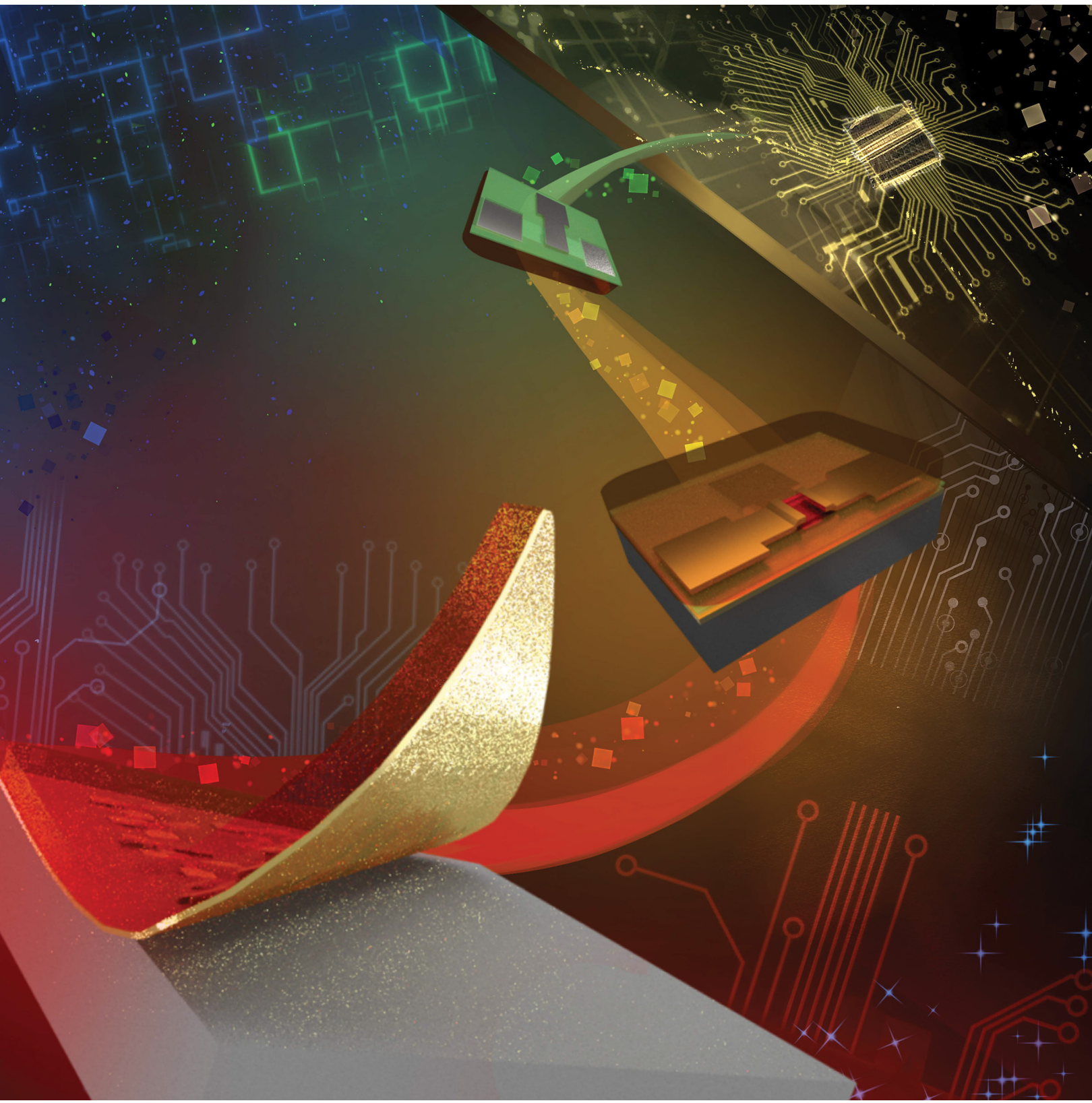

WAHID ET AL.

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Research Article

Flexible Nanoscale Amorphous Oxide Transistors with a Gold-Assisted Transfer Method

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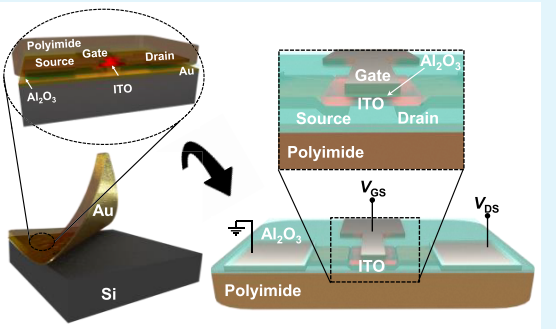
ABSTRACT: We present a new approach to achieve nanoscale transistors on ultrathin flexible substrates with conventional electron-beam lithography. Full devices are first fabricated on a gold sacrificial layer covering a rigid silicon substrate, and then coated with a polyimide film and released from the rigid substrate. This approach bypasses nanofabrication constraints on flexible substrates: (i) electron-beam surface charging, (ii) alignment inaccuracy due to the wavy substrate, and (iii) restricted thermal budgets. As a proof-of-concept, we demonstrate ∼100 nm long indium tin oxide (ITO) transistors on ∼6 μm thin polyimide. This is achieved with sub-20 nm misalignment or overlap between source (or drain) and gate contacts on flexible substrates for the first time. The estimated transit frequency of our well-aligned devices can be up to 3.3 GHz, which can be further improved by optimizing the device structure and performance.



KEYWORDS: *amorphous oxide, indium tin oxide (ITO), transistors, flexible substrate, polyimide*

INTRODUCTION

Electronics on thin, lightweight, bendable substrates could be essential for many future applications in healthcare, wearable systems, and Internet-of-Things (IoT), which require conformal, nonplanar form factors. Cost-effective, flexible thin-film transistors (TFTs) can complement silicon technology and greatly expand its range of applications. In this regard, amorphous oxide semiconductors are highly suitable due to their large-scale manufacturability and electronic transport properties including good electron mobility[1] (>10 cm^2 V^{-1} s^{-1}) and low off-state current[2] (<10^{-20} A/μm). However, electronics with nanoscale features are difficult to pattern on ultrathin flexible substrates using approaches such as electron beam (e-beam) lithography (EBL).

One difficulty is the insulating nature of flexible substrates, leading to charging effects (when EBL is used) and focusing challenges. Depositing a thin metal or conductive polymer layer[3,4] can dissipate these surface charges, but removing this layer can be cumbersome and poses its own limitations. Other high-resolution nanopatterning techniques such as extreme or deep ultraviolet lithography remain unexplored for flexible substrates. Regardless, any patterning technique directly applied on nonflat, wavy, flexible substrates suffers from misalignment issues in subsequent exposures and can limit the performance of nanoscale devices. For transistors, such alignment inaccuracy requires the use of large overlap (>1 μm)[3,5] between the gate and source/drain contacts, which leads to increased parasitic capacitance and limited high frequency performance.

Another difficulty associated with flexible substrates concerns their low thermal budget (≤250 °C), which limits the deposition and/or anneal temperature of thin films. For amorphous oxide TFTs based on indium tin oxide (ITO), which have higher mobility than conventional InGaZnO (μ_{ITO} > 30 cm^2 V^{-1} s^{-1}, μ_{IGZO} ≈ 10 cm^2 V^{-1} s^{-1}),[6,7] a top-gated configuration can be difficult to achieve[8] as it requires annealing at ≥200 °C for good gate modulation.[6] This has more commonly led to demonstrations of back-gated, uncapped transistors, which are not well-suited for circuit implementation.[9,10] All of these issues hinder the potential of nanoscale flexible TFTs.

Given these challenges, some approaches to flexible electronics have first prepared circuit elements on a rigid substrate, before transferring them to flexible substrates using insulating sacrificial layers, such as epoxy resin[11] or polyvinyl alcohol (PVA),[12] or thermal release tapes.[13] However, these methods have not demonstrated nanoscale device features, and

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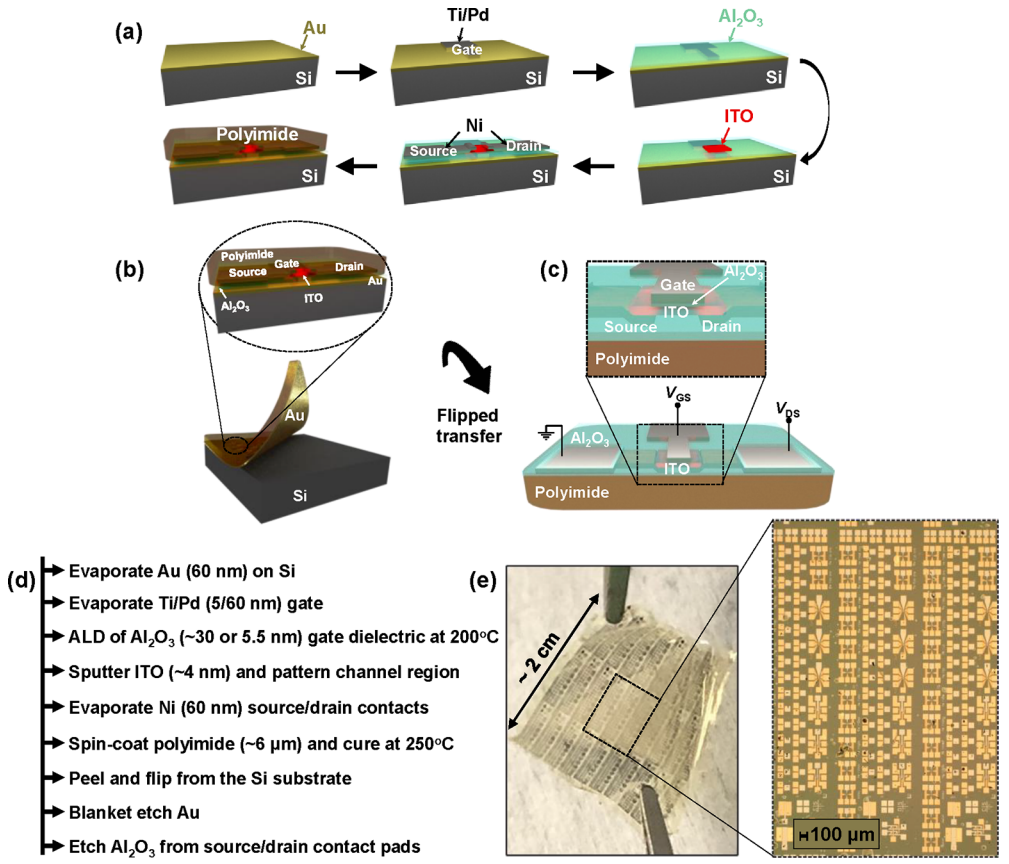

Figure 1. (a) Schematic of the fabrication process steps. (b) Delamination of fully formed ITO device layer from the Si substrate and (c) the final device structure on flexible polyimide (PI) after etching the sacrificial Au. (d) List of detailed fabrication steps. (e) Optical image of an approximately 2 cm × 2 cm flexible PI substrate with arrays of ITO devices and test structures (e.g., for transfer length method), after successful release from Si. The inset shows a zoomed-in microscopy image of the transferred structures and test pads.

they may not lend themselves to EBL nanopatterning due to the insulating layers in the stack.

In this work, we present a water-based transfer approach to achieve nanoscale TFTs on ultrathin polyimide (PI) by first fabricating them on conventional rigid substrates before their release and transfer. We prepare nanoscale back-gated ITO transistors (down to ~100 nm channel length with sub-20 nm misalignment) on a silicon substrate with e-beam lithography and transfer them onto PI using gold (Au) as a sacrificial layer. The conductive and low-adhesion sacrificial metal layer like Au (or Ag) ensures the ease of transfer, and it facilitates EBL by avoiding surface charge buildup. This transfer method also ensures that the final device structure is flipped upside-down to a top-gated transistor configuration, while the EBL on silicon ensures relatively conventional lithography as well as good resolution and alignment accuracy. We also estimate the transit frequency (f_T) of our fabricated transistors to quantify the advantage of such near-perfect alignment. Overall, our technique can be used to realize not only nanoscale flexible TFTs but also other devices requiring precise alignment and/or higher thermal budget, and thus, it can facilitate a variety of flexible electronic devices.

RESULTS AND DISCUSSION

As shown in Figure 1a, we first deposit a 60 nm thick e-beam evaporated Au film on Si; this film will later serve as a sacrificial layer for the transfer process because Au has low adhesion to Si and easily detaches when immersed in deionized water.[14] We then fabricate a back-gated staggered transistor structure on top of the Au film. First, we pattern the nanoscale gate by EBL and deposit the gate metal by e-beam evaporation of Ti/Pd (5/60 nm), followed by atomic layer deposition (ALD) of ~5.5 and ~30 nm thick Al_2O_3 as the gate dielectric, for two types of samples. Next, we deposit ~4 nm thick ITO as the channel material for both samples, using radio frequency (RF) magnetron sputtering at room temperature, at 100 W RF power, 5 mTorr pressure, and 10% O_2 partial pressure.[6]

The transistor channel region is defined by optical lithography and then patterned by wet etching in 1.7% hydrochloric acid. Finally, the source and drain electrodes are defined by EBL, followed by e-beam evaporation of Ni (60 nm) and lift-off. The separation between source and drain defines the channel length (L), between 100 and 600 nm. Large-area pads for electrical probing are defined by optical lithography and lift-off, using the same metals as their respective electrodes.

Figures 1b and 1c illustrate the delamination process and a schematic of the completed device on PI, respectively. The details of the fabrication process steps are listed in Figure 1d, while Figure 1e shows the photograph of a ~2 cm × 2 cm flexible substrate with arrays of ITO devices and test structures after successful release from Si. Additional information about the fabrication is given in the Methods section.

An important outcome of this "upside-down" process flow is that it enables the fabrication of top-gated nanoscale ITO transistors without actively depositing the gate dielectric layer

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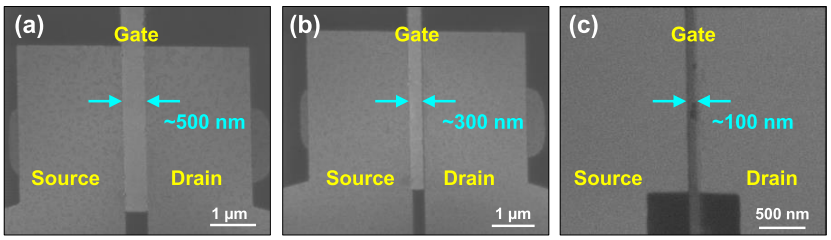

Figure 2. Top-view scanning electron microscopy (SEM) images of fabricated top-gated ITO transistors, showing good alignment accuracy between gate and source/drain contacts for (a) ~500 nm, (b) ~300 nm, and (c) ~100 nm channel lengths (L), with gate-to-contact misalignment only determined by the lithography technique (here <20 nm) on the original Si substrate, not on the wavy, sensitive PI.

onto the channel. Because of better alignment accuracy on the Si substrate, this approach can also facilitate well-aligned structures with minimum overlap between gate and source/drain contacts, which is essential for high-frequency operation. Using this approach, we fabricated transistors down to ~100 nm channel lengths (L), with near-perfect alignment between gate and source/drain electrodes, as shown in Figure 2.

We measured the transfer characteristics (I_D vs V_{GS}) of our top-gated flexible ITO transistors with various channel lengths ($L \approx$ 100, 200, 300, 500, and 600 nm). All electrical measurements were done at room temperature in air using a probe station with a Keithley 4200-SCS parameter analyzer. For the devices with ~30 nm thick Al_2O_3 gate dielectric, we achieved good on-state current ~130 μA/μm for $L \approx$ 300 nm at V_{DS} = 1 V and V_{GS} = 20 V and good on/off current ratio of ~10^8 (Figure 3). The on-state currents for shorter channels (100 and 200 nm) are ~100 μA/μm, likely limited by contact resistance. We note that this staggered top-gate device structure (schematic below the I_D vs V_{GS} curves in Figure 3) without significant gate-to-source/drain overlap has little gate modulation of the contact resistance.[15] In addition, slight misalignment would also cause an ungated channel region, which itself can limit the on-state current, and this misalignment becomes more significant for the shorter channels.

We achieve relatively lower currents for devices with thinner gate dielectrics (~5.5 nm thick Al_2O_3 in Figure 4a), owing to degraded contact resistance. This lower performance can be explained because the conformal ALD of a thicker gate dielectric allows more channel surface area for making top contacts, whereas for thinner dielectric the channel surface area is smaller, resulting in a smaller (sub-10 nm) top contact region (schematic below the I_D vs V_{GS} curves in Figure 4a).

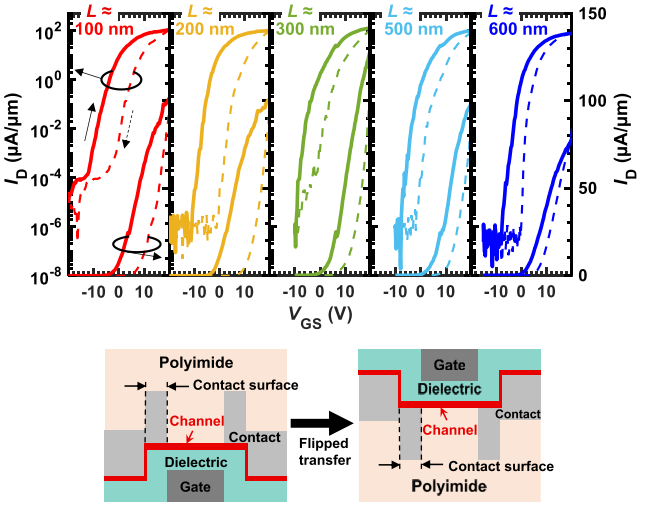

Figure 3. Measured transfer characteristics (I_D vs V_{GS}) of our final top-gated well-aligned ITO transistors with ~30 nm Al_2O_3 gate dielectric on PI substrate, with different channel lengths, L, as labeled in each panel. V_{DS} = 1 V for all measurements, and gate currents were $\leq 10^{-10}$ A, limiting the off-state current for $L \approx$ 100 nm. Solid and dashed small arrows indicate the V_{GS} sweep directions, corresponding to the solid and dashed curves, respectively. For each panel, the left and right axes are in log and linear scales, respectively. Bottom schematics are cross-sections of corresponding device structures before and after transfer onto PI. This illustrates the larger contact surface area enabled by the thicker sidewall deposition of the dielectric.

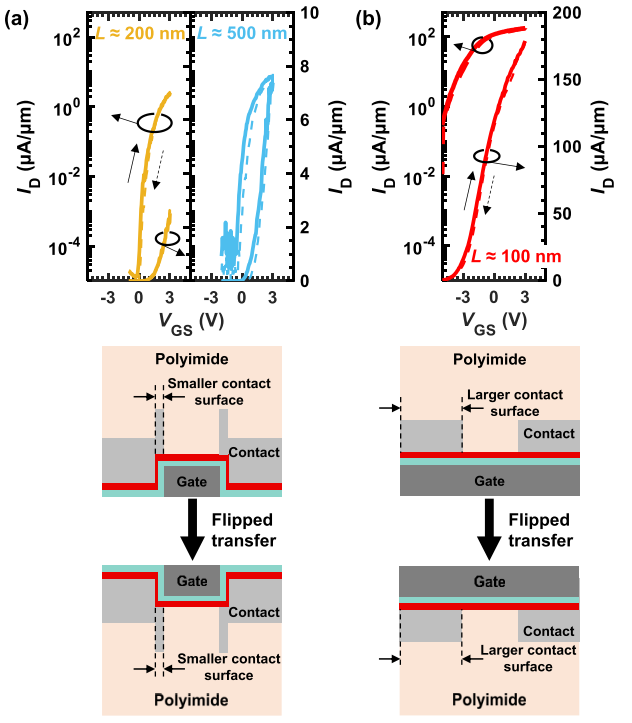

Figure 4. Measured transfer characteristics (I_D vs V_{GS}) of final top-gated ITO transistors with ~5.5 nm Al_2O_3 gate dielectric on PI substrate, having (a) well-aligned gate and (b) overlapped gate, with different channel lengths, L, as labeled in each panel. Gate currents were $\leq 10^{-10}$ A in (a) and up to 10^{-8} A in (b), limiting the off-state current. All measurements are taken at room temperature and V_{DS} = 1 V. Small arrows mark V_{GS} sweep directions, corresponding to the solid and dashed curves, respectively. For each panel, the left and right axes are in log and linear scales, respectively. Bottom schematics are cross-sections of the corresponding device structures before and after transfer onto PI. This illustrates the changes in contact surface area for the different device structures, resulting in varying on-state performance.

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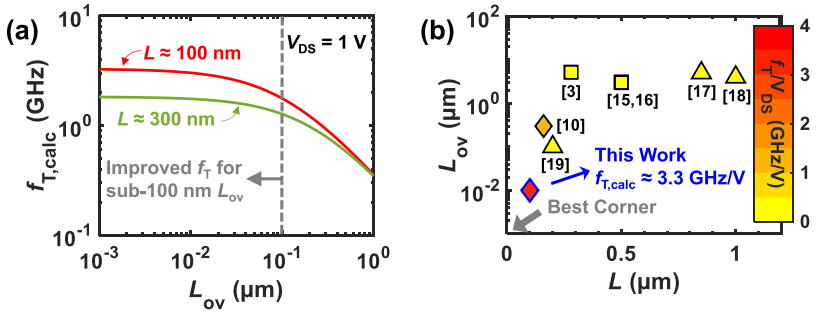

Figure 5. (a) Calculated transit frequency ($f_{T,calc}$) vs overlap length (L_{ov} = total gate overlap with source and drain), showing possible f_T improvement up to 10× by reducing the L_{ov}. The f_T estimate is based on the DC performance of 100 and 300 nm long channel transistors with 30 nm Al_2O_3 dielectric, shown in Figure 3. (b) Benchmark plot of L_{ov} vs channel length (L) for prior flexible TFTs ($L \leq 1$ μm).[3,10,15−19] The symbol colors correspond to the measured f_T/V_{DS} of the various studies and to the colormap on the right (e.g., yellow symbols are below 500 MHz, etc.). The calculated f_T of our work is ~3.3 GHz at $V_{DS} = 1$ V, highlighting the high f_T achievable with reduced L_{ov}. Other existing devices had higher L_{ov} and lower f_T/V_{DS}. Triangular symbols are organic channels, squares are InGaZnO, and the diamonds (including our work) are ITO.

The device in Figure 4a likely makes an edge contact with the channel, leading to poorer contacts. Notably, source/drain contact metals in such oxide transistors can also scavenge oxygen from the channel under the contacts, resulting in more n-doped contact regions and improved contact resistance.[6] The sub-10 nm contact region can barely facilitate this scavenging, further contributing to poor source/drain contacts.

To confirm the role played by the contact surface area, we also measured overlapped gate structures (with ~5.5 nm Al_2O_3), which provide contacts with larger surface and gate modulation, improving the contact resistance and achieving higher currents (Figure 4b). Therefore, this method is likely to benefit from ALD channels, as they can have more conformal sidewall deposition than sputtering, and possibly make better edge contacts with thinner dielectrics. Similarly, embedded and/or planarized gates without the topography could also improve the contact resistance without an additional gate to source/drain overlap.

The calculated f_T of our shortest device ($L \approx 100$ nm) based on its DC performance and geometry[14] can be as high as ~3.3 GHz at $V_{DS} = 1$ V. This estimate is with our device using 30 nm Al_2O_3 gate dielectric, assuming no source/drain-to-gate overlap, and an extrinsic mobility $\mu_{FE} \approx 5.2$ cm^2 V^{-1} s^{-1}, which includes the effects of contact resistance at short channel lengths. We note that the μ_{FE} of our long channel transistors is ~40 cm^2 V^{-1} s^{-1} at room temperature, without the limitations of contact resistance. Because EBL tools can have some inherent misalignment (in the range of few tens of nm), we also calculate the f_T to incorporate that, and Figure 5a shows the trend of calculated f_T for our 100 and 300 nm long channels with various overlapping lengths (L_{ov}, as the total overlap between the gate and source/drain). Notably, f_T can be increased up to 10× by minimizing this overlap from ~1 μm to ~10 nm. Finally, in Figure 5b we demonstrate the lowest overlap length among prior flexible TFTs and compare our estimated achievable f_T with other studies, highlighting the advantages of well-aligned devices.

To test the mechanical stability of our devices, we perform a bending test with a 3 mm radius, as shown in Figure 6a. The device electrical behavior is consistent between "flat" and "bent" conditions (Figure 6b,c), as well as after 100 bending cycles, when returned to the flat condition (Figure 6d). Some hysteresis is apparent in these measurements (yet itself consistent between flat and bent conditions) due to the thicker gate dielectric (~30 nm) used in these devices. This is similar to the hysteresis seen in Figure 3 (~30 nm Al_2O_3 gate dielectric) but absent in Figure 4 (~5.5 nm Al_2O_3 gate dielectric).

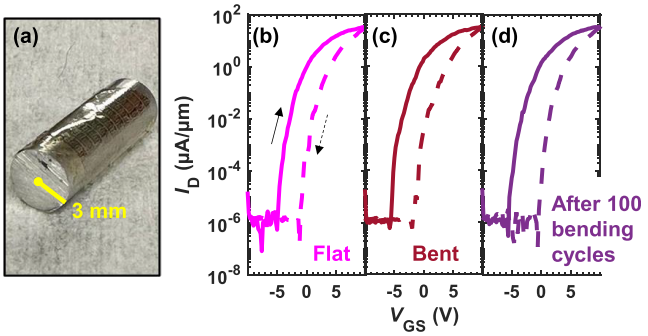

Figure 6. (a) Photograph of the sample bent with a 3 mm radius. Measured I_D vs V_{GS} of top-gated ITO transistors with ~30 nm Al_2O_3 gate dielectric, at room temperature, under (b) flat, (c) bent conditions, and (d) after 100 bending cycles, returned to the flat condition. The same device with $L \approx 200$ nm is measured in (b−d) at $V_{DS} = 1$ V. Small arrows mark forward (solid line) and backward (dashed line) gate voltage sweeps. The measurement instrument noise limit is approached at single-picoampere current levels in the device off-state.

CONCLUSION

We described a new approach to achieve nanoscale TFTs on ultrathin flexible substrates using e-beam lithography, with high alignment accuracy (<20 nm misalignment). As a proof of concept, we apply this here to amorphous oxide semiconductors based on indium tin oxide, but the method is broadly applicable to any flexible electronics that require high-temperature processing (e.g., ferroelectric devices). This transfer process could be used to realize a variety of flexible thin film devices from high-frequency transistors to nonvolatile memory, and enable future low-power and high-performance Internet-of-Things applications.

METHODS

For electron-beam lithography (EBL), we use poly(methyl methacrylate) (PMMA) 495K A2 as the lift-off layer (generating an undercut in the resist stack), followed by PMMA 950K A4, to form the resist stack, each baked at 180 °C for 5 min. Then we use a 1:1 solution of methyl isobutyl ketone (MIBK):isopropyl alcohol (IPA)

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for 30 s for pattern development. This is a solvent-based developer that shows no signs of Au delamination from Si.

For the optical lithography, we use LOL-2000 as the lift-off layer, which is baked at 200 °C for 5 min. Then, SPR 3612 is used as the photoresist layer (baked at 90 °C for 1 min). We use Microposit MF-26A, an aqueous developer containing 2.4% TMAH, to develop the pattern in 30−40 s, followed by a quick rinse in deionized water. To avoid any delamination of Au from Si due to the water-based development, this step must be handled carefully because the patterning is performed directly on Au. Using a thin, uniform insulator layer (like Al_2O_3) on Au before the patterning steps could be helpful to avoid the delamination, if this insulator is not etched by the developer. However, because Al_2O_3 is etched ∼1−2 nm/min in the MF-26A developer, such a dielectric−developer combination was avoided here. For the channel definition step, we use SPR 220-3 as the photoresist (baked at 115 °C for 90 s). We use the same developer in this step for 75 s.

Once our nanoscale devices are fabricated, ∼6 μm of polyimide (PI-2610, HD MicroSystems) is spin-coated on top and cured at 250 °C in a N_2 atmosphere, before releasing the whole stack in deionized water with the help of the Au layer. We then etch the Au using Transene Gold (Au) etchant TFA (containing 42% potassium iodide (KI), 10% iodine (I_2), and 48% water), which avoids etching the gate stack materials. Finally, the source and drain pads are opened for probing by wet etching the Al_2O_3 in Transene Aluminum (Al) Type A etchant (containing 1.5% nitric acid, 50−70% phosphoric acid, 3−10% acetic acid, 15−46% water, and <0.1% nonhazardous surfactant).

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Author Contributions

S.W., A.D., and E.P. conceived the idea and wrote the manuscript. S.W. carried out all fabrication, measurements, and analysis. V.C. prepared graphics and helped with writing.

Notes

The authors declare no competing financial interest.

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