Understanding Interface-Controlled Resistance Drift in Superlattice Phase Change Memory

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***Abstract*— Resistance drift in phase change memory (PCM) reduces the accuracy of analog computing applications such as neural network inference. Recently, PCMs based on superlattice (SL) phase change layers have shown low resistance drift, however the origin of this low drift remains unexplored. Here, we uncover that resistance drift in SL-PCM based on alternating layers of Sb_2Te_3 and $Ge_2Sb_2Te_5$ (GST) is controlled by the number of SL interfaces as well as the degree of SL intermixing. Temperature-dependent measurements reveal smaller and more stable activation energy upon annealing (thus suppressed structural relaxation) in our SL-PCM vs. control GST devices, accounting for the low resistance drift. By controlling SL interfaces, we achieve low resistance drift coefficient $\nu < 0.01$ in these SL-PCMs, maintained after extensive cycling and at various read voltages and intervals - showing robustness required for analog computing with PCM.**

***Index Terms*— Phase change memory, PCM, GST, superlattice, low resistance drift, interface, temperature.**

I. Introduction

PHASE change memory (PCM) is a promising contender for analog compute-in-memory (CIM) due to its non-volatility, large memory window and multi-level programmability [1], [2], [3]. However, PCM resistance drift accounts for a large fraction of the inference accuracy degradation in CIM [4], [5], [6]. In addition, resistance drift can cause merging of intermediate states during multi-level cell programming, resulting in undesired bit errors.

Several methods have been proposed to address these application-level challenges associated with PCM resistance drift. Algorithm-level solutions are being explored, but they often come with increased complexity [6], [7], [8]. Thus, innovations at the material and device level remain important. Earlier efforts to mitigate resistance drift include surfactant PCM and GST composition tuning [9], [10], [11]. While these methods help reduce resistance drift, they often lower the highest resistance state (HRS) and thus decrease the memory window. Recently, superlattice PCM (SL-PCM) with alternating phase change material layers, has been proposed as a promising way to mitigate resistance drift and lower the reset current density [12], [13], [14], [15]. However, the origin of low resistance drift and the role of SL interfaces (the number of SL interfaces and their quality) are less understood.

Here, we first realize a correlation between resistance drift and SL interfaces in SL-PCM based on alternating layers of Sb_2Te_3 and $Ge_2Sb_2Te_5$ (GST). This SL type also allows us to compare the resistance drift with control GST-only devices which have no internal interfaces. We find a decrease of the resistance drift coefficient (ν) with increasing number of clean SL interfaces, however ν increases when intermixing and non-idealities occur within the SL. With an optimized SL using 2 nm/1.8 nm Sb_2Te_3/GST, we obtain a low $\nu < 0.01$ and as low as $\sim$0.002 measured for 10^5 seconds. Using temperature-dependent measurements, we further explore the activation energy in our SL-PCM vs. control GST devices, providing insight into the origin of the SL-PCM low drift. The low resistance drift shows good robustness upon measurements at different read stress, as well as after extensive electrical cycling (10^6 times) and annealing (85°C), promising for high-density multibit operation and PCM-based neuromorphic applications.

II. Device Fabrication and Characterization

Fig. 1(a) shows a schematic of our SL with alternating Sb_2Te_3 and GST layers sputtered at 180°C. The total thickness of the SL stack was $\sim$65 nm including $\sim$4 nm Sb_2Te_3 seed layer. The SL stacks were capped *in situ* with 10 nm TiN to prevent oxidation of the SL. The high-quality SL deposition process was further detailed in [13]. **Figs. 1(b, c)** show high-resolution scanning transmission electron microscopy (STEM) images of our SLs [2/1.8 nm/nm Sb_2Te_3/GST in **(b)** and 4/1.8 nm/nm in **(c)**] revealing sharp internal interfaces and van-der Waals (vdW)-like gaps. (We note some intermixing can occur between the ultrathin layers over larger areas [13], [14], [16].) **Fig. 1(d)** displays the scanning electron microscopy (SEM) cross-section of a fabricated SL-PCM device with TiN/Pt top electrode (TE) and TiN bottom electrode (BE). Similar mushroom-cell control devices were

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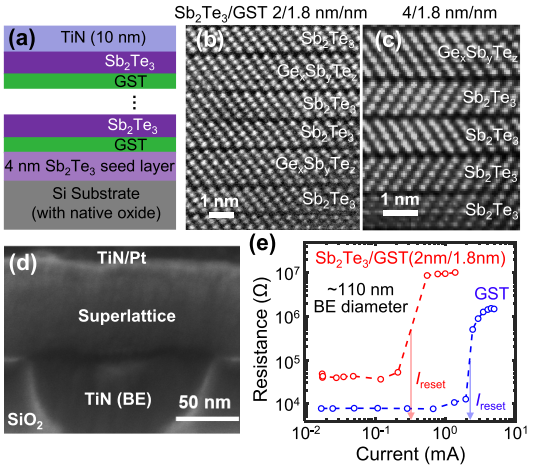

Fig. 1. Device Structure and Characterization: (a) Schematic, and (b, c) high-resolution STEM images of our Sb_2Te_3/GST superlattice (SL) films on a Si substrate (with native oxide) showing vdW-like gaps; 2/1.8 nm/nm and 4/1.8 nm/nm Sb_2Te_3/GST SLs are shown in (b) and (c), respectively. The layered structure is preserved on a TiN electrode, as imaged by TEM in [13] and [14]. (d) SEM cross-section of a mushroom-cell SL-PCM device with ~160 nm bottom electrode (BE) diameter. (e) Measured DC resistance vs. current comparing our SL-PCM and control GST PCM mushroom cells. Arrows mark I_{reset}, taken at 10x resistance change from the low-resistance state (LRS).

fabricated with GST, without internal interfaces. To understand the influence of SL interfaces on resistance drift, we also fabricated SL-PCM with different period thicknesses. The devices were programmed using 1/20/300 ns (set) and 1/20/1 ns (reset) rise/width/fall pulses. The measurement details have been described in our previous work [13].

III. Results and Discussion

Fig. 1(e) shows representative resistance (R) vs. current (I) plots for our SL-PCM vs. control GST-only devices. The reset current in Sb_2Te_3/GST (2/1.8 nm/nm) SL-PCM is notably lower than control GST PCM, due to strong electro-thermal confinement caused by internal SL interfaces [14], [17]. R vs. time measurements in **Fig. 2(a)** show >10× lower resistance drift in the same SL-PCM device (drift coefficient $\upsilon \sim 0.002$) vs. GST PCM ($\upsilon \sim 0.12$), both with ~110 nm BE diameter. However, as shown in **Fig. 2(b)**, the resistance drift increases with larger SL period, i.e., fewer SL interfaces (e.g., 4/1.8 nm/nm and 16/14.4 nm/nm SLs). This suggests that structural confinement and vdW-like gaps play an important role in reducing the resistance drift.

We further find that a higher degree of intermixing (i.e., loss of vdW-like gaps, stacking faults, and disordering) within SL layers also increases the resistance drift. This is evident from our measurement [**Fig. 2(b)**] of 2/0.6 nm/nm SL-PCM, deliberately fabricated with thinner GST than its unit block thickness (~1.8 nm) to introduce intermixing [16]. **Fig. 2(c)** captures the trend between the drift coefficient (υ) and the number of SL interfaces, highlighting an interface-controlled behavior of resistance drift in SL-PCM.

To understand the origin of low resistance drift in SL-PCM, we performed temperature (T)-dependent resistance measurements and extracted the conduction activation energy (E_a) of both GST and SL-PCM devices, using $R(T) = R_0 \exp[E_a/(k_B T)]$, where T is the absolute temperature at which resistance is measured, and R_0 is the initial resistance at time $t = 0$. **Fig. 3(a)** displays the estimated E_a from R vs. T measurements, showing slightly lower E_a in SL-PCM with more interfaces. We note that the measurement temperatures were below room temperature (RT), down to 258 K, to minimize the impact of thermally-activated resistance drift. In other words, measurements above RT would lead to an underestimation of E_a due to temperature-accelerated resistance drift during ramp-up to the higher temperatures [18].

Figs. 3(b, c) show the effect of annealing temperature (T_a, for 30 minutes) on the HRS and E_a, respectively, for both SL-PCM and GST. Such annealing is expected to accelerate resistance drift and is thus equivalent to assessing the long-term drift at RT [18]. Both E_a and HRS show an increasing trend with T_a for GST (no internal interfaces) and SL-PCM with fewer interfaces (e.g., 4 internal interfaces for 16/14.4 nm/nm). On the contrary, an SL-PCM device with higher number of SL interfaces (e.g., 2/1.8 nm/nm SL-PCM with 32 SL interfaces) displays a negligible change in both E_a and HRS even after 85°C annealing for 30 minutes (after which the resistance drift is expected to approach saturation [19]). In fact, we observe a ~5× increase in HRS and ~0.5 eV increase in E_a in our control GST devices, consistent with previous reports [18], [20]. This confirms that the increased E_a corresponding to more structural relaxation is mostly accountable for the T-dependent resistance increase in GST [21]. In contrast, negligible change of E_a upon annealing in 2/1.8 nm/nm SL-PCM points at less structural relaxation with increased number of SL interfaces, leading to a low resistance drift.

Thus, the resistance drift coefficient (υ) is correlated with E_a before annealing as well as with the change in E_a (i.e., ΔE_a) upon annealing at 85 °C (**Fig. 3d**). SL-PCM devices with more SL interfaces (2/1.8 nm/nm) show the lowest E_a or ΔE_a and correspondingly lowest υ, due to better structural confinement in the phase change layers leading to less structural relaxation. In contrary, GST PCM with no internal interfaces and the least structural confinement has more pathways for structural relaxation (as evidenced by larger E_a or ΔE_a upon annealing), resulting in larger resistance drift. This is also in agreement with other chalcogenide material systems [22] and resistance drift models [23].

We further explore the robustness and endurance of the low resistance drift in SL-PCM with 2/1.8 nm/nm Sb_2Te_3/GST and the same total thickness (~65 nm). The low drift coefficient ($\upsilon < 0.01$) is maintained after extensive ($>10^6$) cycling [**Fig. 4(a)**]. Low resistance drift is also retained [**Fig. 4(b)**] for various read stress, down to 1 second read interval shown here. **Fig. 4(c)** shows that υ remains low upon measurement at different read voltages, suggesting that electric field acceleration of resistance drift is absent in SL-PCM. Measurements on SL-PCM devices (2/1.8 nm/nm) with different BE diameters confirm the low resistance drift [averaged over 5 devices for each diameter in **Fig. 4(d)**] showing promise for achieving the same in SL-PCM with sub-100 nm BE diameter. We note that resistance drift is also low ($\upsilon < 0.01$) in the low-resistance state (LRS) of our devices.

Fig. 5 compares the drift coefficients (υ) of Sb_2Te_3/GST SL-PCM in this work with other PCM technologies, including doped GST [8], [24], [25], projected PCM [9], [10], [11], $TiTe_2/Sb_2Te_3$ heterostructure [15], bilayer PCM [26], and other materials [27], [28], [29]. The lowest resistance drift is obtained in our 2/1.8 nm/nm Sb_2Te_3/GST SL-PCM [**Fig. 5(a)**]

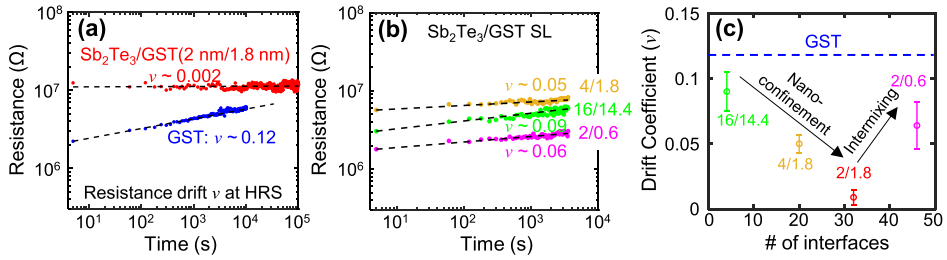

Fig. 2. Interface-Controlled Resistance Drift in SL-PCM: (a) Highest resistance state (HRS) vs. time revealing low resistance drift in SL-PCM (vs. control GST-PCM without internal interfaces) measured up to 10^5s. Dashed lines are fit to the power-law $R(t) \sim (t/t_0)^{\nu}$, where t is the time after programming, t_0 is an arbitrarily chosen constant, and ν is the resistance drift coefficient. (b) Resistance drift for varying number of SL interfaces (e.g., 4/1.8 nm/nm Sb_2Te_3/GST, etc.) and different degree of intermixing. The DC resistance is measured at 0.05 V every 60 seconds. (c) Resistance drift coefficient (ν) vs. number of SL interfaces, capturing the effects of nanoconfinement and SL layer intermixing. The error bars are calculated from drift measurements for five devices and five different cycles of each device, capturing device-to-device and cycle-to-cycle variations.

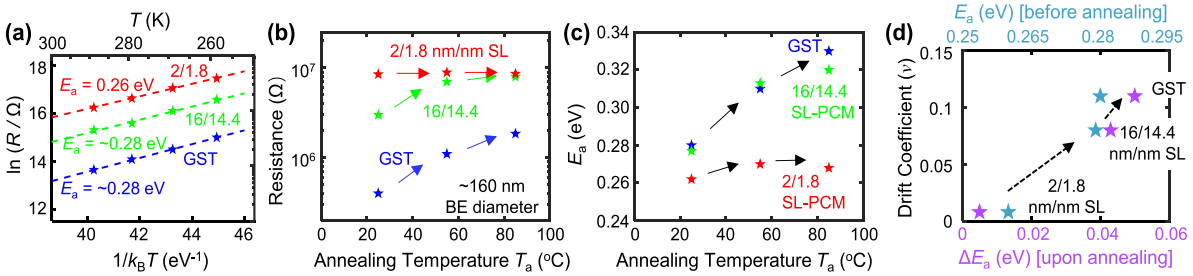

Fig. 3. Effect of Annealing on HRS and Conduction Activation Energy: (a) Extraction of conduction activation energy (E_a) for as-programmed SL-PCM and GST devices at HRS. Devices were programmed at room temperature and cooled down while resistance was measured. (b) HRS measured at room temperature (RT) after 30-minute anneals at varying temperatures. (c) E_a vs. annealing temperature comparing SLs with varying interfaces and control GST, showing negligible change in both HRS and E_a for 2 nm/1.8 nm SL-PCM even after high temperature annealing for 30 minutes. Devices are cooled down after each annealing cycle to obtain RT resistance and E_a. (d) Resistance drift coefficient as a function of E_a (before annealing) and as a function of the increase in E_a i.e., ΔE_a (upon annealing at 85 °C) comparing different SL-PCM devices with varying number of interfaces and control GST-only PCM.

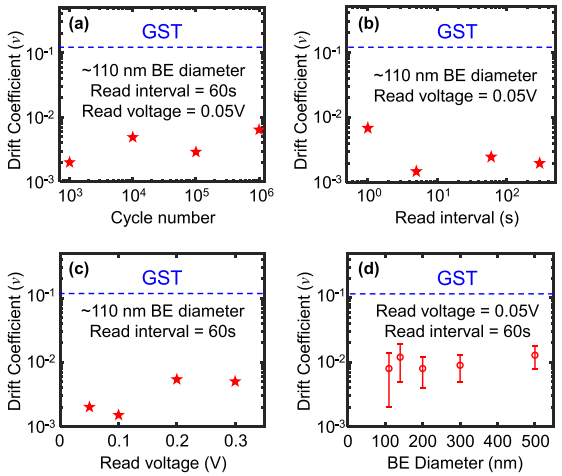

Fig. 4. Robustness and endurance of low resistance drift in SL-PCM with 2 nm/1.8 nm Sb_2Te_3/GST: Resistance drift coefficient (ν) measurements (a) after various electrical switching cycles, (b) at several read intervals, (c) different read voltages, and (d) for various BE diameters of the SL-PCM devices (5 devices for each BE diameter). Resistance drift coefficients are extracted from R vs. time measurements (not shown) on well-cycled SL-PCM devices at room temperature measured for 1 hour. All the devices were cycled for $>10^3$ times using a write-verify scheme.

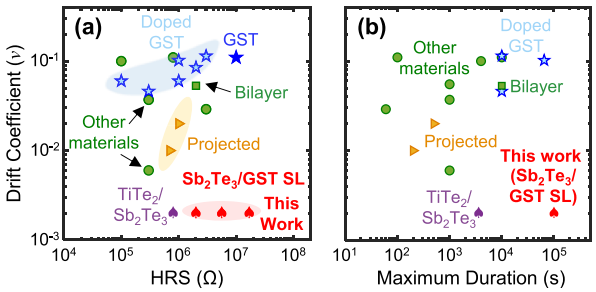

Fig. 5. (a) Benchmarking drift coefficient (ν) vs. highest resistance state (HRS) for various PCMs [8], [9], [10], [11], [15], [24], [25], [26], [27], [28], [29] and our SL-PCMs with different BE diameters (200, 160, 110 nm from left to right). (b) Drift coefficient vs. duration of drift measurement for various PCMs [8], [10], [11], [15], [24], [25], [26], [27], [28], [29] and our SL-PCMs. Bilayer refers to Bi_2Te_3/GST [26], and 'other materials' include nanoconfined Sb [27], [28], and $Cr_2Ge_2Te_6$ [29].

without sacrificing the achieved HRS. Resistance drift in SL-PCM remains negligible up to 10^5 seconds [**Fig. 5(b)**], promising for multibit PCM and neuromorphic applications. Our SL-PCM technology can also be combined with other approaches to mitigate resistance drift, such as elemental doping [24] and thus could lead to further improvement in resistance drift of SL-PCM.

IV. Conclusion

In summary, we uncover the role of interfaces and intermixing of superlattice (SL) layers in controlling the resistance drift of SL-PCM. We also measure lower activation energy in Sb_2Te_3/GST SL-PCM devices (with numerous SL interfaces) correlating to a reduced structural relaxation and thus lower resistance drift in SL-PCM compared to control GST-only PCM. By tuning the number and quality of SL interfaces, we demonstrate low resistance drift in our SL-PCM, robust against extensive endurance cycling and read stress, showing promise for multibit storage and neuromorphic computing.

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