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Low-Power Switching of Phase-Change Materials with Carbon Nanotube Electrodes

Feng Xiong,[1,2] Albert Liao,[1,2] David Estrada,[1,2] Eric Pop[1,2,3]*

[1]Micro & Nanotechnology Lab, University of Illinois, Urbana-Champaign, IL 61801, USA. [2]Dept. of Electrical & Computer Eng., University of Illinois, Urbana-Champaign, IL 61801, USA. [3]Beckman Institute, University of Illinois, Urbana-Champaign, IL 61801, USA.

*To whom correspondence should be addressed. E-mail: epop@illinois.edu

Phase-change materials (PCMs) are promising candidates for nonvolatile data storage and reconfigurable electronics, but high programming currents have presented a challenge to realize low power operation. We controlled PCM bits with single-wall and small-diameter multi-wall carbon nanotubes. This configuration achieves programming currents as low as 0.5 μA (SET) and 5 μA (RESET), two orders of magnitude lower than state-of-the-art devices. Pulsed measurements enable memory switching with very low energy consumption. Analysis of over one hundred devices finds that the programming voltage and energy are highly scalable, and could be below 1 V and single femtojoules per bit, respectively.

Phase-change materials (PCMs) are typically chalcogenides like $Ge_2Sb_2Te_5$ (GST) which have amorphous (a) and crystalline (c) phases with contrasting electrical and optical properties. PCMs are the active material in rewritable DVDs, where phase transformations are induced and read by a pulsed laser (*1, 2*). The data in electrically-programmable PCMs are stored as changes in bit resistivity (*3-6*), which can be reversibly switched with short voltage pulses and localized Joule heating. In this sense, PCMs are appealing vs. other semiconductor memories where data are stored as charge and are susceptible to leakage and volatile behavior. Electrically-programmable PCMs have captivated wide interest for applications in non-volatile memory (*7, 8*) and reprogrammable circuits (*5, 6*) with low voltage operation, fast access times, and high endurance (*3, 4*). These attributes make them contenders for a 'universal' non-volatile memory, which could replace all data storage from random-access memory to hard disks. However, a drawback of PCMs is their high programming current (>0.1 mA), as Joule heat must be coupled to a finite bit volume, previously achieved with 30 to 100-nm diameter nanowires (*9-11*) or metal vias (*12-14*).

We used carbon nanotubes (CNTs) with diameters ~1 to 6 nm as electrodes (*15, 16*) to reversibly induce phase change in nanoscale GST bits. Our findings address the potential size and power reduction that are possible for programmable bits of PCM. We demonstrate reversible switching with programming currents from 1 to 8 μA, two orders of magnitude lower than state-of-the-art PCM devices. We also present a device scaling study that suggests memory switching is possible with voltages below 1 V and energy less than femtojoules per bit.

The CNTs used in this work were grown by chemical vapor deposition (CVD) with Fe catalyst particles on SiO_2/Si substrates (*17, 18*) [also see online supplement (*19*)]. We obtained single-wall and small diameter multi-wall CNTs, and we found that both can be used to switch GST bits. The as-grown CNTs span Ti/Pd (0.5/40 nm) metal contacts with 1 to 5 μm separation (fig. S1 (*19*)). We then created nanoscale gaps in the CNTs through electrical breakdown (*20*) in air or under Ar flow, as illustrated in Fig. 1 and the left inset to Fig. 2A. This simple approach yielded a wide range of nanogaps (from ~20-300 nm) in more than 100 devices, which was essential for our subsequent scaling study. The nanogap is typically near the middle of the CNT, consistent with the electrical breakdown location and with negligible Pd contact resistance (*20, 21*). Then, a ~10-nm GST film was sputtered over the device surface (fig. S2 (*19*)), with settings previously found to preserve the electrical characteristics of CNTs (*18*). This deposition fills the CNT nanogaps, creating self-aligned lateral PCM bits. Such devices can be readily switched and examined by atomic force microscopy (AFM) (Fig. 2); however, a ~5-nm SiO_2 layer deposited after the GST without breaking vacuum (*12*) must be used to prolong the switching lifetimes.

Devices are initially in the OFF state (Fig. 1C) because the as-deposited GST films are amorphous (a-GST) and highly resistive, R_{OFF} ~ 50 MΩ (*22*). A voltage applied at the CNT contacts creates a sizeable electric field (*E*-field) across the nanogap, and switches the GST bit to the crystalline phase (c-GST), which lowers the resistance by about two orders of magnitude, to R_{ON} ~ 0.5 MΩ. Although a-GST covers the entire device, the switching occurs only in the nanogap, which is the location of highest *E*-field and Joule heating.

To test initial memory switching, we sourced current and measured voltage across the devices (Fig. 2). The amorphous bits displayed switching at a threshold voltage V_T as is typical with GST (*7, 8*), and a sharp transformation to a conductive

phase under high *E*-field. Importantly, we note that little voltage is dropped across the CNT electrodes, which are always more conductive than the GST bit, as confirmed with finite-element (FE) simulations [see the online supplement (*19*)]. Transport in the a-GST material is temperature-activated (*23*) even in the ~10 nm thin films, as shown in the right inset of Fig. 2A and discussed in (*19*). Once threshold switching occurs, the bit crystallizes from Joule heating and this marks the SET transition. The SET current was of the order ~1 μA in more than 100 devices tested (*19*), two orders of magnitude lower than SET currents in conventional PCM. However, the threshold voltage V_T scaled linearly with the nanogap size (see below). This linear relationship provides strong evidence that threshold switching in a-GST is driven by *E*-field (*24, 25*) even at the minimal bit sizes explored here.

We examined reversible switching of our devices through pulsed measurements. In Fig. 3A, we plot the resistance after a series pulses with the same duration (150 ns) and increasing amplitude, starting from the resistive OFF state. The resistance decreases abruptly when the current exceeds ~1 μA, marking the SET transition. As in Fig. 2, this signals the transformation of GST in the nanogap to the c-phase, effectively 'reconnecting' the two CNT electrodes. The resistance increases again when the current exceeds ~5 μA, which is the RESET transition. This behavior is consistent with fast melting and quenching of the bit (*7*), returning the material to the a-GST phase. Repeated cell switching (Fig. 3B) exhibited good stability after several hundred cycles in devices encapsulated by SiO_2, as described above.

The dimensions of the bits examined here are in general defined by the small nanogaps (down to ~20 nm), the thin (~10 nm) GST film, and the CNT electrode diameters (~1-6 nm). The low thermal conductivity of GST (*19*) appears to play a role in laterally confining the bit to a scale not much greater than the CNT diameter. The small lateral extent of the bits can be seen in Fig. 2C and fig. S6 (*19*), also confirmed with FE simulations in fig. S4 (*19*). We estimate the effective bit volumes addressed here are as small as a few hundred cubic nanometers.

We present a statistical study of more than 100 devices in Fig. 4. First, we plot R_{ON} and R_{OFF} vs. their respective threshold voltage V_T in Fig. 4A, showing two distinct memory states for every device studied. During fabrication, 61 of the CNT nanogaps were created in air and 44 were created under Ar flow, the latter with smaller gaps due to reduced oxygen (*15, 19, 20*). We note R_{OFF} values are fairly constant (*22*). However, R_{ON} scales proportionally with V_T as seen in Fig. 4A, because both R_{ON} and V_T are related to the nanogap size. R_{ON} is dominated by the resistance of the c-GST and proportional to the nanogap size, as the CNT electrodes are much more conductive. The nanogap size also determines V_T, because threshold switching in a-GST is driven by the *E*-field in the nanogap. The linear scaling trend between V_T and nanogap size in Fig. 4B supports this observation, with an average threshold field of ~100 V/μm. This value is comparable to ~56 V/μm threshold field measured in 30-nm GST films (*26*) and an order of magnitude lower than the breakdown field of SiO_2 (*27*), indicating the switching indeed occurs in the GST bit. The mean SET currents across all nanogaps fabricated in air and Ar were nearly identical at ~2 μA, with a range of 0.5 to 4 μA [Fig. S7C (*19*)]. RESET currents were typically four times higher, ranging from 5 to 8.5 μA as shown in Fig. 3 and Fig. S7D (*19*).

We comment on the ultimate scaling limits of such materials and technology. For our 'best' results, switching occurred at <1 μA (SET), ~5 μA (RESET), and ~3 V across 20-30 nm nanogaps, with only a few microwatts of programming power. The programming current and power are two orders of magnitude lower than present state-of-the-art (*12-14*), enabled by the very small volume of PCM addressed with a single CNT. The minimum energy per bit obtained with our sharpest (~20 ns) pulses is of the order ~100 femtojoules. However, the linear trend of V_T with nanogap size (Fig. 4B) reveals such devices are highly scalable, and suggests that ~5 nm GST bits with CNT electrodes could operate at ~0.5 V and <1 μA, such that nanosecond switching times (*28, 29*) would lead to sub-femtojoule per bit energy consumption [for additional estimates see Section 6 of online supplement (*19*)]. Low-voltage operation could also be achieved by using materials with lower threshold fields, such as GeSb (*26*). These results are encouraging for ultra-low power electronics and memory based on programmable PCM with nanoscale carbon interconnects. (*30*)

References and Notes

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Supporting Online Material

www.sciencemag.org/cgi/content/full/science.1201938/DC1
Materials and Methods
SOM Text
Figs. S1 to S9
References

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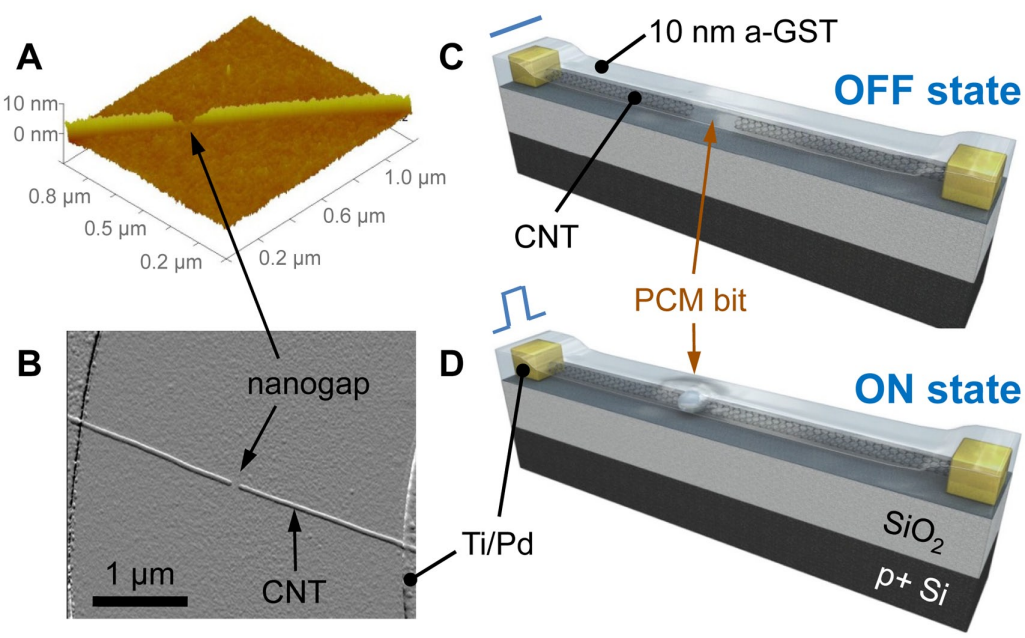
Fig. 1. Schematics of CNT-PCM device. (**A**) Atomic force microscope (AFM) imaging of nanogap created after CNT breakdown under electrical stress. (**B**) AFM image of an as-fabricated device. (**C,D**) Schematic of device obtained after deposition of GST thin film. The device is in its OFF state immediately after fabrication, with highly resistive a-GST in the nanogap. (**D**) The device is switched to its ON state after an electric field in the nanogap transforms the bit to its conductive c-GST phase.

Fig. 2. Initial antifuse-like switching. (**A**) Current vs. voltage of a device with CNT diameter ~3 nm, nanogap ~35 nm, and GST film thickness ~10 nm. The initial sweep (#1) turns the bit ON (a→c) at ~1 μA and V_T = 3.5 V. The c-GST bit phase is subsequently preserved (#2). The left inset shows the *I-V* of the CNT as used to create the nanogap before GST deposition (*20*). The right inset shows temperature-activated transport in the subthreshold regime after a-GST deposition [also see Fig. S9 (*19*)]. The activation energy ~0.38 eV decreases slightly with voltage, consistent with trap-assisted transport in disordered a-GST (*23*). (**B**) and (**C**) show AFM images of the same device before and after switching. Small changes of GST volume in the gap can be seen after switching here without a capping layer (*18*). Also see Fig. S6 in (*19*).

Fig. 3. Reversible memory operation using pulsed measurements. **(A)** Device resistance vs. current pulse magnitude. The width of the SET and RESET pulses are 150 ns (20 ns falling edge) and 50 ns (2 ns falling edge), respectively, as limited by our experimental setup. Sharp transitions are seen at 1 μA (SET) and 5 μA (RESET) current, two orders of magnitude lower than present state-of-the-art (*9-14*). (**B**) Memory endurance test showing excellent separation between ON and OFF state, with no degradation after hundreds of cycles (SET: 1.5 μA, 150 ns; RESET: 6.0 μA, 50 ns). The device shown here is covered by the ~5 nm SiO_2 encapsulation layer.

Fig. 4. Scaling trends of memory devices. (**A**) ON- and OFF-state resistance for 105 devices shown vs. threshold voltage V_T. As marked, 61 nanogaps were created in air ambient (empty symbols), the other 44 devices were formed under Ar flow (solid symbols). Ar-formed nanogaps are consistently smaller (<100 nm) and yield lower-power devices. Dashed lines are trends to guide the eye. **(B)** Threshold voltages scale proportionally to size of nanogap, at an average field of ~100 V/μm. The dashed line is a linear fit, indicating excellent device scalability. Lateral error bar is estimated uncertainty from nanogap measurement under AFM.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0.5 µm
0.2 µm
0.2 µm
0.6 µm
1.0 µm
B
nanogap
1 µm
CNT
C
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OFF state
CNT
PCM bit
D
ON state
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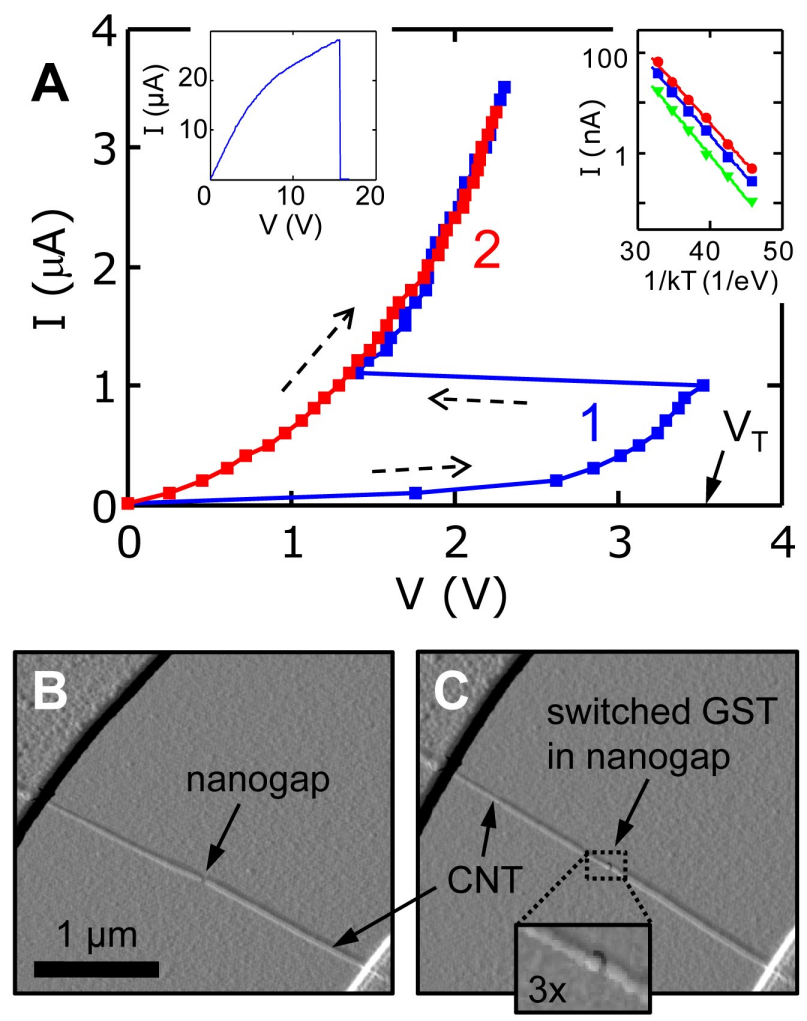
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V_T
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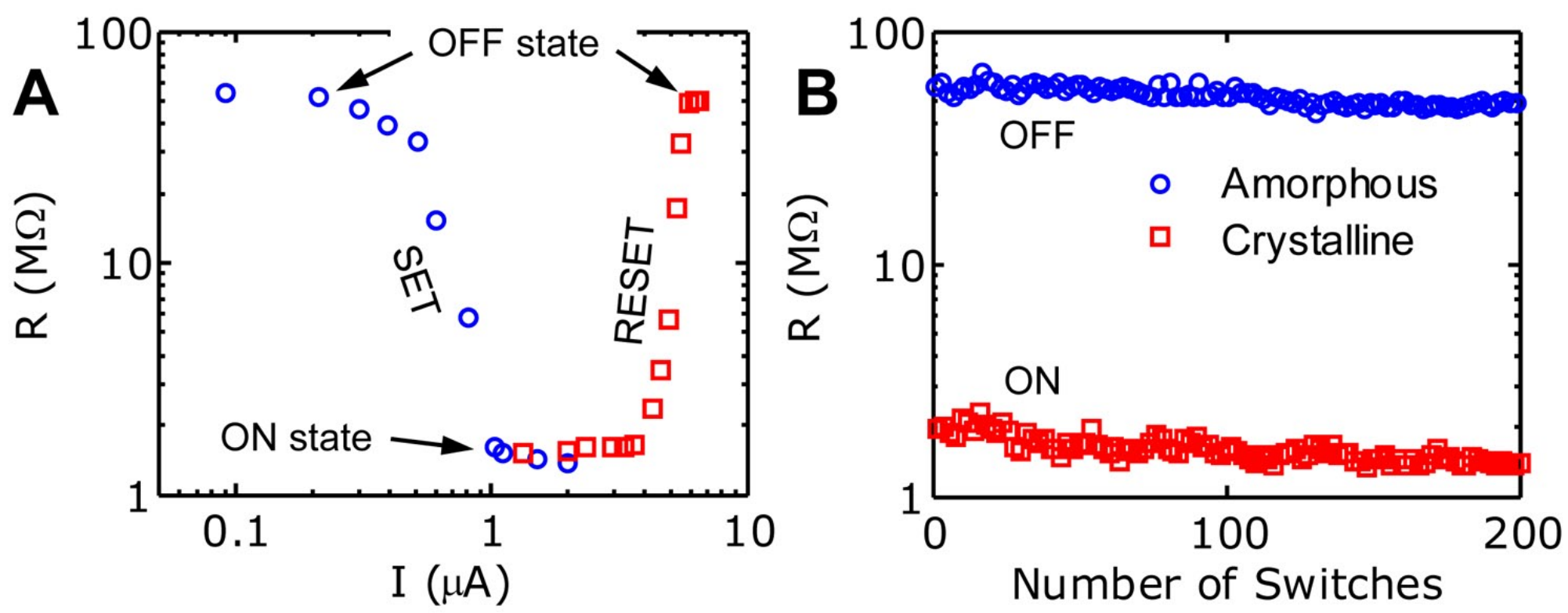
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RESET
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Crystalline
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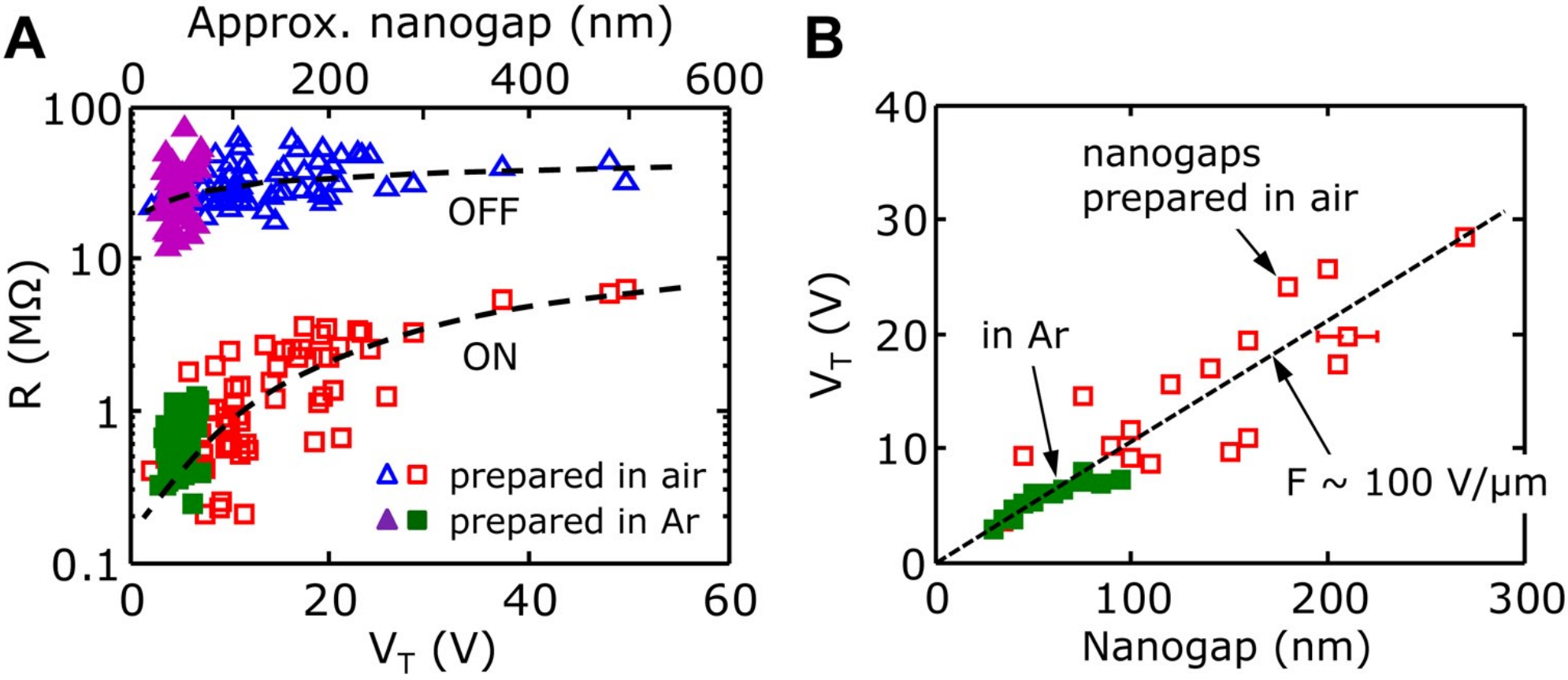
Number of Switches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prepared in Ar
0
20
40
60
V_T (V)
B
40
30
20
10
0
V_T (V)
nanogaps
prepared in air
in Ar
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0
100
200
300
Nanogap (nm)