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Low-Power Switching of Phase-Change Materials with Carbon Nanotube Electrodes

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Phase-change materials (PCMs) are promising candidates for nonvolatile data storage and reconfigurable electronics, but high programming currents have presented a challenge to realize low power operation. We controlled PCM bits with single-wall and small-diameter multi-wall carbon nanotubes. This configuration achieves programming currents as low as 0.5 μA (SET) and 5 μA (RESET), two orders of magnitude lower than state-of-the-art devices. Pulsed measurements enable memory switching with very low energy consumption. Analysis of over one hundred devices finds that the programming voltage and energy are highly scalable, and could be below 1 V and single femtojoules per bit, respectively.

Phase-change materials (PCMs) are typically chalcogenides like $Ge_2Sb_2Te_5$ (GST) which have amorphous (a) and crystalline (c) phases with contrasting electrical and optical properties. PCMs are the active material in rewritable DVDs, where phase transformations are induced and read by a pulsed laser (*1, 2*). The data in electrically-programmable PCMs are stored as changes in bit resistivity (*3-6*), which can be reversibly switched with short voltage pulses and localized Joule heating. In this sense, PCMs are appealing vs. other semiconductor memories where data are stored as charge and are susceptible to leakage and volatile behavior. Electrically-programmable PCMs have captivated wide interest for applications in non-volatile memory (*7, 8*) and reprogrammable circuits (*5, 6*) with low voltage operation, fast access times, and high endurance (*3, 4*). These attributes make them contenders for a 'universal' non-volatile memory, which could replace all data storage from random-access memory to hard disks. However, a drawback of PCMs is their high programming current (>0.1 mA), as Joule heat must be coupled to a finite bit volume, previously achieved with 30 to 100-nm diameter nanowires (*9-11*) or metal vias (*12-14*).

We used carbon nanotubes (CNTs) with diameters ~1 to 6 nm as electrodes (*15, 16*) to reversibly induce phase change in nanoscale GST bits. Our findings address the potential size and power reduction that are possible for programmable bits of PCM. We demonstrate reversible switching with programming currents from 1 to 8 μA, two orders of magnitude lower than state-of-the-art PCM devices. We also present a device scaling study that suggests memory switching is possible with voltages below 1 V and energy less than femtojoules per bit.

The CNTs used in this work were grown by chemical vapor deposition (CVD) with Fe catalyst particles on SiO_2/Si substrates (*17, 18*) [also see online supplement (*19*)]. We obtained single-wall and small diameter multi-wall CNTs, and we found that both can be used to switch GST bits. The as-grown CNTs span Ti/Pd (0.5/40 nm) metal contacts with 1 to 5 μm separation (fig. S1 (*19*)). We then created nanoscale gaps in the CNTs through electrical breakdown (*20*) in air or under Ar flow, as illustrated in Fig. 1 and the left inset to Fig. 2A. This simple approach yielded a wide range of nanogaps (from ~20-300 nm) in more than 100 devices, which was essential for our subsequent scaling study. The nanogap is typically near the middle of the CNT, consistent with the electrical breakdown location and with negligible Pd contact resistance (*20, 21*). Then, a ~10-nm GST film was sputtered over the device surface (fig. S2 (*19*)), with settings previously found to preserve the electrical characteristics of CNTs (*18*). This deposition fills the CNT nanogaps, creating self-aligned lateral PCM bits. Such devices can be readily switched and examined by atomic force microscopy (AFM) (Fig. 2); however, a ~5-nm SiO_2 layer deposited after the GST without breaking vacuum (*12*) must be used to prolong the switching lifetimes.

Devices are initially in the OFF state (Fig. 1C) because the as-deposited GST films are amorphous (a-GST) and highly resistive, R_{OFF} ~ 50 MΩ (*22*). A voltage applied at the CNT contacts creates a sizeable electric field (*E*-field) across the nanogap, and switches the GST bit to the crystalline phase (c-GST), which lowers the resistance by about two orders of magnitude, to R_{ON} ~ 0.5 MΩ. Although a-GST covers the entire device, the switching occurs only in the nanogap, which is the location of highest *E*-field and Joule heating.

To test initial memory switching, we sourced current and measured voltage across the devices (Fig. 2). The amorphous bits displayed switching at a threshold voltage V_T as is typical with GST (*7, 8*), and a sharp transformation to a conductive

phase under high *E*-field. Importantly, we note that little voltage is dropped across the CNT electrodes, which are always more conductive than the GST bit, as confirmed with finite-element (FE) simulations [see the online supplement (*19*)]. Transport in the a-GST material is temperature-activated (*23*) even in the ~10 nm thin films, as shown in the right inset of Fig. 2A and discussed in (*19*). Once threshold switching occurs, the bit crystallizes from Joule heating and this marks the SET transition. The SET current was of the order ~1 μA in more than 100 devices tested (*19*), two orders of magnitude lower than SET currents in conventional PCM. However, the threshold voltage V_T scaled linearly with the nanogap size (see below). This linear relationship provides strong evidence that threshold switching in a-GST is driven by *E*-field (*24, 25*) even at the minimal bit sizes explored here.

We examined reversible switching of our devices through pulsed measurements. In Fig. 3A, we plot the resistance after a series pulses with the same duration (150 ns) and increasing amplitude, starting from the resistive OFF state. The resistance decreases abruptly when the current exceeds ~1 μA, marking the SET transition. As in Fig. 2, this signals the transformation of GST in the nanogap to the c-phase, effectively 'reconnecting' the two CNT electrodes. The resistance increases again when the current exceeds ~5 μA, which is the RESET transition. This behavior is consistent with fast melting and quenching of the bit (*7*), returning the material to the a-GST phase. Repeated cell switching (Fig. 3B) exhibited good stability after several hundred cycles in devices encapsulated by SiO_2, as described above.

The dimensions of the bits examined here are in general defined by the small nanogaps (down to ~20 nm), the thin (~10 nm) GST film, and the CNT electrode diameters (~1-6 nm). The low thermal conductivity of GST (*19*) appears to play a role in laterally confining the bit to a scale not much greater than the CNT diameter. The small lateral extent of the bits can be seen in Fig. 2C and fig. S6 (*19*), also confirmed with FE simulations in fig. S4 (*19*). We estimate the effective bit volumes addressed here are as small as a few hundred cubic nanometers.

We present a statistical study of more than 100 devices in Fig. 4. First, we plot R_{ON} and R_{OFF} vs. their respective threshold voltage V_T in Fig. 4A, showing two distinct memory states for every device studied. During fabrication, 61 of the CNT nanogaps were created in air and 44 were created under Ar flow, the latter with smaller gaps due to reduced oxygen (*15, 19, 20*). We note R_{OFF} values are fairly constant (*22*). However, R_{ON} scales proportionally with V_T as seen in Fig. 4A, because both R_{ON} and V_T are related to the nanogap size. R_{ON} is dominated by the resistance of the c-GST and proportional to the nanogap size, as the CNT electrodes are much more conductive. The nanogap size also determines V_T, because threshold switching in a-GST is driven by the *E*-field in the nanogap. The linear scaling trend between V_T and nanogap size in Fig. 4B supports this observation, with an average threshold field of ~100 V/μm. This value is comparable to ~56 V/μm threshold field measured in 30-nm GST films (*26*) and an order of magnitude lower than the breakdown field of SiO_2 (*27*), indicating the switching indeed occurs in the GST bit. The mean SET currents across all nanogaps fabricated in air and Ar were nearly identical at ~2 μA, with a range of 0.5 to 4 μA [Fig. S7C (*19*)]. RESET currents were typically four times higher, ranging from 5 to 8.5 μA as shown in Fig. 3 and Fig. S7D (*19*).

We comment on the ultimate scaling limits of such materials and technology. For our 'best' results, switching occurred at <1 μA (SET), ~5 μA (RESET), and ~3 V across 20-30 nm nanogaps, with only a few microwatts of programming power. The programming current and power are two orders of magnitude lower than present state-of-the-art (*12-14*), enabled by the very small volume of PCM addressed with a single CNT. The minimum energy per bit obtained with our sharpest (~20 ns) pulses is of the order ~100 femtojoules. However, the linear trend of V_T with nanogap size (Fig. 4B) reveals such devices are highly scalable, and suggests that ~5 nm GST bits with CNT electrodes could operate at ~0.5 V and <1 μA, such that nanosecond switching times (*28, 29*) would lead to sub-femtojoule per bit energy consumption [for additional estimates see Section 6 of online supplement (*19*)]. Low-voltage operation could also be achieved by using materials with lower threshold fields, such as GeSb (*26*). These results are encouraging for ultra-low power electronics and memory based on programmable PCM with nanoscale carbon interconnects. (*30*)

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Supporting Online Material

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Materials and Methods
SOM Text
Figs. S1 to S9
References

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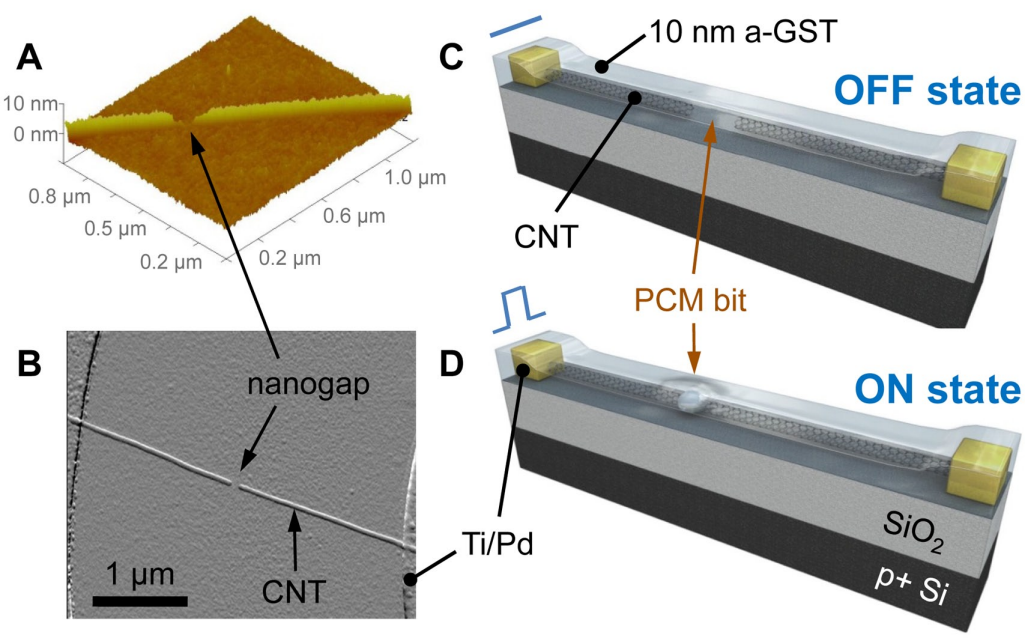
Fig. 1. Schematics of CNT-PCM device. (**A**) Atomic force microscope (AFM) imaging of nanogap created after CNT breakdown under electrical stress. (**B**) AFM image of an as-fabricated device. (**C,D**) Schematic of device obtained after deposition of GST thin film. The device is in its OFF state immediately after fabrication, with highly resistive a-GST in the nanogap. (**D**) The device is switched to its ON state after an electric field in the nanogap transforms the bit to its conductive c-GST phase.

Fig. 2. Initial antifuse-like switching. (**A**) Current vs. voltage of a device with CNT diameter ~3 nm, nanogap ~35 nm, and GST film thickness ~10 nm. The initial sweep (#1) turns the bit ON (a→c) at ~1 μA and V_T = 3.5 V. The c-GST bit phase is subsequently preserved (#2). The left inset shows the *I-V* of the CNT as used to create the nanogap before GST deposition (*20*). The right inset shows temperature-activated transport in the subthreshold regime after a-GST deposition [also see Fig. S9 (*19*)]. The activation energy ~0.38 eV decreases slightly with voltage, consistent with trap-assisted transport in disordered a-GST (*23*). (**B**) and (**C**) show AFM images of the same device before and after switching. Small changes of GST volume in the gap can be seen after switching here without a capping layer (*18*). Also see Fig. S6 in (*19*).

Fig. 3. Reversible memory operation using pulsed measurements. **(A)** Device resistance vs. current pulse magnitude. The width of the SET and RESET pulses are 150 ns (20 ns falling edge) and 50 ns (2 ns falling edge), respectively, as limited by our experimental setup. Sharp transitions are seen at 1 μA (SET) and 5 μA (RESET) current, two orders of magnitude lower than present state-of-the-art (*9-14*). (**B**) Memory endurance test showing excellent separation between ON and OFF state, with no degradation after hundreds of cycles (SET: 1.5 μA, 150 ns; RESET: 6.0 μA, 50 ns). The device shown here is covered by the ~5 nm SiO_2 encapsulation layer.

Fig. 4. Scaling trends of memory devices. (**A**) ON- and OFF-state resistance for 105 devices shown vs. threshold voltage V_T. As marked, 61 nanogaps were created in air ambient (empty symbols), the other 44 devices were formed under Ar flow (solid symbols). Ar-formed nanogaps are consistently smaller (<100 nm) and yield lower-power devices. Dashed lines are trends to guide the eye. **(B)** Threshold voltages scale proportionally to size of nanogap, at an average field of ~100 V/μm. The dashed line is a linear fit, indicating excellent device scalability. Lateral error bar is estimated uncertainty from nanogap measurement under AFM.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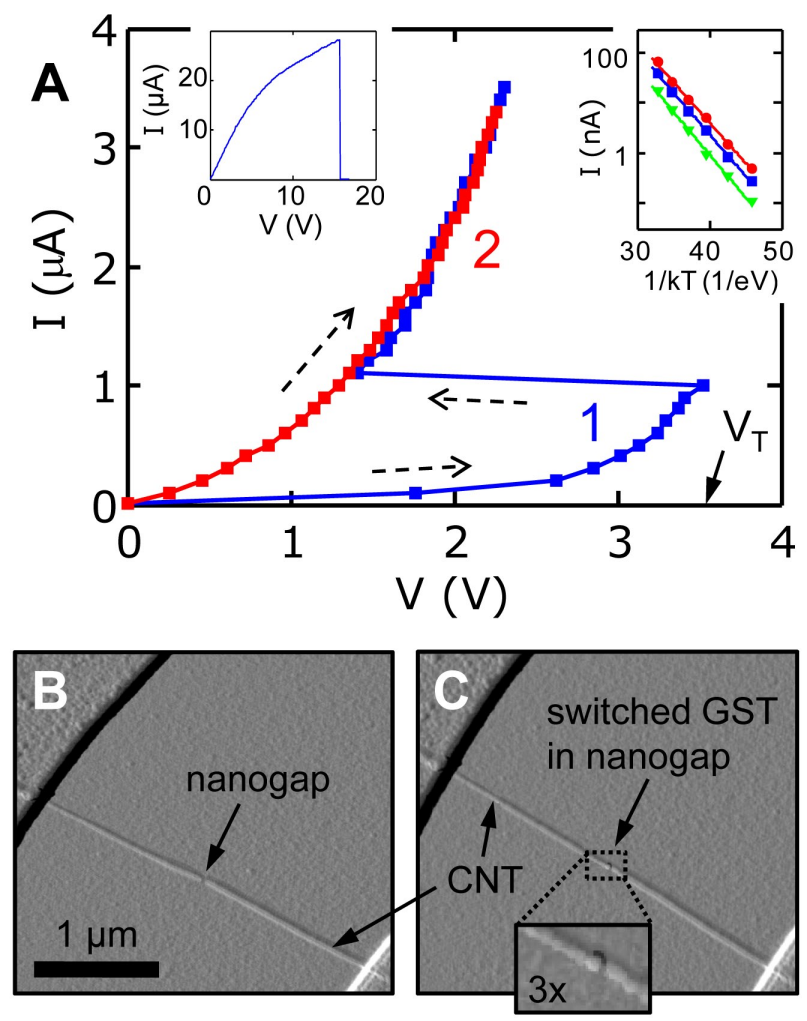
10 nm
0 nm
0.8 µm
0.5 µm
0.2 µm
0.2 µm
0.6 µm
1.0 µm
B
nanogap
1 µm
CNT
C
10 nm a-GST
OFF state
CNT
PCM bit
D
ON state
Ti/Pd
SiO2
p+ Si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V (V)
V_T
1
2
I (μA)
V (V)
I (nA)
1/kT (1/eV)
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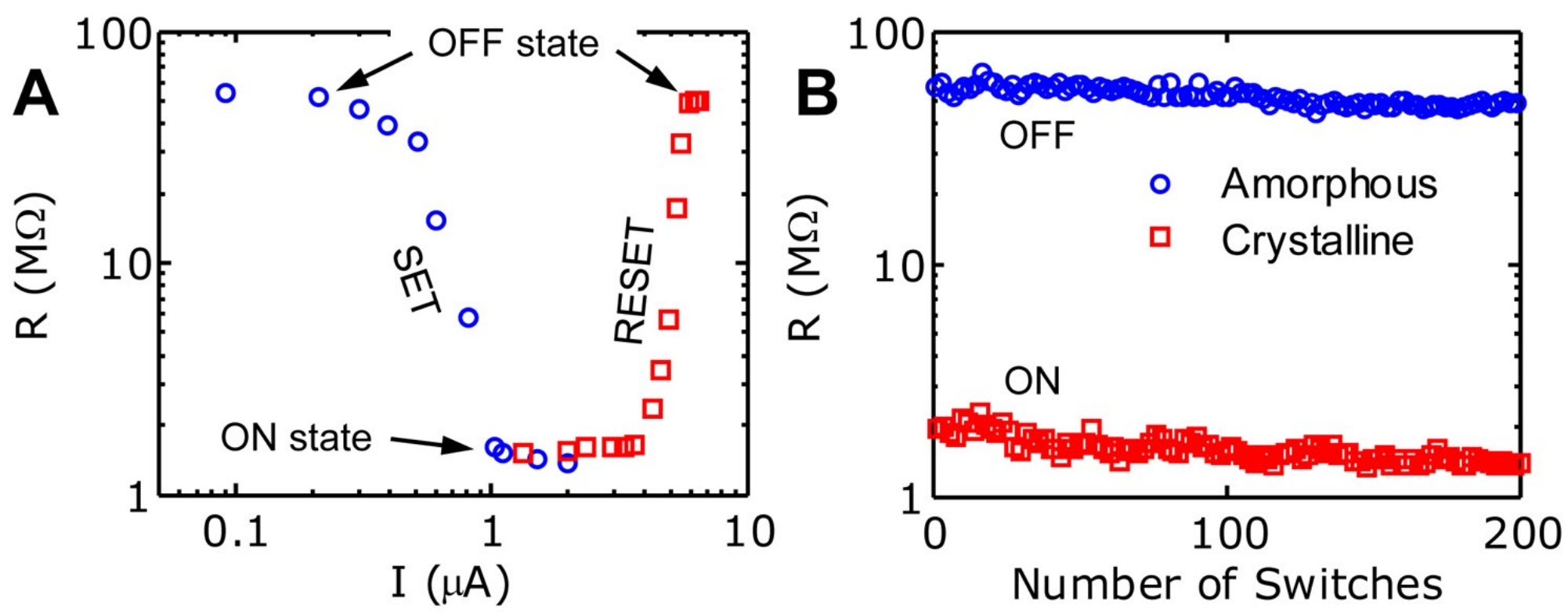
nanogap
1 μm
C
switched GST
in nanogap
CNT
3x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10
1
R (MΩ)
OFF state
SET
RESET
ON state
0.1
1
10
I (μA)
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1
R (MΩ)
OFF
Amorphous
Crystalline
ON
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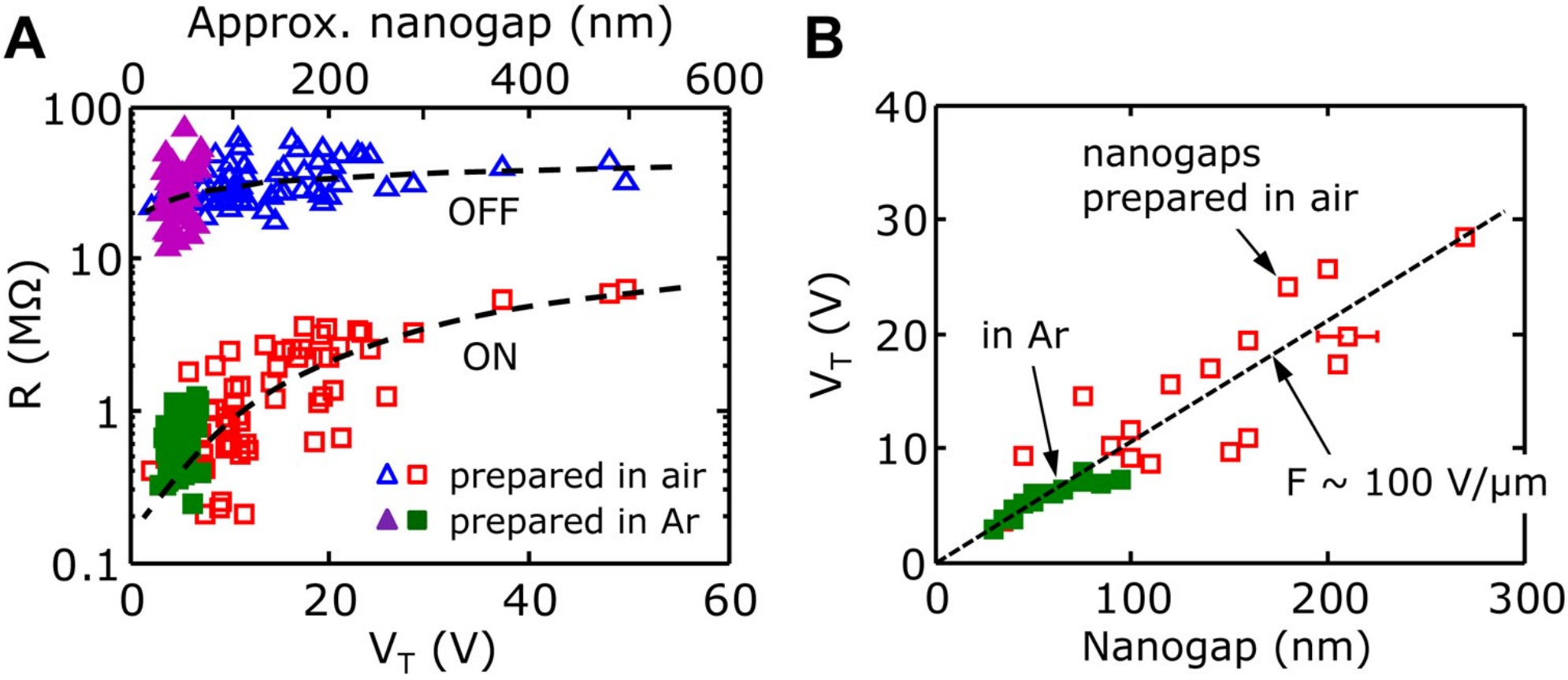
100
200
Number of Switches


A
Approx. nanogap (nm)
0
200
400
600
100
10
1
0.1
R (MΩ)
OFF
ON
prepared in air
prepared in Ar
0
20
40
60
V_T (V)
B
40
30
20
10
0
V_T (V)
nanogaps
prepared in air
in Ar
F ~ 100 V/μm
0
100
200
300
Nanogap (nm)

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Supporting Online Material for

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Low Power Switching of Phase Change Materials with Carbon Nanotube Electrodes

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Supporting Online Materials (SOM) Content:

1. **Methods of CNT Device Fabrication**
2. **GST Thin Film Deposition & Characterization**
3. **Three-Dimensional Finite Element Modeling**
4. **Additional Electrical and AFM Measurements**
5. **Comparison of CNT Nanogap Formation in Air and Ar Flow**
6. **Device Scaling Estimates**
7. **Comparison with Critical Nucleus Size in GST**
8. **Subthreshold Measurements of Ultra-Thin GST**
9. **Supplementary References**

1. Methods of CNT Device Fabrication

Carbon nanotubes (CNTs) were grown by chemical vapor deposition (CVD) using a mixture of CH_4 and C_2H_4 as the carbon feedstock, and H_2 as the carrier gas at 900 ^oC. The flow rate of CH_4 to C_2H_4 was kept large to grow predominantly single-walled CNTs. Fe (~2 Å thick deposited by e-beam evaporation) is used as the catalyst for CNT growth. The catalyst was deposited on ~70 nm thick SiO_2 and highly p-doped Si wafers. Patterned catalyst islands are formed using photolithography and lift-off. Prior to growth, the catalyst was annealed at 900 ^oC in Ar environment to ensure the formation of Fe nanoparticles, from which the CNTs grow. The nanotubes were contacted with Ti/Pd (1/40 nm) electrodes defined using photolithography. The electrode separation on our test chips is varied from L ~ 1-5 μm, although the exact CNT length is not essential for low-power GST switching, with the CNTs being much more conductive than GST.

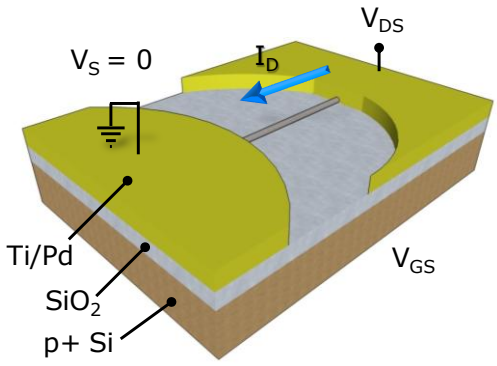

Fig. S1. *The schematics of the initial CNT devices that are used in this work, before nanogap formation. Semi-circular electrodes are used for tighter control of CNT length (1-3).*

2. GST Thin Film Deposition & Characterization

GST thin film deposition is done in high vacuum using an ATC 2000 custom four gun co-sputtering system (AJA International), with a deposition rate at 0.4 Å/s at 12 W DC power. Deposition at this rate ensures that there is only minimal damage to the CNT from the sputtering process (*3*). The sputtering target $Ge_2Sb_2Te_5$ was purchased from ACI Alloys Incorporated. Thin film thickness is characterized with X-ray reflectivity measurement using Philips Xpert Pro XRD system on control samples. By probing diffraction intensities at glancing angles of incidence, we are able to confirm the GST thin film thickness is 10.0 ± 0.4 nm (Fig. S2A).

We have also performed atomic force microscopy (AFM) measurements on our samples before and after GST deposition (Fig. S1B and S1C, respectively). The measured RMS surface roughness of our devices only increased minimally from ~0.3 nm to ~0.5 nm (*3*).

3. Three-Dimensional Finite Element Modeling

We have developed a comprehensive 3D finite element (FE) model accounting for the electro-thermal interactions in our devices using COMSOL Multiphysics. In the simulation, an electrical model is used to predict the voltage and current distribution in the device; while a thermal model is employed to predict the temperature distribution. The two are coupled via Joule heating and the temperature dependence of material properties. The modeling schematic for the CNT-PCM device is consistent with the actual device structure and is shown in Fig. S3A.

In the electrical model, the Poisson and continuity equations are solved to obtain the voltage and current distribution in the device: $\nabla\cdot[\sigma(x,y,z,t)\nabla V] = 0$. The electrical conductivity of GST, σ_{GST}, depends on its phase, temperature and in the case of amorphous GST (a-GST), the electric

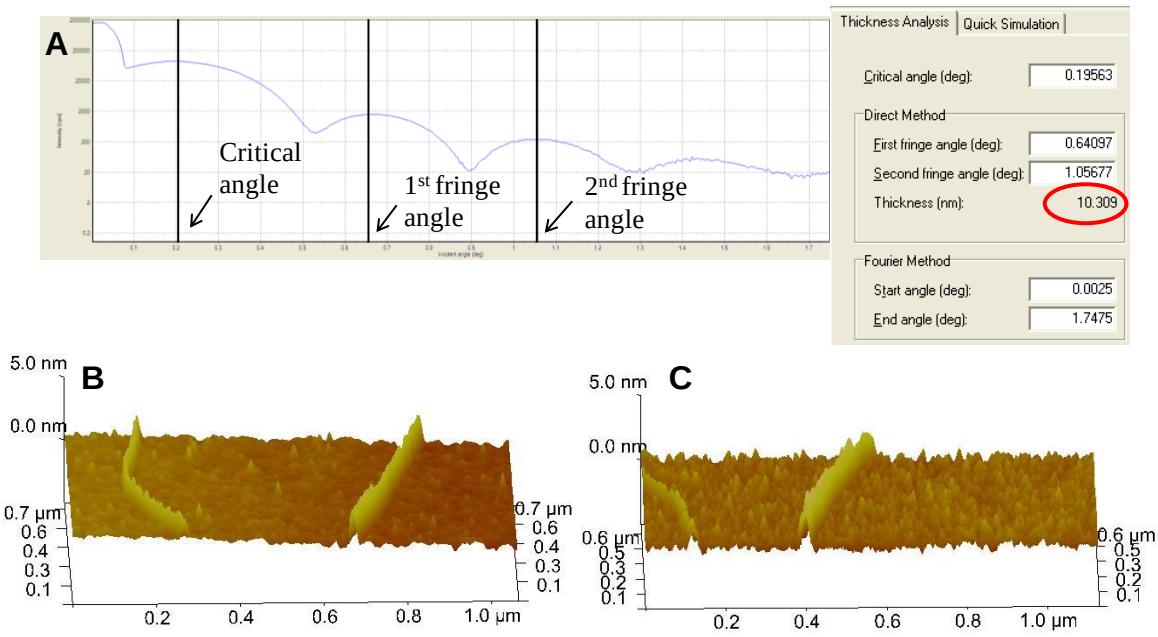

Fig. S2. (A) *X-ray reflectivity measurement of sputtered GST thin film using control samples. The control sample is fabricated by sputtering GST directly onto highly doped Si substrate immediately after the removal of the the native oxide layer by wet etching. The measurement confirms the GST thin film thickness is 10 nm.* ***(B)*** *and* ***(C)*** *AFM images of CNTs before and after GST deposition, indicating the GST thin film is highly conformal with minimal roughness.*

field, as shown in Fig. S3B. At T > 150 ºC, the a-GST transforms into the face centered cubic (fcc) crystalline phase (c-GST), with a sharp drop in resistivity. When T > 350 ºC, GST transforms into hexagonal closed pack (hcp) phase, with another (smaller) decrease in resistivity. The temperature dependence of GST resistivity (Fig. S3B) is numerically incorporated in our model and based on experimental results from Lankhorst *et al (4)*.

The electrical conductivity of the CNT σ_{CNT} is calculated based on a model developed by Pop *et al* (*5*): $\sigma_{CNT} = (4q^2/h)\cdot(\lambda_{eff}/A)$, where q is the elementary charge, h is Planck's constant, λ_{eff} is the effective carrier mean free path, and $A = \pi db$ is the cross-sectional area of the CNT, where d and b (~0.34 nm) are the diameter and wall thickness of the nanotube respectively. The nanotube conductivity is temperature and position dependent through the effective mean free path λ_{eff}, which can be calculated using the Matthiessen's rule as: $\lambda_{eff}^{-1} = \lambda_{AC}^{-1} + \lambda_{OP,ems}^{-1} + \lambda_{OP,abs}^{-1}$.

On all external boundaries, electrically insulating boundary conditions are applied, except across the electrodes, where a constant current flow is assumed. Electrical contact resistance is simulated on interior boundaries between GST/electrodes (~ 150 kΩ), CNT/electrodes (~ 50 kΩ) and GST/CNT (~100 kΩ).

In the thermal model, the transient heat equation is used to obtain the temperature and GST phase in the device: $\nabla\cdot[k(x,y,z,t)\nabla T] + Q = C_v(\partial T/\partial t)$, where k is the thermal conductivity, T is the temperature, $Q = I^2R$ is the Joule heat generation and C_v is the volumetric heat capacity. The thermal conductivity of GST (k_{GST}) depends both on temperature and phase (Fig. S3C) as described by Lyeo *et al* (*6*). Table 1 summarizes the main material properties used in this work.

Adiabatic thermal boundary conditions are used on all exterior boundaries except the bottom of the SiO_2, where a constant T = 293 K is assumed (convective cooling by air and radiation loss are insignificant). At interior boundaries, thermal boundary resistance (TBR) is applied to model the heat fluxes and temperature gradients at the interfaces. The TBR is modeled by adding a very thin thermally resistive layer at all relevant interfaces, with thickness d_{th} and thermal conductivity k_{th} such that the TBR $R_{th} = d_{th}/k_{th}$. The Pd/CNT boundary is assumed to have a TBR $R_{th} = 1.2 \times 10^7$ K/W (*7*); while a thermal conductance g = 0.17 $WK^{-1}m^{-1}$ per CNT length is applied at the CNT/SiO_2 boundary (*5*). All other interior boundaries have $R_{th} = 2.5 \times 10^{-8}$ m^2KW^{-1} which is typical for many systems (*8*).

Table 1. Material properties used in simulation.

	k (W/m/K)	C ($J/m^3/K$)	σ (S/m)
Pd (electrode)	22	2.93×10^6	1×10^7
SiO_2	1.4	1.72×10^6	1×10^{-16}
GST	$k_{GST}(T)$ as in Fig. S3	1.24×10^6	$\sigma_{GST}(T)$ as in Fig. S3
CNT	3000	1.10×10^6	$\sigma_{CNT}(T)$ as in Ref. (*5*)

We performed different sets of simulations each with increasing current flow. In each simulation, a constant current pulse was applied for 100 ns. The current-voltage simulation is compared to experimental data for a specific device in Fig. S3D. Blue circles show the experimental results of a CNT-PCM device with 2.0 µm CNT length, 2.5 nm CNT diameter, and 70 nm nanogap size. As explained in the main text, the voltage snapback behavior is caused by threshold switching in GST and followed by a→c phase change due to Joule heating. The FE model correctly captures these characteristics with the standard material parameters.

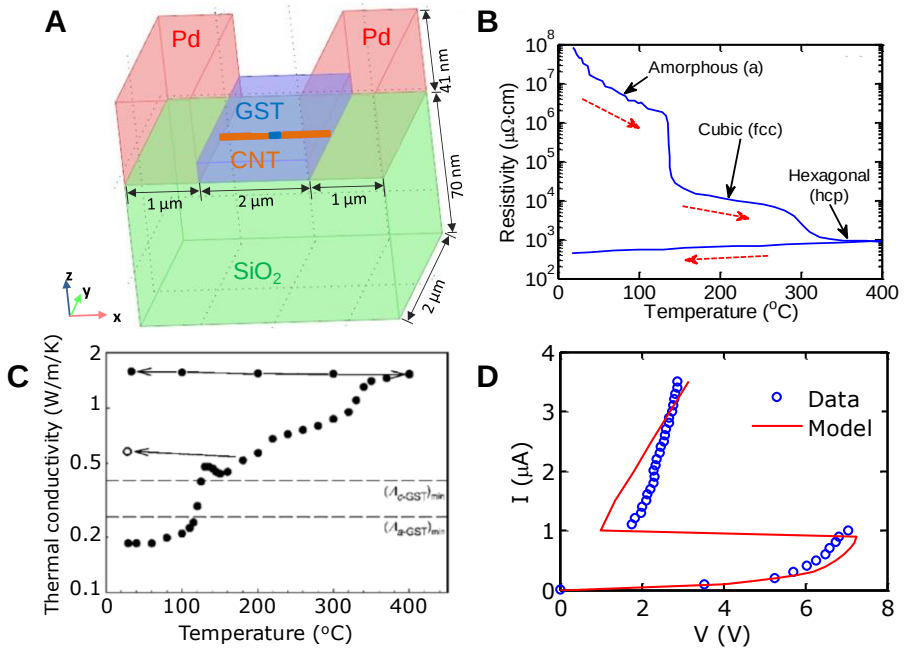

Fig. S3. (A) *Schematic of the 3-dimensional FE model of the CNT-PCM device from COMSOL simulations, closely following the experimental layout (Fig. 1 in main text).* ***(B)*** *Temperature dependence of GST resistivity and* ***(C)*** *thermal conductivity.* ***(D)*** *I-V characteristics (experimental data and simulations) of a nanotube-PCM device. The CNT length = 2.0 µm, diameter = 2.5 nm and nanogap size = 70 nm; GST film is 10 nm thick. The snapback behavior is observed when the localized E-field in the gap exceeds the threshold value.*

The temperature profile of GST in the CNT gap region before and after the threshold switching is illustrated in Fig. S4. In its highly resistive state, the current passing through the CNT-PCM device is on the order of 100 nA. At low voltage the Joule heat generated is insufficient to reach the GST crystallization temperature ~420 K (Fig. S4A). However, once the electric field (E-field) in the nanogap reaches the threshold value, the a-GST in the nanogap switches into a conductive state, and the local current density in the GST nanogap increases drastically. At this point, sufficient heat is generated to raise the temperature to where the GST changes into its stable crystalline phase (c-GST). The bulk GST that is not exposed to high E-field and current flow remains in the highly resistive a-GST phase and therefore does not heat up significantly (Fig. S4, B and C).

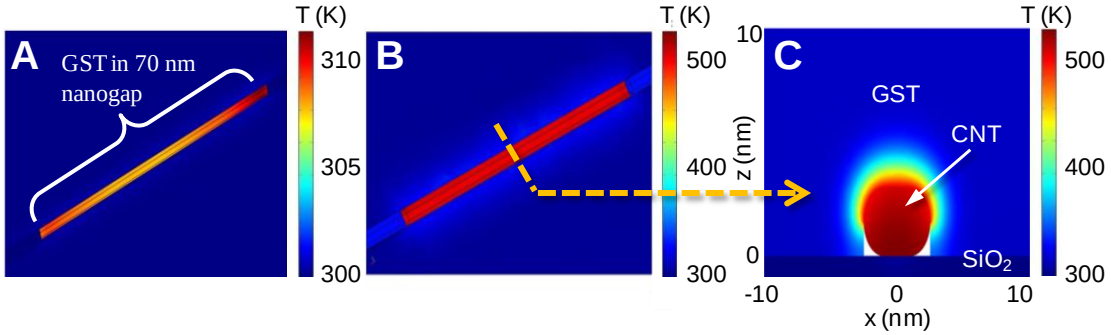

Fig. S4. (A) *Simulated temperature profile of GST in the nanogap before and* ***(B)*** *after it switches into the highly conductive state. Importantly, simulations show that the GST outside the nanogap region remains at relatively low temperature and thus still in the amorphous phase, primarily due to the low thermal conductivity of GST. This is an important feature, which enables the very small bit volume addressed here (few hundred cubic nanometers), and the ultra-low power operation.* ***(C)*** *Cross-sectional temperature profile of the GST in the center of the nanogap, indicating once again the highly confined current flow and heating region.*

4. Additional Electrical & AFM Measurements

Electrical measurements were performed with a Keithley 4200 Semiconductor Characterization System (SCS), a Keithley 3402 Pulse Generator (PG), and an Agilent Infiniium 50004A oscilloscope. The device resistance after applying the SET and RESET pulses is measured with the 4200 SCS at a 2.0 V DC bias. The SET and RESET current magnitudes were calculated from the applied voltage amplitude and the device resistance. Fig. S5 shows a typical waveform.

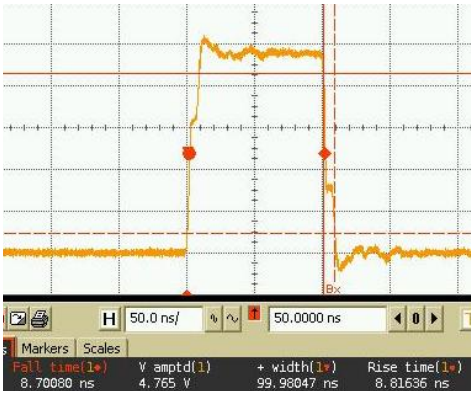

Fig. S5. *A typical RESET pulse waveform.*

Figure S6 below shows additional electrical and AFM measurements of other the nanotube-PCM devices. These are similar to those shown in Fig. 2 in the main text, but for devices with larger nanogap size, and consequently larger threshold voltage V_T. These devices have nanogaps of ~100 nm and ~210 nm, and V_T = 9 V and 19.8 V, respectively, representative of the general scaling trend observed in Fig. 4 of the main text (a→c switching is E-field driven).

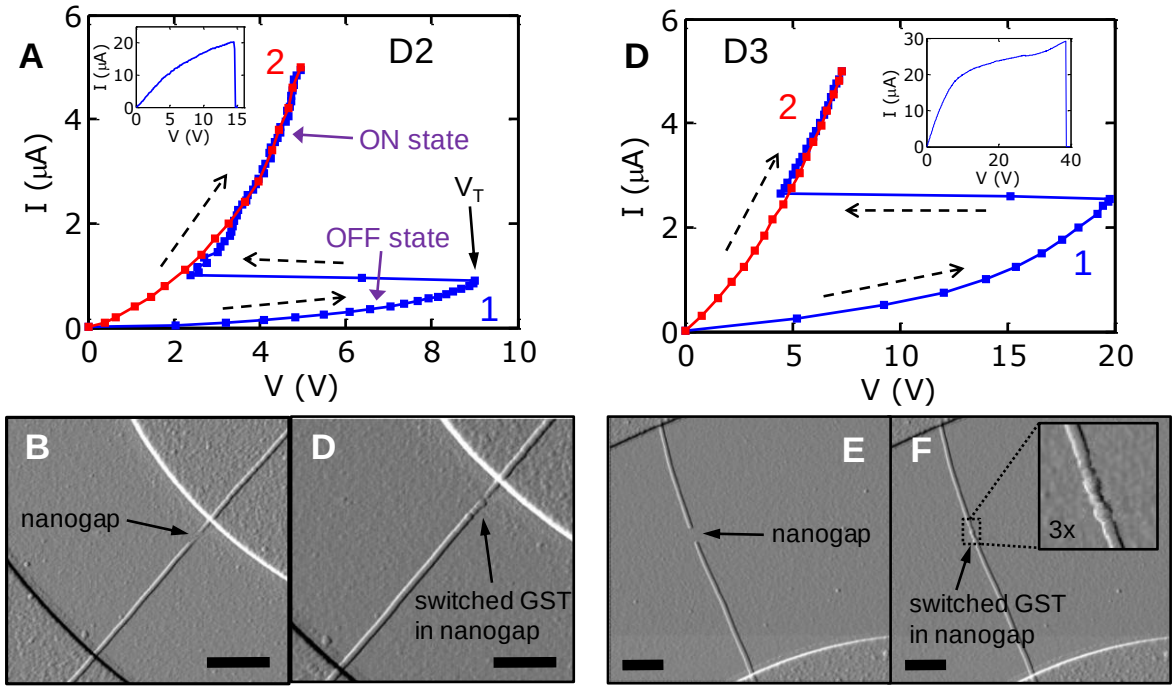

Fig. S6. *Characterization of additional CNT-PCM devices. (**A**) and (**D**) I-V characteristics of two devices before and after SET. Devices have CNT diameter = 2.5 nm (2.1 nm), CNT length = 2.2 μm (3.8 μm) and nanogap size = 100 nm (210 nm). SET currents are 0.9 μA (2.4 μA) and threshold voltages V_T = 9 V (19.8 V). Insets show CNT I-V leading to nanogap formation. (**B**) and (**E**) are AFM images after nanogap formation. **(D)** and **(F)** are AFM images after SET operation. Note the inset shows the narrow (small volume) conductive GST path created, consistent with the simulation from Fig. S4. The scale bars are 0.5 μm. (also see Fig. 2 in main text.)*

5. Comparison of CNT Nanogap Formation in Air and Ar Flow

In order to create the CNT nanogaps, we performed electrical breakdown of CNTs both in ambient air and under Ar flow. We have also 'cut' CNTs with AFM manipulation, but the electrical breakdowns offered a much faster route to obtain a wide range of nanogaps (Fig. 4). Of course, while the CNT breakdown method is extremely useful here, it would not be the preferred route for obtaining nanogaps in a more scalable manufacturing environment. Nevertheless, we believe it is useful to present some observations associated with this technique here.

First, we note that CNT breakdowns 'under Ar flow' were done by flowing Ar (which is heavier than air) from a small nozzle over the entire test chip while probing. Thus, some diminished amount of oxygen was still available for CNT breakdown, unlike the breakdowns performed in vacuum in the second panel of Fig. 2C of Ref. (*1*). There, the CNT break in vacuum could lead to SiO_2 damage, which was not seen here either in ambient air or under Ar flow.

Second, we found that nanogaps formed in Ar are always smaller (always <100 nm) due to the diminished amount of oxygen, as seen in Fig. 4 (main text) and Fig. S7 (below). This is useful because, as mentioned in the main text, CNT-PCM devices with smaller nanogap size operate at lower threshold voltages.

We report additional statistics for all devices measured by AFM in Fig. S7. We find no clear dependence between nanogap size and CNT diameter (Fig. S7A). In a sense, this is encouraging because it suggests that tight control of CNT electrode diameter may not be necessary to make very low power devices. Our simulations (Figs. S3 and S4) also suggest this is the case, because the resistance of the GST bit always dominates that of the CNT (both in the a- and c-GST phase), thus rendering variability in the CNT of less importance. This fact could be important for mass production of such electronics where some amount of CNT variability could be tolerated.

Figure S7B shows the dependence of nanogap size on CNT length, after both air and Ar-flow breakdowns. These data seem to suggest some dependence of nanogap size on CNT length for nanogaps created in ambient air. This was also noted in Ref. (*9*), although at smaller CNT lengths (<1 μm) where the CNT temperature profile would be more steeply varying. On the other hand, for CNTs longer than ~1 μm the temperature profile is relatively flat (*5*). Figure S7C shows the range of SET currents (~0.5 to 4 μA) across all devices tested where diameter data from AFM was also available. Figure S7D compares SET and RESET current for the subset of devices where both these and AFM data were available. The RESET current range is ~5 to 8.5 μA.

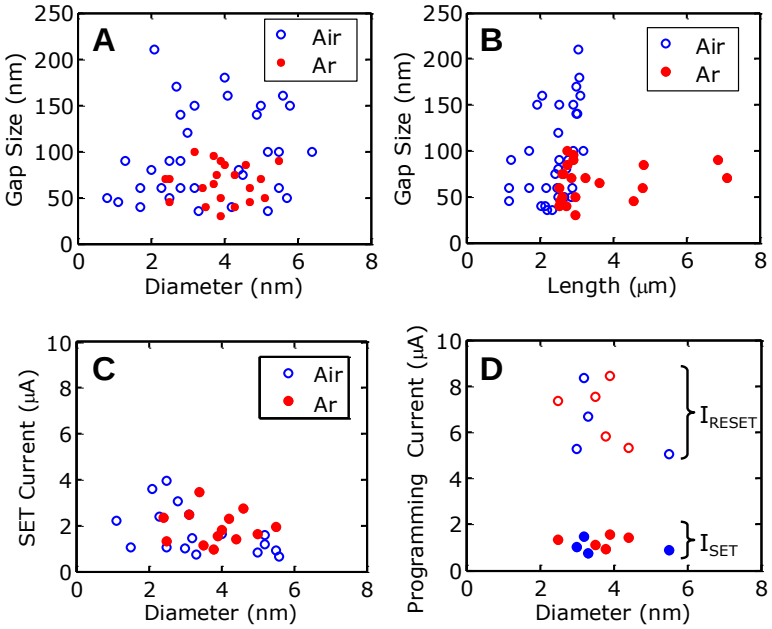

Fig. S7. (A) *CNT nanogap dependence on CNT diameter. Blue circles indicate devices that were broken down ('cut') in air, red solid dots are devices that were prepared under Ar flow.* ***(B)*** *The CNT nanogap size vs. original CNT length. For both devices that were broken down in air and under Ar flow, we observe that CNTs with smaller length tends to have smaller gap size.* ***(C)*** *SET current vs. CNT diameter. No clear trend is observed.* ***(D)*** *SET and RESET current vs. CNT diameter for the same devices.*

6. Device Scaling Estimates

Our 'best' devices in this study have 20-30 nm nanogaps with threshold voltages below 3 V, SET currents below 1 μA, and RESET currents ~5 μA. This corresponds to programming power below 3 μW (2.6 μW for 'best case'), significantly lower than the nearly ~1 mW programming power in conventional PCM devices. We are achieving such record-low power because of the extremely low effective bit volumes (hundreds of cubic nanometers) that can be addressed with CNT electrodes of few-nanometer diameters. Moreover, the scaling trend in Fig. 4B indicates

such devices are highly scalable, and even lower (perhaps by another ~10×) switching power may be possible.

To understand these limits, we theoretically consider 5 nm nanogaps between CNT electrodes, which should lead to SET switching voltage and current of ~0.5 V and 0.2 μA, respectively. The PCM volumes of such smallest addressable bits would be of the order ~20 nm^3. In addition, a comparable volume of the surrounding GST and SiO_2 will be heated up to approximately 1/3 of the temperature of the GST bit, based on the simulations of Fig. S4 and Ref. (*7*). Here, the three roles of the CNT as the smallest low-resistance electrodes (~2 nm diameter) *and* that of low thermal conductivity of the GST and SiO_2 (~1 $Wm^{-1}K^{-1}$) *and* that of the CNT-GST interface thermal resistance are important in limiting the bit volume. This is in accord with experimental observations in Fig. S6 above and Fig. 2C in the main text, where only a GST volume of diameter comparable to that of the CNT is addressed and participates in switching; this fact is also supported by our simulations, see Fig. S4.

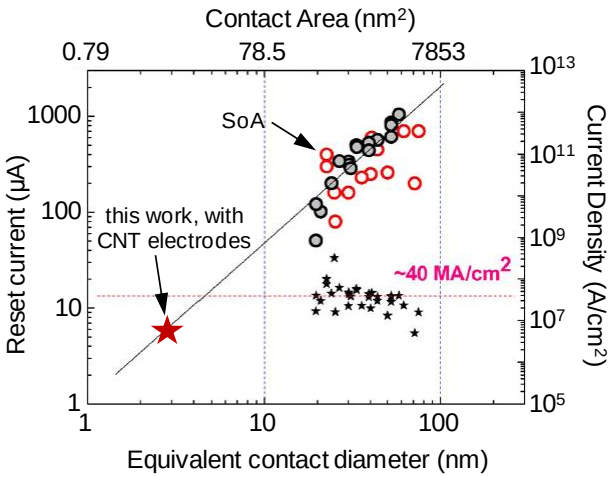

Fig. S8. *Scaling of programming current in phase-change materials (PCM), >0.1 mA in commercial state-of-the-art (SoA) [after (10)]. Our results with CNT electrodes (this work) show approximately two orders of magnitude lower power and reset current.*

We estimate the absolute lowest limits of programming energy of the smallest GST bits as follows. We take GST and SiO_2 heat capacity from Table 1 (*7*), a temperature rise $\Delta T \sim 150$ K for the a→c transition (SET) and $\Delta T \approx 600$ K for the c→a transition (RESET). The programming energy/bit is $E = \sum C_i V_i \Delta T_i$ where the subscript i represents the material heated (GST or SiO_2) and V_i is the respective volume (*7, 8*). The absolute minimum energy needed to heat up and switch such small bits are $E_{SET} \approx 5 \times 10^{-18}$ J (= 5 aJ) and $E_{RESET} \approx 2 \times 10^{-17}$ J (= 20 aJ).

More conservative (and realistic) estimates can be obtained considering that the shortest pulses known to induce switching in GST today are of the order ~2.5 ns for SET and 0.4 ns for RESET (*11*). The switching estimates then become $E_{SET} \approx E_{RESET} \approx 0.2$ fJ, with programming power of the order ~0.1 μW. In practice, our sharpest pulses in this work are ~20 ns, limited by the Keithley 3402 pulse generator and our pad and cable layout. These lead to switching energy of the order ~100 fJ/bit in this work. While these calculations are simple, they are backed up by finite-element simulations [Section 3 above, and Ref. (*7*)], and they serve as useful indicators of the energy and power dissipation limits of such devices.

We compare the RESET current and current density of our devices with that of state-of-the-art (SOA) technology, as shown in Fig. S8. This figure compares our results with those widely available among SOA as summarized by Ref. *(10)*. The typical current density of SOA devices is of the order 40 MA/cm^2 (with a fairly broad spread, from 10-100 MA/cm^2) as shown in Fig. S8. The best RESET current of our devices is ~5 μA (Fig. S7), but the current density varies from a maximum at the "tip" of the CNT electrodes to a minimum as the current spreads into the GST bit (Fig. S4). With this consideration, our device current density is also in the range ~10-100 MA/cm^2, which is consistent with the present SOA. The significant advantage of our device geometry comes from the extremely small diameter and good conductivity of the CNT electrodes.

7. Comparison with Critical Nucleus Size in GST

In this Section we compare our minimum bit sizes (as small as a few hundred cubic nanometers, as described in Section 6) with the minimum dimensions imposed by the critical nucleus in GST. The crystallization process in GST is nucleation driven. According to classical nucleation theory, there is a critical radius r_c, below which the crystallization process is energetically not favorable. This critical radius r_c may be calculated from the interfacial free energy σ and the Gibbs free energy difference between the parent and the crystalline phase per unit volume $\Delta G_{lc,V}$, as $r_c = 2\sigma/\Delta G_{lc,V}$ (*12*). Taking σ = 40 mJ/m^2 (*13*), ΔG_c = 1.15 eV and using the relationship $\Delta G_c = (16\pi/3)\sigma^3/(\Delta G_{lc,V})^2$ (*12*), we estimate that the critical radius r_c ~ 1.05 nm. The smallest GST bits addressed in our experiments are of the order ~10 nm, being approximately an order of magnitude greater than r_c in any of the three directions. This suggests that smaller volumes of GST could be addressed still, with sub-femtojoule switching energy as estimated above.

8. Subthreshold Measurements of Ultra-Thin GST

We investigated the temperature dependence of our a-GST subthreshold current to understand the transport mechanism. The subthreshold I-V of a typical CNT-PCM device (here with V_T = 7.2 V) as a function of temperature in vacuum are shown in Fig. S9. The subthreshold current shows an exponential dependence on applied voltage >0.5 V, which is typical in amorphous chalcogenides (*14*), confirming the a-GST transport. To further understand this, we extract the activation energy of our a-GST as a function of its applied bias. For any voltage, we plot the subthreshold current at different temperatures as a function of 1/kT, as shown in the Arrhenius plot in Fig. S9B (also Fig. 2A right inset). We obtain the activation energy as the negative of the slope of the linear fit, here E_A = 0.396, 0.385 and 0.374 eV for applied bias of 1, 2 and 3 V, respectively. While more work is needed to understand subthreshold conduction in such thin GST films (here ~10 nm), these results are similar to Ref. (*14*) for thicker films. This result is important by itself, as it confirms that the conduction mechanism even in the ~10 nm thin a-GST films used here is a temperature- and field-activated trap-assisted mechanism. The activation energy decreases as the applied bias increases, since the electric field lowers the potential barrier (*14*).

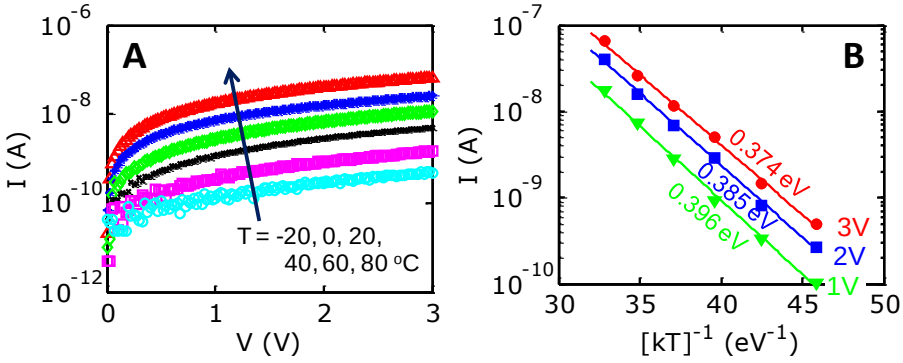

Fig. S9. *Temperature dependent subthreshold measurements.* ***(A)*** *Current-voltage of ~10 nm thin film PCM in the subthreshold regime (in vacuum, with increasing temperature).* ***(B)*** *Arrhenius plot of subthreshold current. Activation energies are extracted from the negative slope of the fit, with values of E_A = 0.396, 0.385 and 0.374 eV at applied bias 1, 2 and 3 V, respectively. These results show that even at ~10 nm GST film thicknesses and sub-50 nm bit dimensions, the subthreshold conduction mechanisms are similar to those previously reported for a-GST (14).*

9. Supplementary References

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