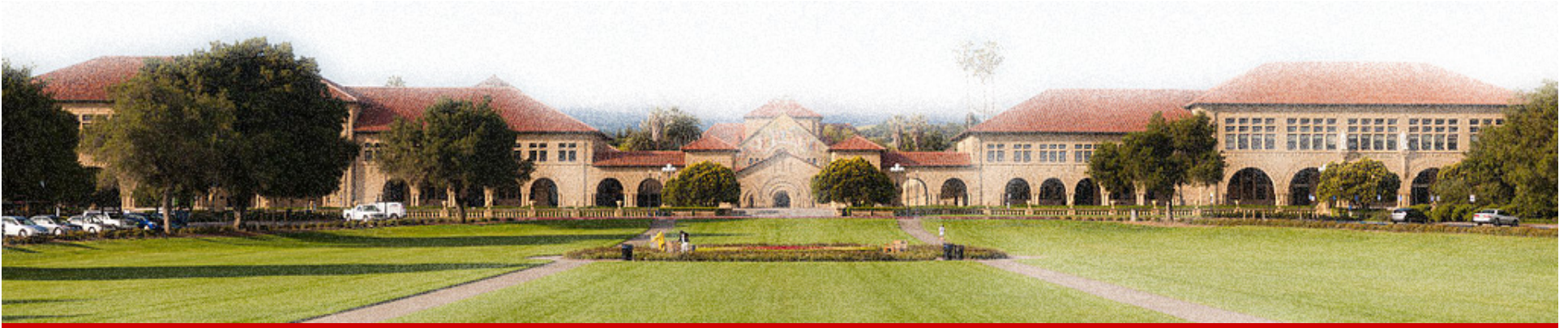


# Thermal Resistance (measurements & simulations) In Electronic Devices

(part of an online short course)

Eric Pop  
Electrical Engineering, Stanford University



# Topics

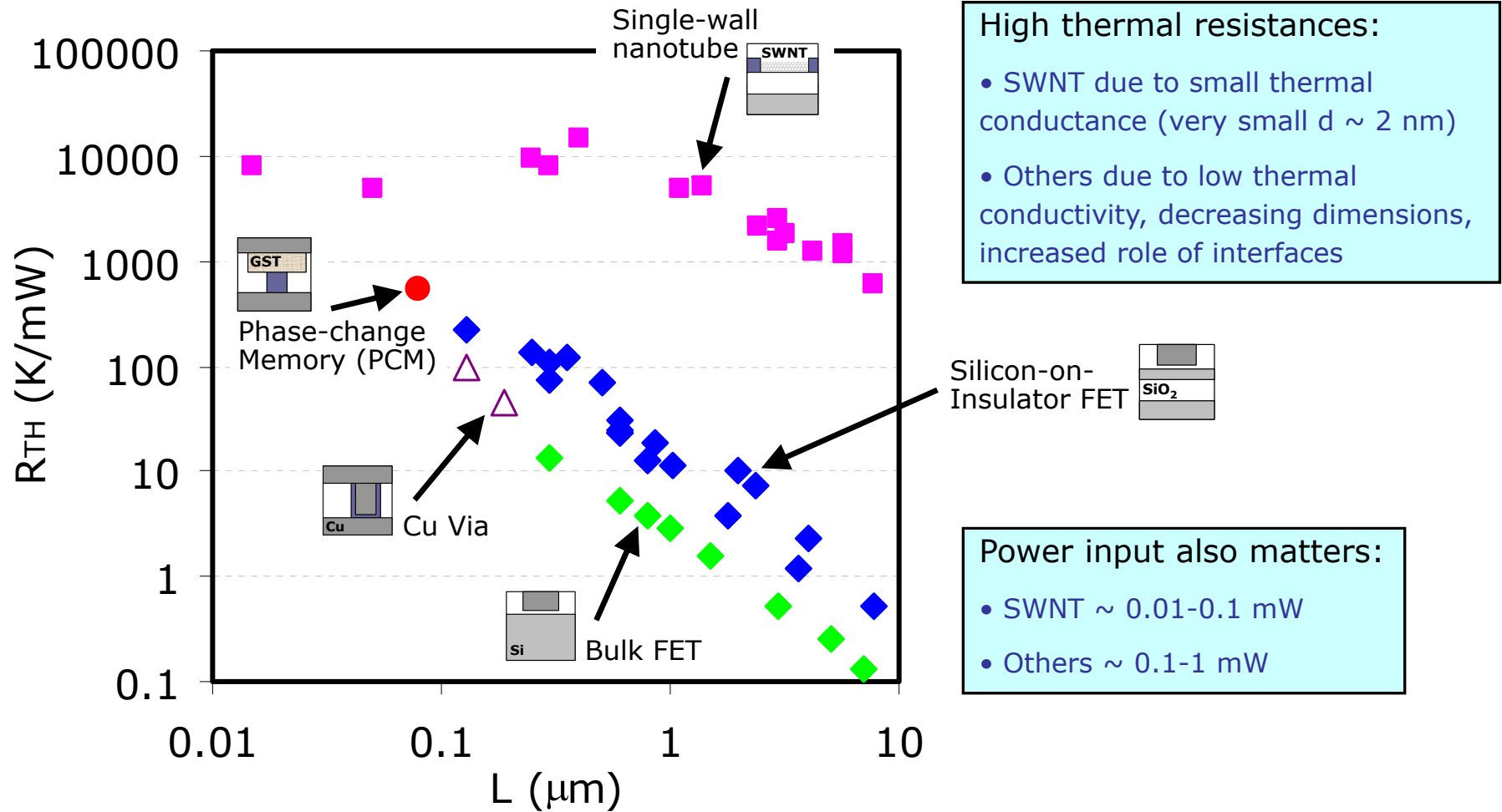
- 1) Basics of Joule Heating
- 2) Heating in Devices & Circuits
- 3) Thermal Resistance & Estimates**
- 4) Device Thermometry

# Thermal-Electrical Cheat Sheet

<u>Thermal</u>			<u>Electrical</u>	
Temperature	$T$ [K]	$\Leftrightarrow$	Voltage	$V$ [V]
Heat	$Q$ [J]	$\Leftrightarrow$	Charge	$Q$ [C]
Heat transfer rate	$q$ [W]	$\Leftrightarrow$	Current	$i$ [A]
Thermal resistance	$R_T$ [K/W]	$\Leftrightarrow$	Electrical resistance	$R$ [V/A]
Thermal capacitance	$C_T$ [J/K]	$\Leftrightarrow$	Electrical capacitance	$C$ [C/V]
<b>Governing equations</b>				
<u>Steady-State condition</u>				
Temperature Rise		$\Leftrightarrow$	Voltage Difference	
$\Delta T = q R_T$			$\Delta V = i R$	
<u>Transient condition</u>				
Heat diffusion		$\Leftrightarrow$	RC transmission line	
$\nabla^2 T = R_T C_T \frac{\partial T}{\partial t}$			$\nabla^2 V = RC \frac{\partial V}{\partial t}$	

Figure 1. Thermal-Electrical analogous quantities.

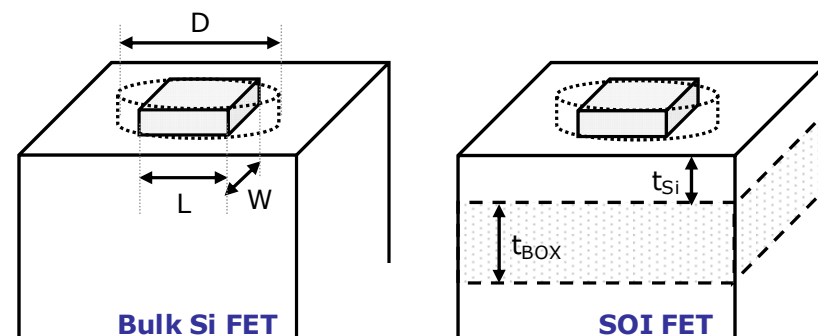
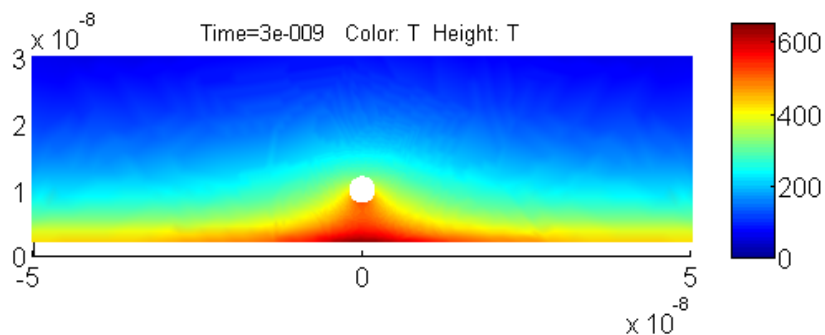
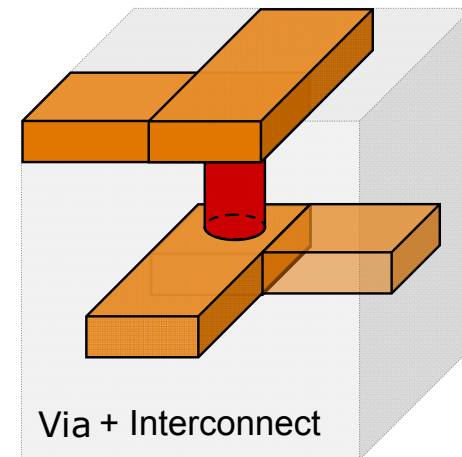
# Device Thermal Resistance Data



Data: Mautry (1990), Bunyan (1992), Su (1994), Lee (1995), Jenkins (1995), Tenbroek (1996), Jin (2001), Reyboz (2004), Javey (2004), Seidel (2004), Pop (2004-6), Maune (2006).

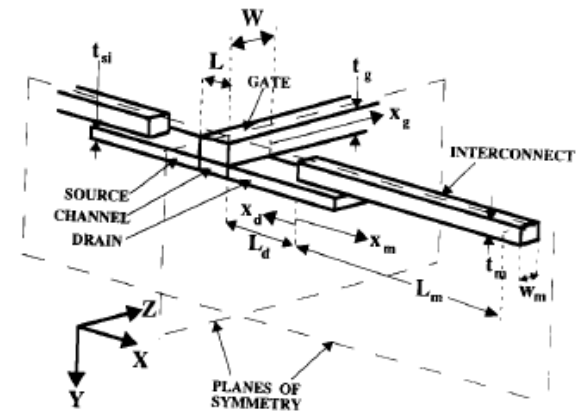
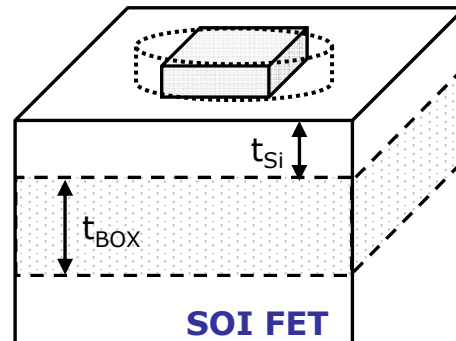
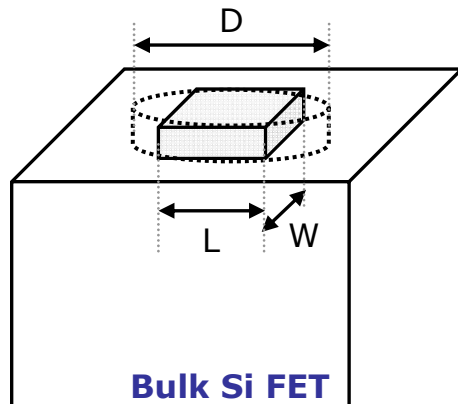
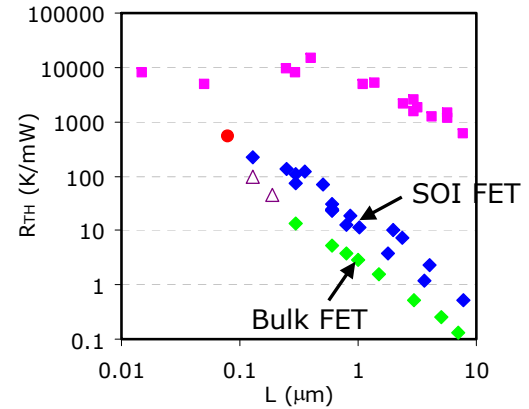
# Approaches for Thermal Resistance

- Time scale:
  - **Steady-State (DC)**
  - Transient
- Geometric complexity:
  - Lumped element (shape factors)
  - Analytic
  - Finite element (Fourier law)



# Modeling Device Thermal Resistance

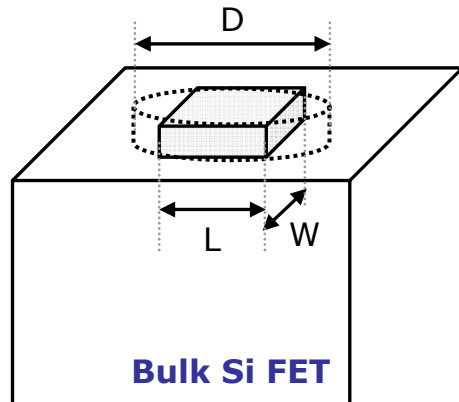
- Steady-state (DC) models
  - Lumped: Maury (1990), Goodson-Su (1994-5), Pop (2004), Darwish (2005)
  - Finite-Element



$$R_{TH} = \frac{1}{2k_{Si}D} \approx \frac{1}{2k_{Si}\sqrt{LW}} S$$

$$R_{TH} \approx \frac{1}{2W} \left( \frac{t_{BOX}}{k_{BOX}k_{Si}t_{Si}} \right)^{1/2}$$

# Examples (1)

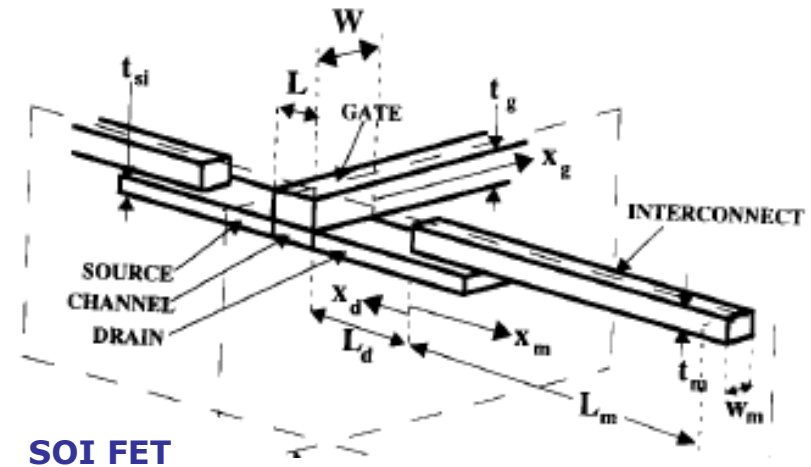


$$R_{TH} = \frac{1}{2k_{Si}D} \approx \frac{1}{2k_{Si}\sqrt{LW}} S$$

$k_{Si} \sim 100 \text{ Wm}^{-1}\text{K}^{-1}$  (highly doped Si)  
and "D" = 1  $\mu\text{m}$

then  $R_{TH} \sim 5 \text{ K/mW}$

so  $\Delta T = PR_{TH} \sim 5 \text{ K}$  with 1 mW power



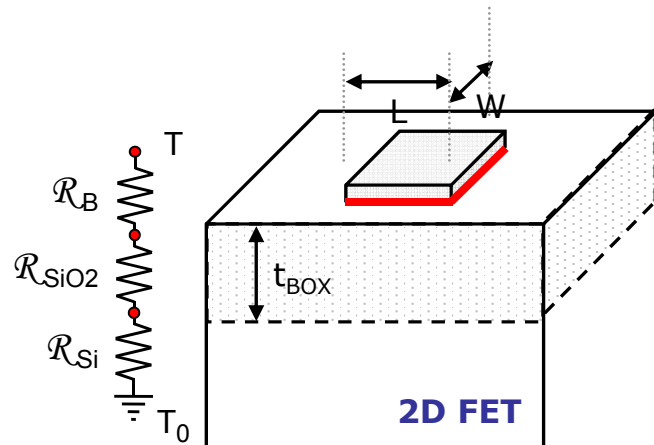
$$R_{TH} \approx \frac{1}{2W} \left( \frac{t_{BOX}}{k_{BOX}k_{Si}t_{Si}} \right)^{1/2}$$

$t_{Si} = 10 \text{ nm}$ ,  $t_{BOX} = 50 \text{ nm}$ ,  $W = 1 \mu\text{m}$   
 $k_{Si} \sim 10 \text{ Wm}^{-1}\text{K}^{-1}$  (reduced in thin film)  
and  $k_{BOX} \sim 1.4 \text{ Wm}^{-1}\text{K}^{-1}$

then  $R_{TH} \sim 130 \text{ K/mW}$

so  $\Delta T = PR_{TH} \sim 67 \text{ K}$  with 0.5 mW power

# Examples (2)



$t_{\text{BOX}} = 90 \text{ nm}$ ,  $L = W = 1 \text{ }\mu\text{m}$  and  $k_{\text{BOX}} \sim 1.4 \text{ W/m/K}$   
 TBR = thermal boundary resistance  $\sim 10^{-8} \text{ m}^2\text{K/W}$

$$R_B = \text{TBR} / (WL) \sim 10 \text{ K/mW}$$

$$R_{\text{SiO}_2} = t_{\text{BOX}} / (k_{\text{BOX}} * WL) \sim 60 \text{ K/mW}$$

$$R_{\text{Si}} = 1 / [2 * k_{\text{Si}} * (W + t_{\text{BOX}})] \sim 4.5 \text{ K/mW}$$

total  $R_{\text{TH}} \sim 75 \text{ K/mW}$  so  $\Delta T = PR_{\text{TH}} \sim 30 \text{ K}$  with  $0.4 \text{ mW}$  power

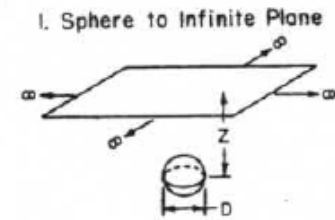
note the  $\text{SiO}_2$  layer dominates, but TBR also plays an important role



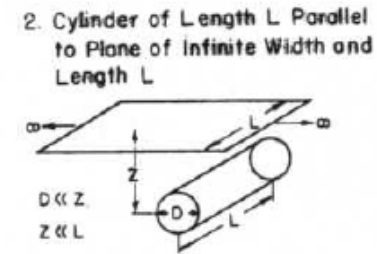
# Shape Factors

Sunderland, ASHRAE (1964), many others

- Heat flux:  $q = Sk(T_1 - T_0)$
- Equivalent thermal resistance  $R_{TH} = 1/Sk$



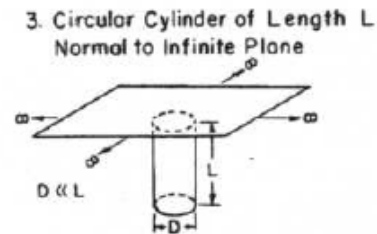
$$S = \frac{2\pi D}{1 + (D/4Z)}$$



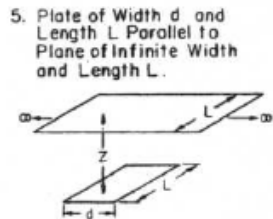
$$S \approx \frac{2\pi L}{\ln(4Z/D)}$$

a more exact solution is:

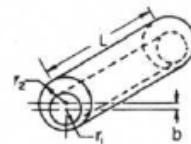
$$S = \frac{2\pi L}{\cosh^{-1}(2Z/D)}$$



$$S = \frac{2\pi L}{\ln(4L/D)}$$

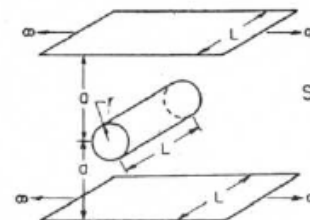


$$S = 1.45 \left[ \log \frac{Z+d}{d} \right]^{-0.59} L$$

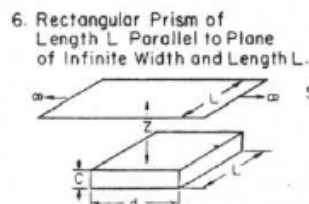


$$S = \frac{2\pi L}{\cosh^{-1} \left[ \frac{r_1^2 + r_2^2 - b^2}{2r_1 r_2} \right]}$$

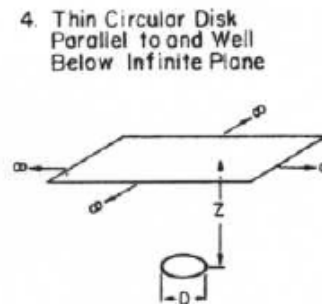
12. Cylinder of Length L between Parallel Planes of Infinite Width and Length L.



$$S = \frac{2\pi L}{\ln(4a/\pi r)}$$



$$S = 1.685 \left[ \log \frac{Z+d}{d} \right]^{-0.59} \left[ \frac{Z}{c} \right]^{-0.078} L$$



$$S \approx 4D$$

more exact:

$$S = \frac{4.44D}{1 - (D/5.66Z)}$$

# Many Shape Factors (Compact Models)

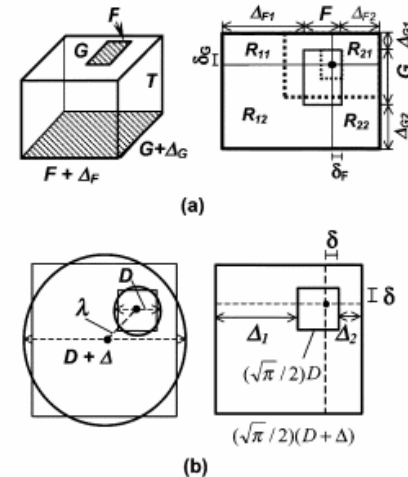
IEEE ELECTRON DEVICE LETTERS, VOL. 26, NO. 12, DECEMBER 2005

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## A Unified Compact Model of Electrical and Thermal 3-D Spreading Resistance Between Eccentric Rectangular and Circular Contacts

Shreepad Karmalkar, P. Vishnu Mohan, and B. Presenna Kumar

$$\frac{R_{\Delta F=0}^{\Delta G \rightarrow \infty}}{R_{\Delta G=0}^{\Delta F=0}} = \frac{G}{2T \tan \alpha_G} \ln \left( 1 + \frac{2T \tan \alpha_G}{G} \right)$$

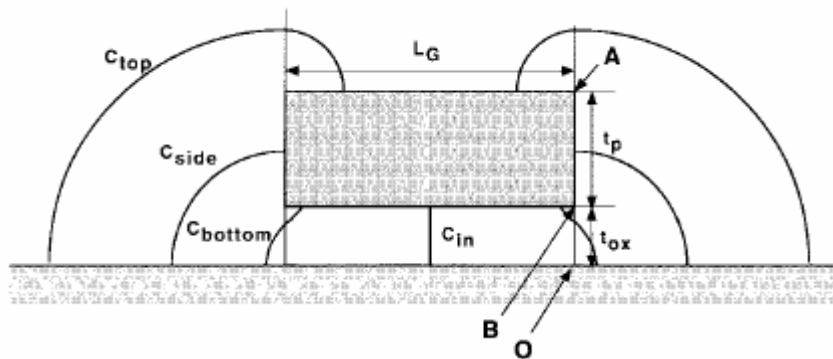


IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 46, NO. 9, SEPTEMBER 1999

1895

## Parasitic Capacitance of Submicrometer MOSFET's

Kunihro Suzuki, *Member, IEEE*



$$C_{\text{side}} = \frac{\epsilon_{ox}}{\pi} \ln[a]$$

$$a = 2K(K^2 - 1)^{1/2} + 2K - 1$$

$$K = 1 + \frac{t_p}{t_{ox}}$$

# Obtaining the Temperature Distribution

- So far we've only looked at lumped thermal models
- Now we want temperature distribution  $T(x)$
- Simplest case: Si layer on  $\text{SiO}_2/\text{Si}$  substrate (SOI)
- Or interconnect on thermally insulating  $\text{SiO}_2$

$$T_m - T_0 = Z_1 \cosh [m_m(L_m - x_m)] \quad (1)$$

$$T_d - T_0 = Z_2 \exp[m_d x_d] + Z_3 \exp[-m_d x_d] \quad (2)$$

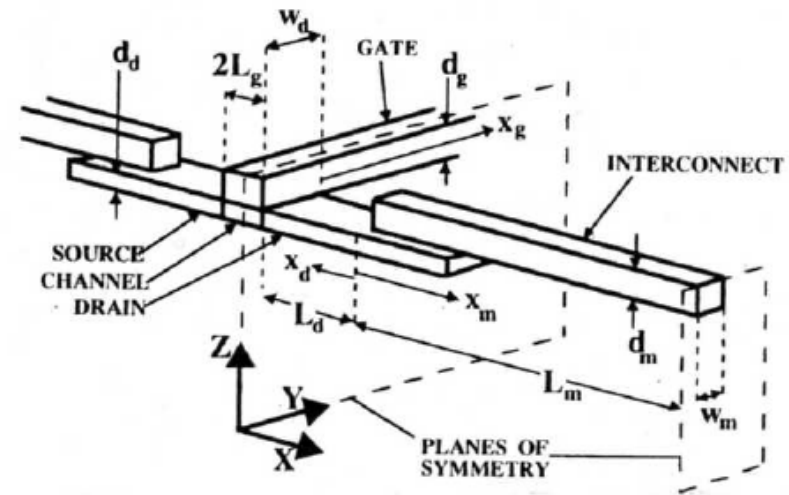
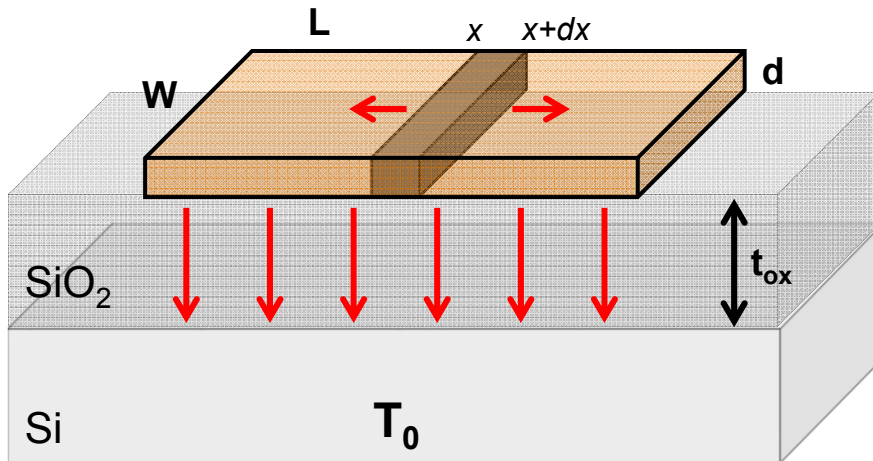


Fig. 2 Geometry of the thermal model of a SOI FET (Goodson and Flik, 1992)

# 1-D Interconnect with Heat Generation



$$\text{Heat: } Q = -Ak \frac{dT}{dx}$$

$$\text{Electrical: } I = AJ = A(\sigma F) = A\sigma \frac{dV}{dx}$$

Write energy balance equation  
for element "dx"  
pick units of J or W (= J/s)

**Energy In (here, Joule heat) = Energy Out (left, right, bottom) + Change in Internal Energy**

$$Q''' Adx - kA \left. \frac{\partial T}{\partial x} \right|_x - kA \left. \frac{\partial T}{\partial x} \right|_{x+dx} + hWdx(T - T_0) = C(Adx) \frac{\partial T}{\partial t}$$

divide by ( $Adx$ ):

$$Q''' + \nabla(k\nabla T) - h \frac{W}{A} (T - T_0) = C \frac{\partial T}{\partial t}$$

e.g.  $J \cdot E$  if non-uniform  
or  $I^2 R / (W L d)$  if uniform

convection-like term, here  $h = k_{\text{ox}} / t_{\text{ox}}$  and  $W/A = 1/d$   
"W" can be "perimeter" if heat loss in all directions

# Ex: 1D Rectangular Nanowire

## Analysis of failure mechanisms in electrically stressed Au nanowires

C. Durkan,<sup>a)</sup> M. A. Schneider, and M. E. Welland

Department of Engineering, Nanoscale Science Group, University of Cambridge, Trumpington Street, Cambridge CB2 1PZ, United Kingdom

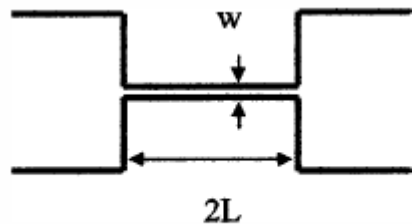


FIG. 1. Schematic of wire geometry.

$$\nabla^2 T - m^2 T + \frac{Q}{k} = 0, \quad (1)$$

where

$$m = \sqrt{\frac{k_{\text{sub}}}{ktd}}$$

$1/m$  is natural length scale  
“thermal healing length”

$$L_H = \sqrt{\frac{k}{k_{\text{sub}}} td_{\text{sub}}}$$

where  $Q = J^2 \rho$ ,  $k$ ,  $k_{\text{sub}}$ ,  $t$  and  $d$  are the thermal conductivity and thickness of the wire and the substrate, respectively. It should be noted that the resistivity of such a film will be approximately 2.5 times larger than the bulk value due to grain boundary scattering and the Fuchs size effect.<sup>5</sup> The

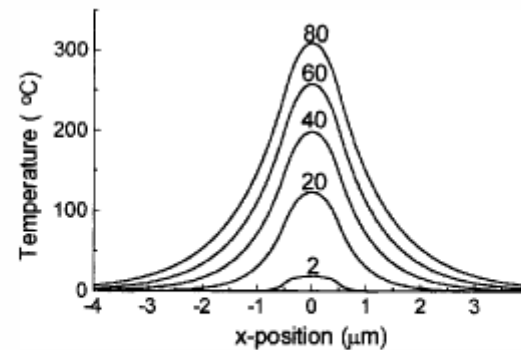


FIG. 2. Calculated temperature along 20 nm thick and 1000 nm long Au wires carrying  $2 \times 10^{12} \text{ A m}^{-2}$ , for several substrate oxide thicknesses (in nm).

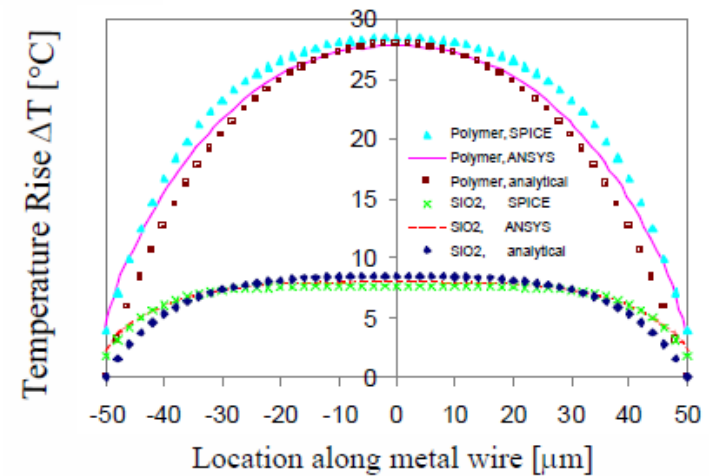
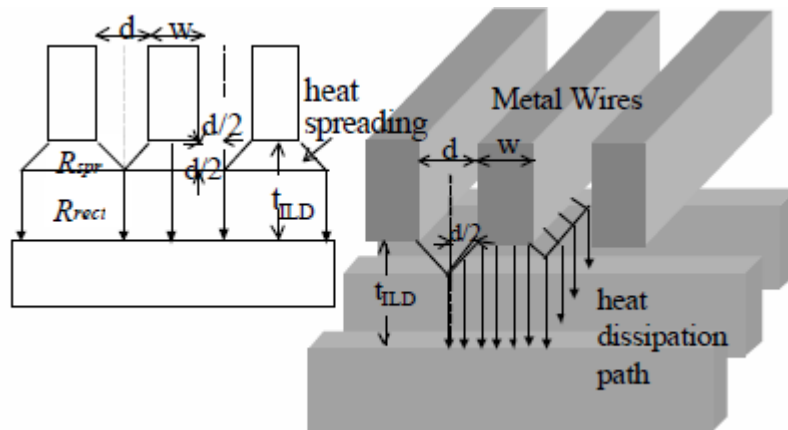
$$T_{\text{wire}} = -\frac{Q}{2km^2} e^{-mL} (e^{mx} + e^{-mx}) + Q e^{-mx} \left( \frac{td}{k_{\text{sub}}} - \frac{1}{km^2} \right) + \frac{Q}{km^2}, \quad (2)$$

$$T_{\text{contact}} = Q \left[ \frac{td}{k_{\text{sub}}} - \frac{1}{km^2} + \frac{1}{2km^2} (e^{mL} - e^{-mL}) \right] e^{-m|x|}. \quad (3)$$

# Interconnect Heat Loss and Crosstalk

## Analytical Thermal Model for Multilevel VLSI Interconnects Incorporating Via Effect

Ting-Yen Chiang, Kaustav Banerjee, *Member, IEEE*, and Krishna C. Saraswat, *Fellow, IEEE*



$$T(x) = T_0 + \Delta T_{Max} \left( 1 - \frac{\cosh(x/L_H)}{\cosh(L/2L_H)} \right), \quad -L/2 \leq x \leq L/2 \quad (9)$$

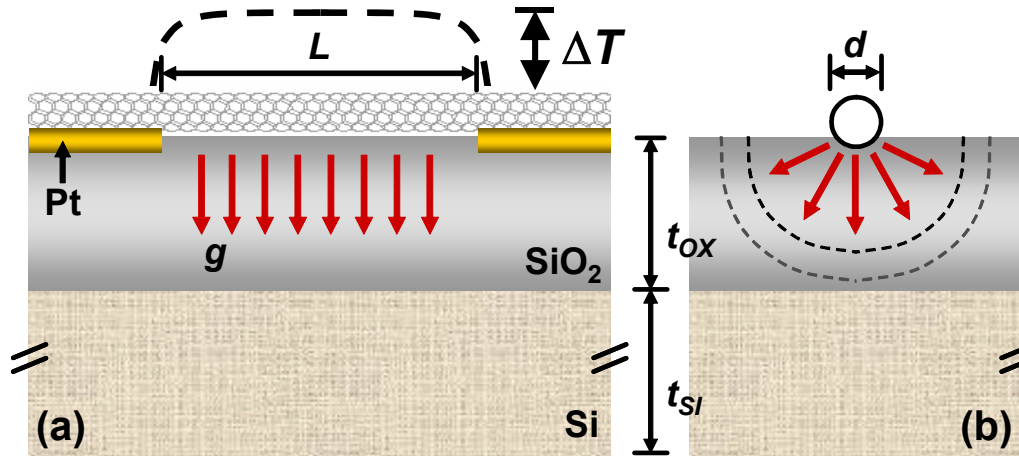
where  $\Delta T_{Max}(= j_{rms}^2 \rho L_H^2 / k_M)$  is the temperature rise in the wire

$$R_{th,ILD} = \frac{t_{ILD}}{k_{ILD} w_{effective}} = \frac{t_{ILD}}{k_{ILD} w s}$$

Using (11) and (12),  $s$ , can be obtained as

$$s = \left( \frac{w}{t_{ILD}} \frac{1}{2} \left( \frac{w+d}{w} \right) + \frac{w}{t_{ILD}} \frac{t_{ILD} - d/2}{w+d} \right)^{-1}$$

# Ex: Carbon Nanotube (Cylinder)

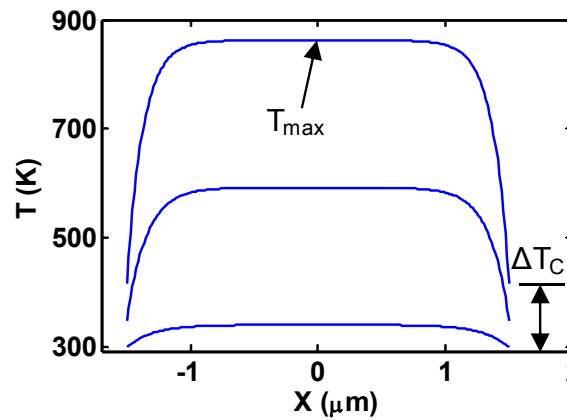


$$A\nabla(k\nabla T) + p' - g(T - T_0) = 0$$

$$T(x) = T_0 + \frac{p'}{g} \left[ 1 - \frac{\cosh(x/L_H)}{\cosh(L/2L_H)} \right]$$

$$p' = I^2 \frac{dR}{dx} = I^2 \frac{h}{4q^2} \frac{1}{\lambda_{eff}} \quad L_H = \sqrt{\frac{kA}{g}}$$

Role of cylindrical heat spreading (shape factor!)  $\left. \vphantom{\frac{\pi k_{ox}}{\ln\left(\frac{8t_{ox}}{\pi d}\right)}} \right\} g_{ox} = \frac{\pi k_{ox}}{\ln\left(\frac{8t_{ox}}{\pi d}\right)}$



Role of thermal contact resistance

$$\left. \vphantom{\frac{kA}{dx} \Big|_C} \right\} kA \frac{dT}{dx} \Big|_C = \frac{\Delta T_C}{\mathcal{R}_{C,Th}}$$

E. Pop *et al.*  
J. Appl. Phys. 101, 093710 (2007)



# Further Reading

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- C. Durkan et al., “Analysis of failure mechanisms in electrically stressed Au nanowires,” *J. Appl. Phys.* **86**, 1280 (1999), <http://dx.doi.org/10.1063/1.370882>
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- T.-Y. Chiang et al., “Analytical Thermal Model for Multilevel VLSI Interconnects Incorporating Via Effect,” *IEEE EDL* **23**, 31 (2002), <http://dx.doi.org/10.1109/55.974803>
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- E. Pop, “Energy Dissipation and Transport in Nanoscale Devices,” *Nano Research* **3**, 147 (2010), <http://dx.doi.org/10.1007/s12274-010-1019-z>

