Achieving 1-nm-Scale Equivalent Oxide Thickness Top-Gate Dielectric on Monolayer Transition Metal Dichalcogenide Transistors With CMOS-Friendly Approaches

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***Abstract*— Monolayer two-dimensional transition metal dichalcogenides (2-D TMDs) are promising semiconductors for future nanoscale transistors owing to their atomic thinness. However, atomic layer deposition (ALD) of gate dielectrics on 2-D TMDs has been difficult, and reducing the equivalent oxide thickness (EOT) with CMOS-compatible approaches remains a key challenge. Here, we report ultrathin top-gate dielectrics on monolayer TMDs using industry-friendly approaches, achieving 1-nm-scale top-gate EOT. We first show ALD of HfO_2 on both monolayer WSe_2 and MoS_2 with a simple Si seed, enabling EOT $\approx$ 0.9 nm with subthreshold swing SS $\approx$ 70 mV/dec, low leakage, and negligible hysteresis on MoS_2. We also demonstrate direct ALD of ultrathin alumina (AlO_x) on monolayer MoS_2 with good quality and uniformity using triethylaluminum (TEA) precursor, followed by ALD of HfO_2. Combining our findings, we show that the threshold voltage (V_T) can be controlled by the interfacial dielectric layer on the 2-D transistor channel.**

***Index Terms*— 2-D semiconductor, atomic layer deposition (ALD), equivalent oxide thickness (EOT), gate-stack, MoS_2, threshold voltage (V_T), triethylaluminum (TEA).**

I. Introduction

THE 2-D transition metal dichalcogenides (2-D TMDs) are promising semiconductors for electronics, showing good mobility in atomically thin (even sub-nm) films [1], low OFF-state current due to bandgaps larger than silicon [2], and back-end-of-line compatible growth temperature [3], [4]. However, high-quality TMDs with good transport properties (e.g., mobility) must have low defect density, that is, very few or even no partially filled surface dangling bonds. This means that atomic layer deposition (ALD) of ultrathin dielectrics cannot easily occur due to lack of nucleation sites on the TMD surface [5] unlike the surface of conventional semiconductors, like Si. To achieve top-gate dielectrics on 2-D TMDs, previous studies have used a thin seed layer deposited by physical vapor deposition [6], [7], [8], [9], [10], [11] or chemical vapor deposition (CVD) [12], [13]. However many of these approaches either lack semiconductor industry compatibility, or cannot achieve sub-1 nm equivalent oxide thickness (EOT), as required by modern and future technologies [14]. Here, the EOT is the equivalent SiO_2 thickness with the same capacitance as that of the actual insulator being used. (Specifically, EOT $= 1$ nm is 3.45 μF/cm^2 capacitance per unit area.)

In this work, we describe two approaches to achieve 1-nm-scale top gate EOT on 2-D TMD transistors with industry-friendly materials and processes. We first introduce use of an ultrathin Si seed layer deposited by electron-beam evaporation that enables ALD of HfO_2 on monolayer (1L) MoS_2 and WSe_2. Then, we show direct ALD of ultrathin aluminum oxide (AlO_x) at low temperature on monolayer MoS_2 which facilitates subsequent ALD of HfO_2. Through both approaches, we also show that the threshold voltage (V_T) of monolayer MoS_2 transistors can be engineered by scaling the interlayer (seed layer) of the top-gate dielectric. While some preliminary aspects of this work were presented in a conference abstract [15], in this article we present additional data, more comprehensive discussion and characterization.

II. Evaporated Silicon Seed Layer for 2-D TMDs

We first examine the deposition of Si seed layer [11] by electron-beam evaporation on monolayer WSe_2 and MoS_2. This approach is used because Si evaporation is widely available in many academic and research facilities, potentially enabling a relatively easy method to achieve ultrathin-EOT top gates. We first check if the Si seed evaporation process damages the 2-D TMDs, which were grown by CVD on SiO_2/Si substrates [16]. Fig. 1 shows Raman measurements

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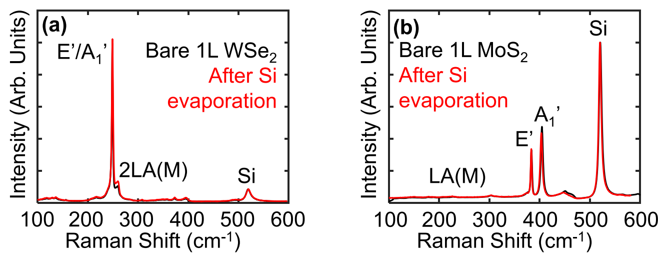

Fig. 1. Raman spectra before (black) and after (red) thin ~1 nm Si layer evaporation on bare (a) monolayer (1L) WSe_2 and (b) monolayer MoS_2, on SiO_2 (90 nm) on Si substrate. Both signals are normalized to the Si peak at ~520 cm^{-1}. Laser source of 532 nm wavelength, with incident power of 2.5% (0.12 mW) was used. Raman signals before and after Si seed evaporation show almost no difference, indicating no clear evidence of damage for both monolayer WSe_2 and MoS_2.

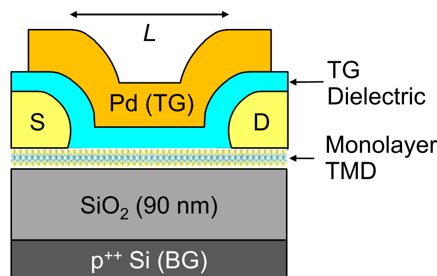

Fig. 2. Cross-sectional schematic of our dual-gated monolayer TMD transistors (not to scale). Au and Pd are deposited as source (S)/drain (D) contact metal to monolayer MoS_2 and WSe_2, respectively. Pd is used as top gate (TG) metal for both MoS_2 and WSe_2 transistors. The highly doped Si can also be used as a back gate (BG).

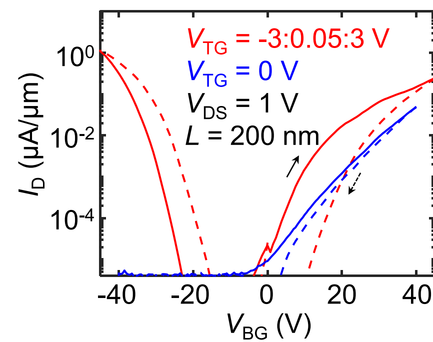

Fig. 3. I_D versus V_{BG} of monolayer WSe_2 transistor using top-gate dielectric with Si ~1 nm/HfO_2 ~5 nm. Measurements are with V_{TG} = 0 V (in blue, unipolar) and with dual-gating (in red, ambipolar). Solid and dashed lines represent forward and reverse sweeps, respectively.

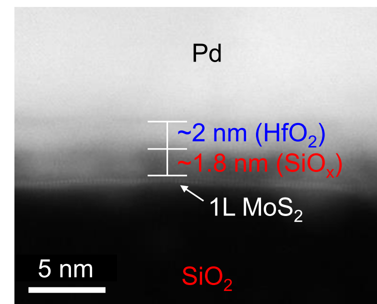

Fig. 4. Cross-sectional STEM image of a top-gate stack with ~0.7 nm Si seed (which becomes 1.6–1.8 nm of SiO_x) followed by ALD HfO_2 ~2 nm on monolayer MoS_2, on SiO_2. The TG here is Pd.

before and after Si deposition onto our monolayer WSe_2 and MoS_2. Here, we evaporate ~1 nm of Si with a deposition rate of 0.2 Å/s and chamber pressure of ~10^{-7} Torr. For both monolayer WSe_2 and MoS_2, we do not observe any clear evidence of damage from the Si evaporation, as the Raman spectra before and after the seed layer remain virtually indistinguishable. No LA(M) peak (which has been correlated with defects) appears in the monolayer MoS_2, and the existing E′ and A_1' peaks remain unchanged [17].

We next proceed to incorporate such seed layers into transistors with a top gate (TG), whose cross-sectional schematic is shown in Fig. 2. These are effectively dual-gate transistors because the highly doped Si substrate can also be used as a back gate (BG). The fabrication process flow is as follows: first, we synthesize monolayer MoS_2 at 750 °C or monolayer WSe_2 at 850 °C directly by CVD on a thermally oxidized 90 nm thick SiO_2 on a highly doped p-type silicon substrate [16]. We pattern and etch the active channel region using XeF_2 dry-etch recipe, followed by source (S) and drain (D) contact metal deposition using electron-beam evaporation of Au and Pd for MoS_2 and WSe_2, respectively. These can now already serve as back-gated monolayer TMD transistors.

Then, we deposit a blanket Si seed layer by electron-beam evaporation at a rate of ~0.2 Å/s and chamber pressure of ~10^{-7} Torr. When the Si seed is exposed to air it oxidizes [11] into SiO_x and we continue with ALD of HfO_2 at 200 °C using tetrakis(dimethylamido) hafnium (IV) and H_2O as precursors on both WSe_2 and MoS_2, to form the TG dielectric. Finally, we deposit Pd as the top gate by electron-beam evaporation. In our devices, the TG and S/D have ~0.2 μm overlap (see Fig. 2) to avoid ungated channel resistance regions. All transistors are annealed and then measured in probe station vacuum (~10^{-4} Torr) at 150 °C and room temperature, respectively.

Fig. 3 shows drain current (I_D) versus back-gate voltage (V_{BG}) measurements of a top-gated monolayer WSe_2 device. These transistors display unipolar n-type behavior with the BG sweep when the top-gate is grounded ($V_{TG} = 0$ V). However, by double-gating (both BG and TG swept simultaneously, as labeled), the WSe_2 device shows ambipolar behavior from much tighter coupling of the TG. We note some hysteresis here due to suboptimal band alignment of monolayer WSe_2 with SiO_x defect states [18], which requires further investigation. Thus, for the remainder of this study we focus on TG dielectric deposition efforts on monolayer MoS_2, which we have found has almost no hysteresis.

Fig. 4 shows a scanning transmission electron microscopy (STEM) cross section of ~0.7 nm Si seed followed by ~2 nm ALD HfO_2 on monolayer MoS_2. We observe that the ~0.7 nm evaporated Si becomes 1.6–1.8 nm of SiO_x due to volume expansion during oxidation. The SiO_x interfacial layer displays good uniformity while providing ALD nucleation sites for the HfO_2 on top, without any physical damage seen in the monolayer MoS_2 channel. This is consistent with the Raman measurements displayed earlier, in Fig. 1(b).

We further reduce the Si seed thickness to fabricate monolayer MoS_2 devices with thinner TG dielectrics. Fig. 5(a) presents I_D versus V_{TG} of a representative device with ~0.2 nm Si seed followed by ~5 nm of ALD HfO_2 in the TG stack. This achieves an ON/OFF current ratio >10^7 and negligible hysteresis (<10 mV at constant current $I_D = 0.1$ nA/μm) due

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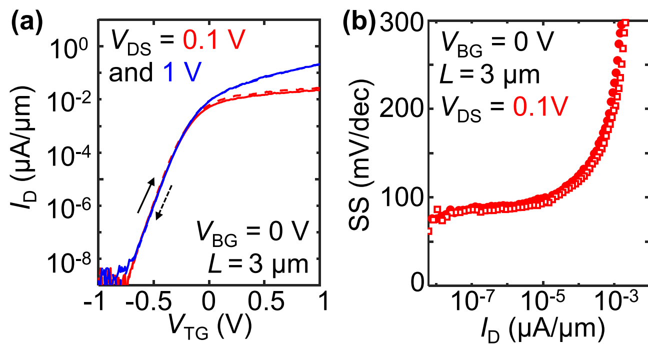

Fig. 5. (a) I_D versus V_{TG} of top-gated monolayer MoS_2 device with Si ~0.2 nm/HfO_2 ~5 nm as TG dielectric. Solid and dashed lines show forward and reverse sweeps, respectively. (b) Corresponding subthreshold swing SS versus I_D at V_{DS} = 0.1 V. Filled circles and unfilled squares represent forward and reverse sweeps, respectively. We observe SS reaching ~70 mV/dec at the lower current levels.

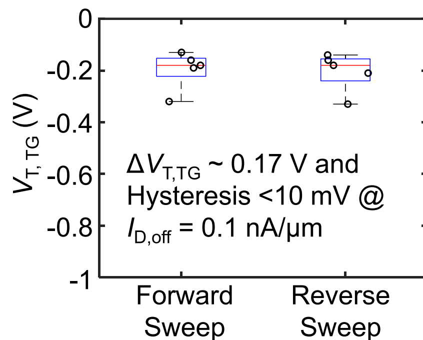

Fig. 6. Top-gate threshold voltage ($V_{T,TG}$) distribution from forward and reverse sweeps of devices with the same TG dielectric as Fig. 5. Here, V_{DS} = 0.1 V and V_{BG} = 0 V on 3-μm-long monolayer MoS_2 transistors. $V_{T,TG}$ are extracted at constant current I_D = 0.1 nA/μm.

to the good defect band alignment of the SiO_x interfacial layer with the monolayer MoS_2 conduction band [18]. Fig. 5(b) shows the corresponding subthreshold swing SS versus I_D, displaying $SS_{min} \approx$ 70 mV/dec at room temperature, enabled by the ultrathin interlayer of SiO_x.

We combine data from multiple devices in Fig. 6, which shows the top-gate threshold voltage ($V_{T,TG}$) distribution from several devices using the same gate stack as in Fig. 5. We note low TG device variability ($\Delta V_{T,TG}$) $\leq$ 0.17 V and consistent threshold voltage between forward and backward voltage sweeps. Here, $V_{T,TG}$ is extracted at constant current I_D = 0.1 nA/μm [19].

Fig. 7(a) and (b) shows the cross-sectional TEM image and the corresponding energy dispersive X-ray spectroscopy (EDS) of the device in Fig. 5(a) with evaporated ~0.2 nm Si followed by ~5 nm of ALD HfO_2 as the TG dielectric. Note there is no longer a clear distinction of the SiO_x/HfO_2 interface here due to the ultrathin Si seed, which likely gets "consumed." Nevertheless, the TG dielectric displays good uniformity with total physical thickness of ~5 nm. The EDS elemental mapping in Fig. 7(b) confirms uniform HfO_2 deposition on MoS_2, which is enabled by the ultrathin ~0.2 nm Si seed. Using the dielectric constant value of ~22 of the HfO_2 from our ALD chamber [20], we estimate the top-gate EOT $\approx$ 0.9 nm. More discussion on the estimation of top-gate EOT will be covered in a later section.

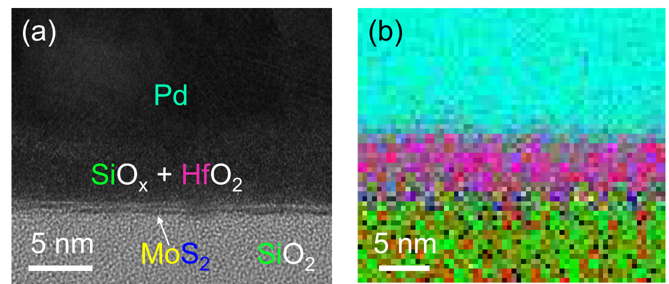

Fig. 7. (a) Cross-sectional TEM image of a top-gated monolayer MoS_2 FET using Si ~0.2 nm/HfO_2 ~5 nm as TG dielectric. (b) Corresponding EDS elemental mapping image. The elemental color mapping in (b) corresponds to the color of the elements in (a) except for oxygen.

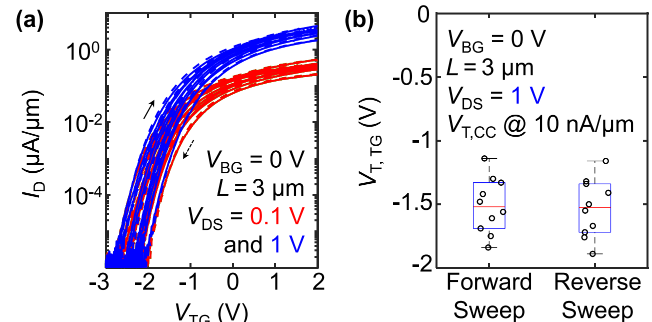

Fig. 8. (a) I_D versus V_{TG} of top-gated monolayer MoS_2 devices with TEA AlO_x ~6 nm/ALD HfO_2 ~6 nm as TG dielectric. Solid and dashed lines mark forward and reverse sweeps, respectively. Total of ten devices are measured, at V_{DS} = 0.1 V (red) and 1 V (blue). (b) Corresponding top-gate threshold voltage ($V_{T,TG}$) distribution comparing forward and reverse sweeps from devices shown in (a). $V_{T,TG}$ are extracted at constant current I_D = 10 nA/μm.

III. Low-Temperature ALD for MoS_2

In the previous section, we showed that evaporated Si seed layer can enable an ultrathin top-gate stack on monolayer TMD transistors. However, we note that evaporation is not conformal, and a process with conformal gate dielectric deposition for ultimate scaling of gate-all-around 2-D TMD transistors needs to be developed [21]. In this section, we describe direct ALD of alumina (AlO_x) at 100 °C using triethylaluminum (TEA) and H_2O as precursors. We refer to this as TEA AlO_x, and we have found that this process provides excellent ALD coverage of TEA AlO_x on monolayer MoS_2, which can also serve as a nucleation layer for ALD of HfO_2 on top [15]. Here, we discuss the behavior of our monolayer MoS_2 transistors using TEA AlO_x followed by ALD HfO_2 as the TG dielectric.

Fig. 8(a) shows the I_D versus V_{TG} curves from multiple measured devices using ~6 nm of TEA AlO_x followed by ~6 nm of HfO_2 as TG dielectric. Owing to the high-quality TEA AlO_x interlayer, devices show hysteresis as low as <10 mV (at constant current 10 nA/μm) with low defect density [18]. Fig. 8(b) shows the top-gate threshold voltage (extracted at constant current of 10 nA/μm) distribution of the forward and reverse sweeps from Fig. 8(a), and we note that the TG device-to-device variability across the chip is <0.7 V. The variability observed within the chips is largely attributed to limitations of the nanofabrication process at the academic research facilities where the devices were made.

Next, we reduce the interlayer TEA AlO_x thickness (down to 3 and 1.5 nm), and Fig. 9(a) shows I_D versus V_{TG} from

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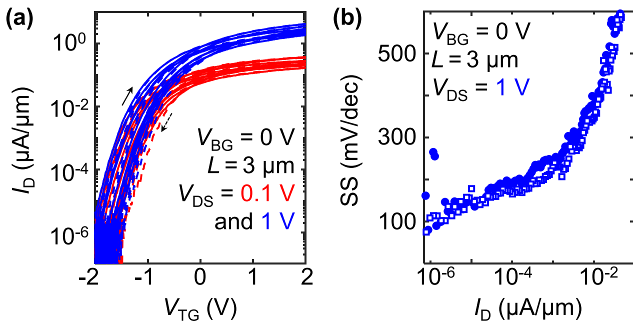

Fig. 9. (a) I_D versus V_{TG} of top-gated monolayer MoS_2 devices with TEA AlO_x ~3 nm/ALD HfO_2 ~6 nm as TG dielectric. Solid and dashed lines are forward and reverse sweeps, respectively. Total of ten devices are measured, at V_{DS} = 0.1 V (red) and 1 V (blue). (b) Corresponding subthreshold swing SS versus I_D from (a) with V_{DS} = 1 V. Filled circles and unfilled squares correspond to forward and reverse sweeps, respectively. With this TG dielectric stack, devices achieve SS < 100 mV/dec at room temperature.

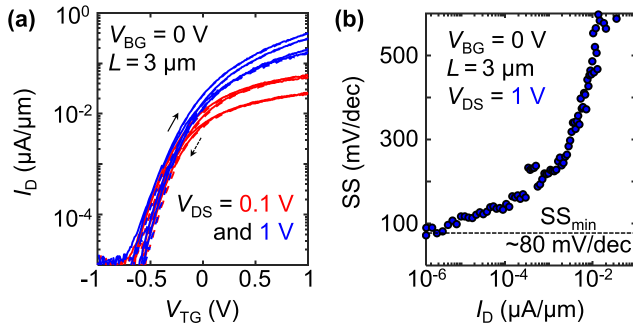

Fig. 10. (a) I_D versus V_{TG} of top-gated monolayer MoS_2 devices with TEA AlO_x ~1.5 nm / ALD HfO_2 ~6 nm as TG dielectric. Solid and dashed lines are forward and reverse sweeps, respectively. Total of four devices are measured, at V_{DS} = 0.1 V (red) and 1 V (blue). (b) Corresponding SS versus I_D from (a) with V_{DS} = 1 V. Using this TG dielectric stack, the device reaches SS ≈ 80 mV/dec, owing to the ultrathin TEA AlO_x on MoS_2.

multiple measured devices using ~3 nm of TEA AlO_x followed by ~6 nm of ALD HfO_2 as TG dielectric. Devices show ON/OFF current ratio $>10^6$ with hysteresis as low as <10 mV (at constant current of 10 nA/μm) with the reduced TEA AlO_x interlayer thickness of ~3 nm. Fig. 9(b) shows subthreshold swing SS versus I_D from a representative device in Fig. 9(a), with the minimum value SS_{min} reaching sub-100 mV/dec at room temperature.

We further reduce the TEA AlO_x interlayer thickness and Fig. 10(a) shows I_D versus V_{TG} from devices using ~1.5 nm of TEA AlO_x followed by ~6 nm of ALD HfO_2 as TG dielectric. Here, we observe that all devices show small hysteresis window of <10 mV (at constant current 10 nA/μm) owing to the ultrathin top gate dielectric. Moreover, Fig. 10(b) shows SS versus I_D from a representative device in Fig. 10(a), with the minimum SS_{min} reaching 80 mV/dec at room temperature. We note that this TG dielectric deposition approach uses materials (AlO_x, HfO_2) and processes (ALD) that are entirely industry-friendly.

IV. Interlayer Scaling for TG MoS_2 Transistors

In this section, we explore how changing the interfacial (seed layer) thickness affects the top-gate threshold voltage. For the evaporated Si seed layer, we fabricated TG monolayer MoS_2 transistors with Si seed thicknesses of 0.3, 0.4, and 0.7 nm followed by ~5 nm of ALD HfO_2 as TG dielectric.

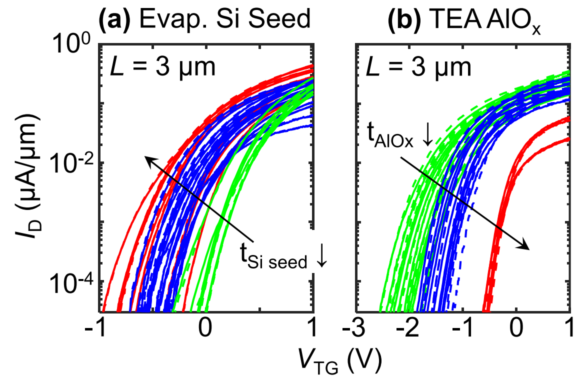

Fig. 11. I_D versus V_{TG} of monolayer MoS_2 transistors at V_{DS} = 0.1 V and V_{BG} = 0 V. (a) Top-gate stack using evaporated Si seed 0.3 nm (red), 0.4 nm (blue), and 0.7 nm (green), followed by ~5 nm HfO_2 as TG dielectric. (b) Top-gate stack using TEA AlO_x 1.5 nm (red), 3 nm (blue), and 6 nm (green), followed by ~6 nm HfO_2 as TG dielectric. Solid and dashed lines represent forward and reverse sweeps, respectively. Despite some variation, a V_T shift is clearly seen (arrows).

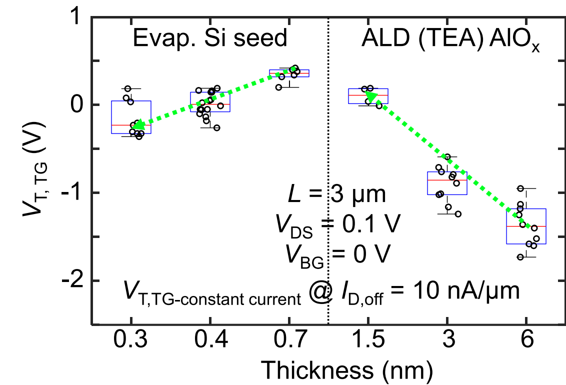

Fig. 12. Box plots summarizing the effect of interfacial layers on top-gate threshold voltage, $V_{T,TG}$, for monolayer MoS_2 transistors from Fig. 11. $V_{T,TG}$ is controlled by the interfacial layer thickness and type, with opposite trends for Si seed (left) and TEA AlO_x (right). $V_{T,TG}$ is extracted at 10 nA/μm constant current, at room temperature. Data points are given small lateral jitter to make them more distinguishable.

For the TEA AlO_x interlayer, top-gated monolayer MoS_2 transistors are fabricated with TEA AlO_x thicknesses of 1.5, 3, and 6 nm followed by ~6 nm of ALD HfO_2 as TG dielectric. Fig. 11 displays the corresponding I_D versus V_{TG} with various $Si(O_x)$ and TEA AlO_x thicknesses, and we observe all devices with negligible hysteresis, owing to the good-quality interlayer dielectrics [18]. In particular, we observe clear changes of the top-gate threshold voltage with scaling the interlayer thickness.

Fig. 12 shows box plots of $V_{T,TG}$ distributions (at 10 nA/μm constant current) from Fig. 11, with some variability observed across each chip, mainly due to the constraints in process control at the multiuser academic fabrication facilities. Comparing the mean values from the box plots, we find that the interfacial (seed) layer thickness and material can control the top-gate threshold voltage, with opposite trends: $V_{T,TG}$ shifts negative when reducing the Si seed, and positive when reducing the AlO_x interfacial layer thickness. This is consistent with the gradual formation of a dipole by such layers with HfO_2 [22], [23], or with positive fixed charges in ultrathin SiO_x and negative fixed charges in ultrathin AlO_x interfacial layers [24], [25]. Although more physical insight must be obtained, these observations represent the first systematic demonstration of V_T control for top-gated 2-D transistors.

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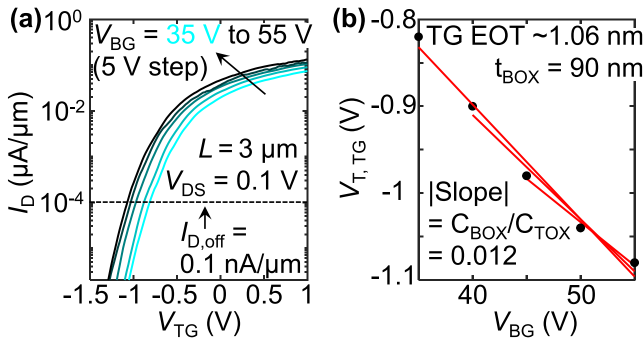

Fig. 13. (a) I_D versus V_{TG} with V_{BG} = 35–55 V with 5 V step on a top-gated monolayer MoS_2 transistor using TEA AlO_x ~1.5 nm followed by ALD HfO_2 ~6 nm as TG dielectric. (b) Corresponding top-gate threshold voltage $V_{T,TG}$ (at 0.1 nA/μm constant current) versus V_{BG}. C_{BOX} and C_{TOX} represent back-gate and top-gate oxide capacitance per unit area, respectively.

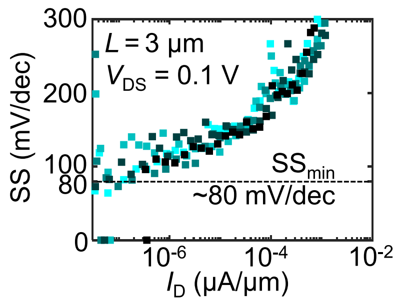

Fig. 14. SS versus I_D from Fig. 13(a). Color of data points corresponds to the color of V_{BG} bias: V_{BG} = 35 V in cyan with a 5 V step up to V_{BG} = 55 V in black. This device reaches SS ≈ 80 mV/dec at room temperature.

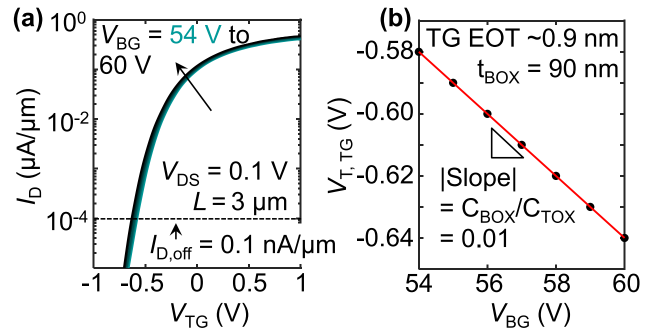

Fig. 15. (a) I_D versus V_{TG} at V_{BG} from 54 to 60 V with 1 V step on a TG MoS_2 transistor using evaporated Si 0.2 nm followed by ALD HfO_2 ~5 nm as TG dielectric. (b) Corresponding $V_{T,TG}$ versus V_{BG} ($V_{T,TG}$ is extracted by constant current at 0.1 nA/μm). C_{BOX} and C_{TOX} represent the back-gate oxide capacitance and top-gate oxide capacitance, respectively.

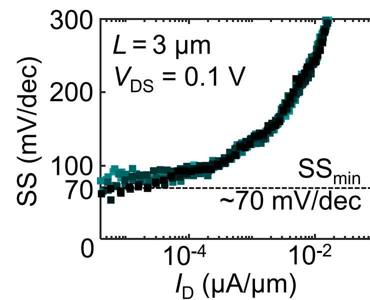

Fig. 16. SS versus I_D from Fig. 15(a). Color of data points corresponds to the color of V_{BG} bias: V_{BG} = 54 V in cyan with a 1 V step up to V_{BG} = 60 V in black. This device reaches SS ≈ 70 mV/dec.

V. Top-Gate EOT Estimates for 2-D Transistors

In this section, we estimate the EOT from the thinnest TG dielectric stack used in each interlayer study: 1) TEA AlO_x ~1.5 nm/ALD HfO_2 ~6 nm and 2) evaporated Si ~0.2 nm/ALD HfO_2 ~5 nm. Due to the difficulty of extracting the top-gate EOT by capacitance-voltage measurements directly on monolayer MoS_2 devices (whose area is too small), we use an estimation method that is widely used in the 2-D TMD literature [9], [10], [13], [26], [27]. Fig. 13(a) shows I_D versus V_{TG} at various V_{BG} (35–55 V with a 5 V step) using TEA AlO_x ~1.5 nm followed by ALD HfO_2 ~6 nm as the TG dielectric on a 3-μm-long MoS_2 transistor. Fig. 13(b) displays the corresponding $V_{T,TG}$ (at 0.1 nA/μm constant current) versus V_{BG} from Fig. 13(a). Here, we note a linear trend, where the magnitude of the slope represents the ratio of the BG oxide capacitance to TG oxide capacitance, because they both control the transistor channel area as parallel plate capacitors from opposite sides. Consequently, the slope magnitude is also the ratio of TG EOT to BG EOT. Because the BG insulator in all our device is 90 nm of SiO_2, we can thus estimate the TG EOT = 1.06 ± 0.12 nm from the magnitude of the slope. This device also achieves top-gate leakage current density $J_{TG} < 3\ \mu A/cm^2$, limited by the instrument noise floor. Fig. 14 shows SS versus I_D from Fig. 13(a), and we achieve SS_{min} ≈ 80 mV/dec owing to the high-quality scaled TEA AlO_x interlayer on MoS_2.

We also extract the top-gate EOT of the monolayer MoS_2 transistor from Fig. 5, which used evaporated Si ~0.2 nm followed by ALD HfO_2 ~5 nm as the TG dielectric. Fig. 15 shows I_D versus V_{TG} at multiple V_{BG} (=54–60 V with 1 V step), and the corresponding $V_{T,TG}$ versus V_{BG}. The magnitude of the slope in Fig. 15(b) once again represents the ratio of the TG EOT to the BG EOT, where the latter is 90 nm of SiO_2. Here, we estimate TG EOT ≈ 0.9 nm from the device in Fig. 5 which also achieves top-gate leakage current density less than 2 $\mu A/cm^2$, limited by the measurement instrument noise floor. Fig. 16 shows SS versus I_D from Fig. 15(a), and we observe the device reaches SS_{min} ≈ 70 mV/dec at room temperature due to the high-quality interface of the evaporated Si seed layer and monolayer MoS_2.

We note there are some considerations to be taken when using the EOT estimation technique described here. When extracting the $V_{T,TG}$, devices can be dominated by contact resistance (R_C) if the contacts are not fully back-gated [28]. To minimize the effect of R_C on threshold voltage, we used only devices with long channels (3-μm-long) for these estimates [29]. Moreover, we measured the devices with high V_{BG} here, which reduces R_C due to contact gating. Note that our estimated EOT is effectively a CET (capacitance equivalent thickness) because it contains a contribution from the TMD channel, which is automatically included in our capacitance-based estimates [30].

Finally, we compare our results in Fig. 17 with other top-gated monolayer MoS_2 devices, showing top-gate leakage current density J_{TG} versus EOT at V_{TG} = 1 V, when both were available. Our results are some of the best achieved to date, showing 1-nm-scale top-gate EOT with low leakage current density and good subthreshold swing. We note that our processes use CMOS-compatible materials, and the AlO_x

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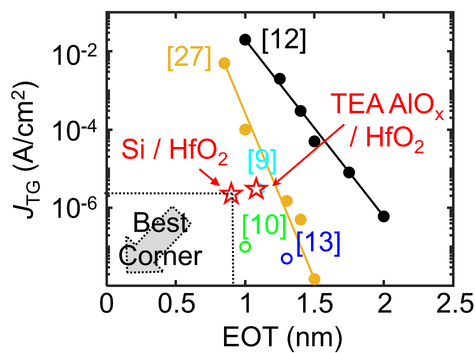

Fig. 17. Benchmarking of top-gate leakage current density (J_{TG}) versus EOT at $V_{TG} = 1$ V from comparable monolayer MoS_2 devices available in the literature [9], [10], [12], [13], [27] and this work (red stars). Unfilled symbols indicate J_{TG} reaching the noise floor of the instrument. Our work is near the "best corner," while using fully CMOS-compatible materials and (for AlO_x seed) industry-friendly processes as well.

interfacial layer (by ALD) is particularly compatible with industry-scale fabrication.

VI. Conclusion

We report top-gated monolayer TMD transistors with ultrathin EOT achieved using industry-friendly approaches. These include evaporated Si and ALD TEA AlO_x interfacial layers, which enable the subsequent ALD of HfO_2. With Si seed, we achieve EOT ≈ 0.9 nm with SS ≈ 70 mV/dec and negligible hysteresis on monolayer MoS_2. (The same approach also enables ambipolar monolayer WSe_2 transistors.) We also show direct ALD of AlO_x using TEA precursor, which enables good uniformity on monolayer MoS_2, providing 1-nm-scale top-gate EOT with SS ≈ 80 mV/dec and negligible hysteresis. Finally, we demonstrate that the top-gate threshold voltage is controllable by the seed layer thickness and type on 2-D transistors for the first time, an essential step toward practical applications.

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