Role of Oxygen Deficiencies on the Stability of Indium Tin Oxide (ITO) Transistors

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***Abstract*— We investigate the threshold voltage (V_T) stability of indium tin oxide (ITO) transistors under positive gate bias stress, comparing the performance of Al_2O_3 and HfO_2 dielectrics. We attribute the unusual negative V_T shift ($\Delta V_T < 0$ V) of our top-gated devices to oxygen scavenging by the dielectric. Notably, devices with Al_2O_3 dielectric achieve median $|\Delta V_T| \leq 10$ mV at room temperature, ~10× lower than devices with HfO_2, highlighting the significant influence of the dielectric layer. We also demonstrate that opposing effects of the top and bottom gates in a dual-gated transistor can be used to attain a median $|\Delta V_T| \approx 150$ mV with 2 V gate stress voltage, at elevated temperature (85°C), which is ~3× lower than the top-gated devices under identical stress conditions.**

***Index Terms*— ITO, transistors, top-gated, dual-gated, dielectric layer, bias stress stability, threshold voltage shift.**

I. Introduction

AMORPHOUS oxide semiconductors like ITO are promising for back-end-of-line memory and logic field-effect transistors (FETs), owing to their low-temperature, large area deposition [1], [2], [3], [4]. However, stability of these FETs is crucial for their practical implementation, with $|\Delta V_T| \leq 30-50$ mV desired up to 85-100°C operating temperature [5]. To achieve this, it is important to understand the factors influencing V_T, based on different process steps [6], [7], [8], [9]. Moreover, depending on device architecture, both positive and negative ΔV_T can occur in oxide transistors under positive bias stress, making the physical origin of the V_T instability complex and difficult to address [7], [10], [11], [12].

Here, we study the effect of top dielectric layer and annealing condition on the positive bias temperature instability (PBTI) of several top-gated (TG) ITO transistors at room temperature. For both positive and negative V_T devices, our results highlight the significance of the dielectric material on device stability under varying bias conditions. Using the most optimized dielectric and annealing conditions, we then perform PBTI measurements on TG and dual-gated (2G) ITO FETs at 85°C to assess their stability under practical operating temperatures. Our investigation helps elucidate the physical mechanisms behind positive and negative V_T shifts in different oxide FET structures.

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II. Fabrication and Measurement

Figs. 1(a, b) show schematics of our top-gated (TG) and dual-gated (2G) ITO transistors, respectively. **Fig. 1(c)** details the fabrication flow [2]. Here, HfO_2 and Al_2O_3 serve as gate dielectrics, deposited using atomic layer deposition with tetrakis(dimethylamido)hafnium (TDMA-Hf) and trimethylaluminium (TMA) as Hf and Al precursors. Oxygen plasma and ozone are used as oxidants for HfO_2 and Al_2O_3 deposition, respectively.

Fig. 1(d) shows a top-view optical image of a TG device and the measure-stress-measure scheme to study PBTI, is shown in **Fig. 1(e)**. The I_D vs. V_{GS} curves are measured before (stress time, $t_{stress} = 0$ s) and after applying a gate stress voltage ($V_{GS,stress}$) for $t_{stress} = 1$, 10, 100, 1000 s cumulatively. V_T is extracted at constant current $= (W/L) \times 100$ nA, where W and L are channel width and length. The V_T shift is defined as the difference between stressed and unstressed V_T after 1000 s stress duration: $\Delta V_T = V_{T,stressed} - V_{T0}$.

III. Results and Discussion

A. HfO_2 versus Al_2O_3 Dielectrics

We first perform PBTI measurements at room temperature (RT). **Figs. 2(a,b)** show the I_D vs. V_{GS} curves of unannealed devices with ~5 nm thick HfO_2 and Al_2O_3 dielectrics, respectively. The device with HfO_2 shows a more negative ΔV_T than the Al_2O_3 device, even considering the higher HfO_2 capacitance ($V_{GS,stress} = 1$ V for HfO_2 and 2 V for Al_2O_3). PBTI usually causes a positive ΔV_T due to electron trapping in the gate dielectric and/or at the channel/dielectric interface.

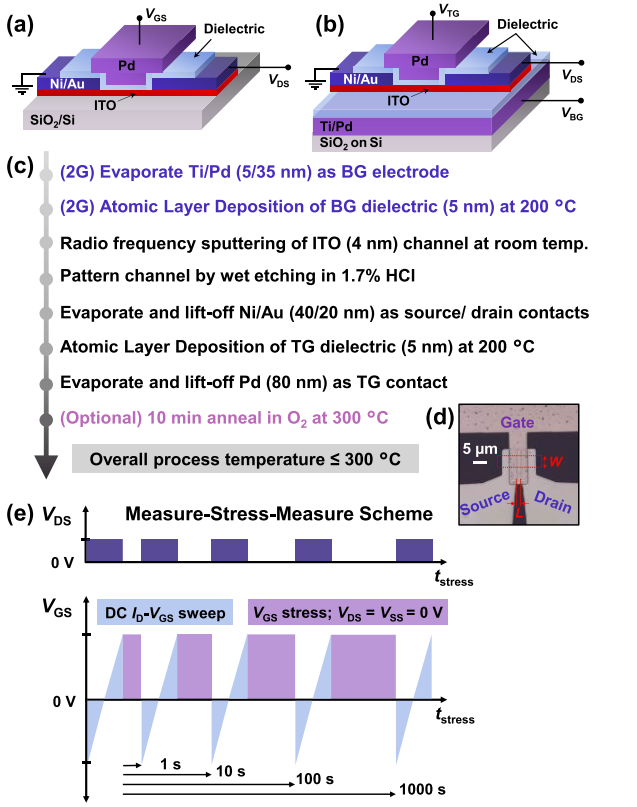

Fig. 1. Schematics of (a) top-gated (TG) and (b) dual-gated (2G) ITO transistors. (c) Detailed fabrication process flow. (d) Top-view optical image of a completed TG device. (e) Schematic of the measure-stress-measure scheme used for positive bias stress analysis. The stress time (t_{stress}) is cumulative over 4 cycles.

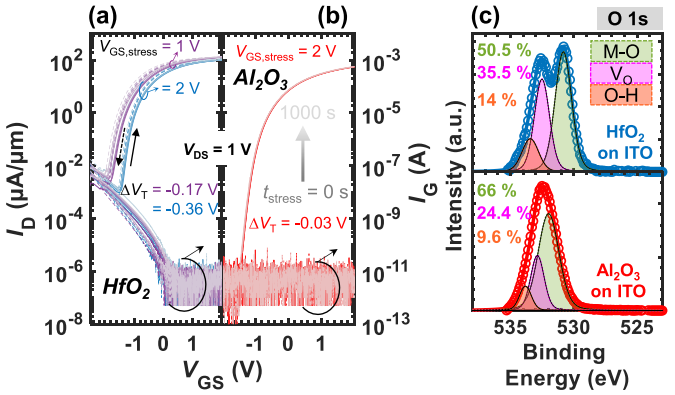

Fig. 2. Measured I_D vs. V_{GS} of representative unannealed top-gated (TG) ITO transistors at room temperature, with ~5 nm thick (a) HfO_2 and (b) Al_2O_3 dielectrics. Solid and dashed curves mark sweep directions, as indicated. All devices have $L \approx 2$ μm channel length. The right-side axis displays the TG leakage, I_G. (c) Measured X-ray photo-electron spectroscopy (XPS) of O 1s binding energy for HfO_2 and Al_2O_3 (both ~5 nm thick) on ITO, indicating high O vacancy (V_O) concentration in the HfO_2 film. V_T is extracted at constant current of $(W/L)\times$100 nA.

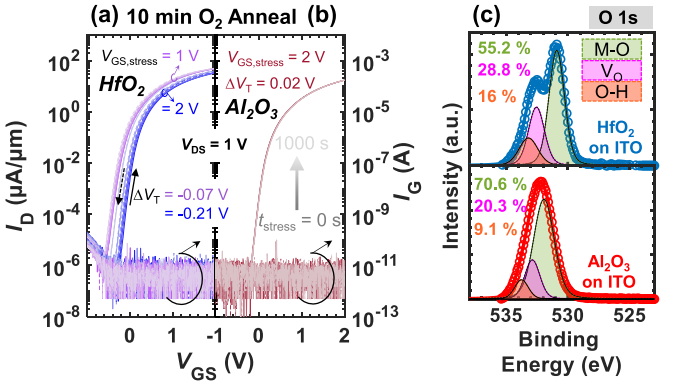

Fig. 3. Measured I_D vs. V_{GS} of representative top-gated (TG) ITO devices at room temperature (RT), with ~5 nm thick (a) HfO_2 and (b) Al_2O_3 dielectrics; both annealed in O_2 at 300 °C for 10 min. Solid and dashed curves mark sweep directions, as indicated. All channels are $L \approx 2$ μm long. The right-side axis monitors the TG leakage, I_G, during the measurement. V_T is extracted at constant current of $(W/L)\times$100 nA. (c) Measured X-ray photo-electron spectroscopy (XPS) of O 1s binding energy for HfO_2 and Al_2O_3 (both ~5 nm thick) on ITO, indicating reduced O vacancy (V_O) concentration after O_2 annealing.

Therefore, such a negative ΔV_T under PBTI is unexpected, and often attributed to hydrogen-related defect migration from dielectric to channel [5]. However, the X-ray photo-electron spectroscopy (XPS) data from the two samples [**Fig. 2(c)**], show a higher oxygen (O) vacancy concentration in HfO_2 [13], [14], [15], [16], indicating that the negative ΔV_T is likely caused by defective HfO_2 film scavenging O from the ITO during PBTI, causing additional O vacancies (*i.e.* electron donors) in the channel and a negative V_T shift.

B. Effect of O_2 Anneal

Figs. 3(a,b) show PBTI for devices with HfO_2 and Al_2O_3 respectively, after annealing in O_2 at 300°C for 10 min. Because the O_2 anneal is performed post-fabrication, it helps passivate O vacancies in the HfO_2 dielectric and causes less O scavenging from the ITO, resulting in improved V_T stability. However, the Al_2O_3 dielectric device still shows smaller $|\Delta V_T|$, indicating the dominant effect of the dielectric itself. **Fig. 3(c)** shows the corresponding XPS data, revealing an expectedly lower O vacancy concentration in both films after O_2 annealing [13], [14], [15], [16].

In **Fig. 4**, we summarize these results by plotting ΔV_T vs. the initial V_{T0} of all devices, accounting for the variability of our processing in an academic nanofabrication facility. The O_2-annealed devices with HfO_2 and Al_2O_3 dielectric display an expected positive shift in V_{T0}. The median ΔV_T of the former under stress is improved from −200 mV to −80 mV for $V_{GS,stress} = 1$ V, and from −565 mV to −210 mV for $V_{GS,stress} = 2$ V, due to the O vacancy passivation in HfO_2. On the contrary, the median ΔV_T of the devices with Al_2O_3 increases upon O_2 annealing (+45 mV) and shows a positive ΔV_T. This indicates the possibility of creating oxygen interstitials in the Al_2O_3 during O_2 anneal and subsequent electron trapping in these defects under positive bias stress [17], [18]. The overall summary plot in **Fig. 4** shows no trend with initial V_{T0} of the device (which results in different overdrive stress) and rather confirms the significant role of the gate dielectric on ΔV_T, *i.e.* device stability.

C. High-Temperature Measurement

Because unannealed devices with Al_2O_3 dielectric show the smallest $|\Delta V_T|$ under PBTI at room temperature, we also measured them at 85°C with different $V_{GS,stress}$ to assess their stability at higher operating temperature. **Fig. 5** shows the I_D vs. V_{GS} measurements under different bias conditions,

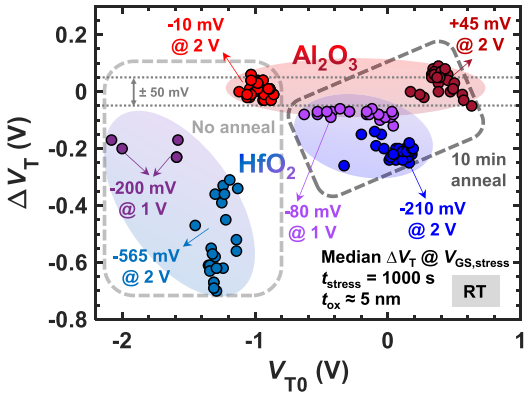

Fig. 4. Summary plot of ΔV_T vs. initial V_{T0} for top-gated ITO transistors, measured at room temperature (RT) after cumulative $t_{stress} = 1000$ s. The median ΔV_T for each sample with 5 to 20 devices is mentioned at the specified gate stress voltage. Here, t_{ox} = gate oxide thickness. V_T is extracted at constant current of $(W/L)\times 100$ nA.

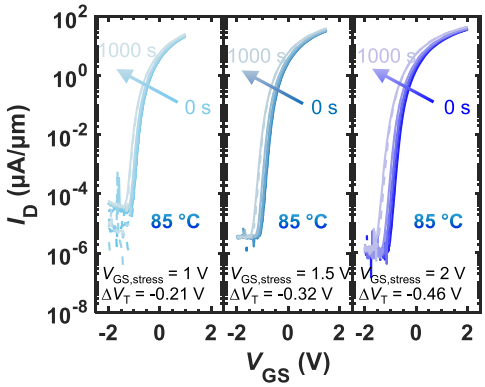

Fig. 5. High-temperature (85 °C) I_D vs. V_{GS} measurements of representative unannealed top-gated ITO devices with Al_2O_3 gate dielectric, at various stress voltages ($V_{GS,stress}$); $L \approx 2$ μm and $V_{DS} = 1$ V for all measurements. V_T is extracted at constant current of $(W/L)\times 100$ nA.

revealing a degraded $|\Delta V_T|$ at 85°C, which could be due to enhanced O scavenging at higher temperature, or thermal ionization of neutral O vacancies releasing electrons [19].

D. Dual-Gated Devices

We also fabricate dual-gated transistors [schematic shown in Fig. 1 (b)] with Al_2O_3 dielectric (for both top- and bottom-gate) and observe an expected improvement of V_T, subthreshold slope (SS) and maximum drive current ($I_{D,max}$) with dual-gate (2G) modulation vs. single-gate control, on the same device [**Fig. 6(a)**]. The plot of V_T shift, ΔV_T vs. stress time, t_{stress} at room temperature [**Fig. 6(b)**] reveals a trend of positive ΔV_T for BG sweep (due to electron trapping; consistent with our previously reported bottom-gated devices [7], [12]) and negative ΔV_T for TG sweep (due to O scavenging by top dielectric; consistent with our top-gated devices). The 2G modulation shows an intermediate ΔV_T, which indicates a balance between the top- and bottom-gate sweeps.

A similar trend is observed for devices measured at 85° [**Fig. 6(c)**], achieving median $|\Delta V_T|$ of 6 devices down to 150 mV even at the 85 °C elevated temperature. This underscores the significant impact of device architecture on bias stress stability. **Fig. 6(d)** illustrates the role of oxide deposition sequence, resulting in more O-rich films in the

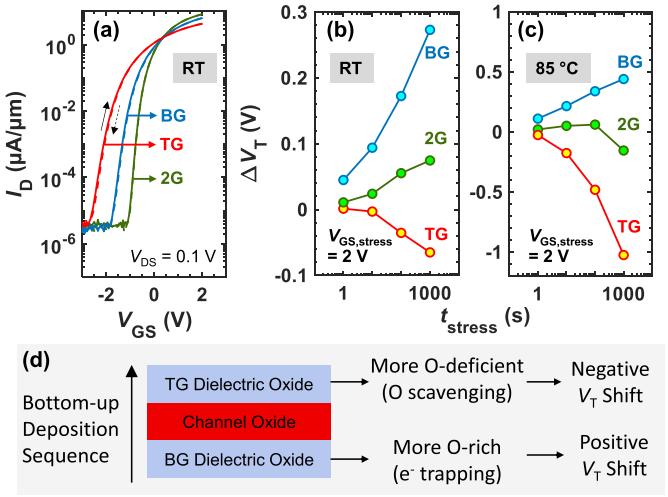

Fig. 6. (a) Room temperature (RT) I_D vs. V_{GS} measurements of the same dual-gated ITO transistor with ~5 nm Al_2O_3 top and bottom dielectric, showing top-gate (TG), bottom-gate (BG) and dual-gate (2G) modulation. Plots of ΔV_T vs. cumulative t_{stress}, showing positive shift for BG, negative shift for TG, and intermediate shift for 2G sweeps, for measurements at (b) RT and (c) 85 °C. The BG, TG and 2G measurements in (b) and (c) are performed on different devices of the same sample. Each symbol in (c) represents the median value of 5-6 devices to account for variability. V_T is extracted at constant current of $(W/L)\times 100$ nA. (d) Illustration of oxide deposition sequence resulting in more O-rich films in the bottom layers and more O-deficient films in the top layers, because bottom layers are exposed to additional O_2 flow during the deposition of top layers. The different film types cause positive vs. negative V_T shifts accordingly.

bottom layers and more O-deficient films in the top layers, because the bottom layers are exposed to additional O_2 flow during the top layer depositions. As a result, the BG dielectric is likely to trap electrons and cause a positive ΔV_T while the TG dielectric is likely to scavenge oxygen from the channel and release electrons, causing a negative ΔV_T. Therefore, the dual-gate structure can be carefully optimized to achieve a low V_T shift by balancing out the effects of the two gates [17].

IV. Conclusion

We conducted a study on the stability of top- and dual-gated ITO transistors, and observed that top-gated devices with Al_2O_3 dielectric exhibited exceptional stability, with $|\Delta V_T| \leq$ 10 mV at room temperature. This stability is likely due to the lower oxygen vacancy concentration in the Al_2O_3 film, which minimizes oxygen scavenging from the channel, resulting in more stable device behavior. In the case of dual-gated devices, our findings suggest that the opposing effects from the two gates could help achieve a $|\Delta V_T| \approx 150$ mV at 85 °C, and this stability may be further enhanced through careful optimization of both gate stacks, indicating the potential for improved performance in dual-gated configurations.

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