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Monte Carlo Simulation of Electrical Transport with Joule Heating and Strain in Monolayer MoS_2 Devices

Maritha A. Wang and Eric Pop*

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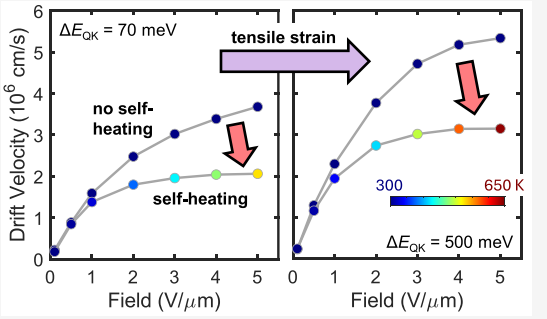
ABSTRACT: Two-dimensional (2D) semiconductors are candidates for future nanoscale (e.g., nanosheet) transistors, wherein high current densities and high-density integration cause self-heating, limiting performance and reliability. Here, we study the effects of self-heating and strain on electrical transport in monolayer MoS_2 using electro-thermal Monte Carlo simulations. Incorporating Joule self-heating with a generalizable thermal resistance model reveals that at high lateral field (~5 V/μm) and high charge carrier density (~10^{13} cm^{-2}), transistor temperatures can increase by more than 200 K in steady state. The electron saturation velocity decreases to 2.1 × 10^6 cm/s with self-heating but can reach 5.3 × 10^6 cm/s at room temperature if self-heating is mitigated and tensile strain is applied to reduce intervalley scattering. Simulations also reveal that electron mean free paths are just 2−3 nm in this high-field regime. These results provide fundamental insights showing that both self-heating and strain must be considered in emerging 2D transistors.



KEYWORDS: *MoS_2, 2D transistor, self-heating, strain, mobility, high-field transport*

Ultrathin transition metal dichalcogenides (TMDs), at the limit of a single layer, have attracted interest for nanoscale devices due to their atomic thinness, van der Waals interfaces, and mechanical strength. For example, such two-dimensional (2D) TMD semiconductors could be scaled beyond conventional silicon devices, which exhibit performance degradation at small dimensions due to increased surface scattering.[1] Recent studies have also suggested that such materials could play a role in three-dimensional (3D) heterogeneous integration of electronics, due to relatively lower synthesis temperatures.[2−4] Thus, it is becoming increasingly important to understand the fundamental limits of electrical transport in TMDs, especially in technology-relevant contexts, including substrates, strain, and temperature rise due to self-heating from device and circuit operation.

Despite relatively good thermal conductivity along the in-plane direction[5] (higher than silicon[6] in nanometer-thin films), common TMDs have relatively high thermal boundary resistance (TBR) at their out-of-plane interfaces[5,7−9] due to weaker van der Waals coupling with adjacent materials. Moreover, TMD transistors are likely to be surrounded by electrical insulators (e.g., SiO_2 or HfO_2)[10,11] which also have low thermal conductivity. As a result, when current flows through an ultrathin TMD transistor channel, the Joule self-heating generated by electron−phonon interactions can lead to significant temperature rise,[9] resulting in performance degradation and reliability concerns. These effects could be exacerbated in technologies like nanosheet transistors,[12−14] where channels are vertically stacked in very tight geometries with many interfaces and high current densities.

Here, we use the semi-classical Monte Carlo method[15−21] to investigate electrical transport in monolayer MoS_2 transistors with Joule self-heating and strain. This approach is well-suited for studying charge transport in semiconductors because it solves the Boltzmann Transport Equation directly and is fast compared to first-principles methods, while including quantum mechanical details like the energy band structure and electron−phonon scattering. Monte Carlo simulations of charge transport couple naturally with studies of thermal behavior because the energy exchanged in electron−phonon scattering events can be summed to yield the Joule heat dissipated. This approach has been previously used to examine self-heating[22] in Si, but not in TMD devices. Here, we simulate electron transport in monolayer MoS_2 including intrinsic (intravalley and intervalley) electron−phonon scattering, tensile strain, and heat loss to the substrate. We also evaluate device structures that allow us to compare our results with existing experimental measurements.[9,23−25] Our simulations are carried out with and without Joule self-heating and (varying

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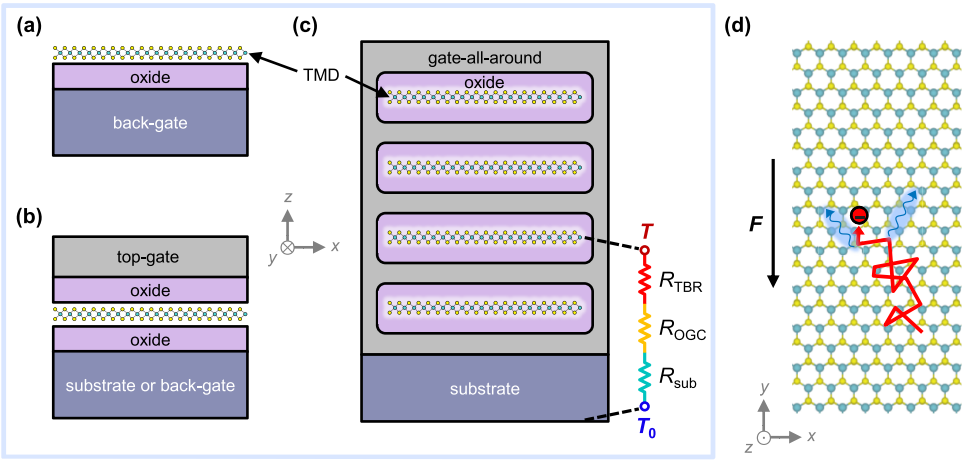

Figure 1. Cross-section schematics along the width of (a) a back-gated transistor,[1,9] (b) a dual-gated transistor,[10] and (c) a gate-all-around nanosheet transistor[13] with monolayer TMD channels, illustrating several use cases and the thermal resistance between the channel and substrate. This includes the thermal boundary resistance between TMD and gate oxide (R_{TBR}), the combined thermal resistance of the oxide, gate stack, and contacts (R_{OGC}), and the substrate thermal resistance (R_{sub}). Current flow is in the y-direction, between source and drain contacts not shown in the cross-section. (d) Top-view schematic of the TMD channel with an electron drift trajectory (red) under the influence of an electric field F and phonon scattering (blue wavy arrows). Left/right boundaries are reflective (v_x becomes $-v_x$), and top/bottom boundaries are periodic here.

levels of) strain, enabling us to place lower and upper bounds on the phonon-limited electron mobility and high-field saturation velocity. This work highlights the importance of incorporating Joule heating and strain in the analysis of emerging TMD transistor technologies.

The heat dissipation path in a transistor can be complex depending on the materials, interfaces, and geometry of the device.[5,26−29] For example, nanoscale dimensions reduce the thermal conductivity of materials,[6,30] while the thermal boundary resistance (TBR or Kapitza resistance) of interfaces[5,8,9] can also become a significant bottleneck. Figure 1a-c shows the cross-section schematics of three transistor geometries, from back-gated (most common for basic charge transport experiments)[1,9] to a future multi-channel nanosheet device.[13] A general thermal resistance model is also shown, which includes the thermal boundary resistance at the TMD-oxide interface (R_{TBR}), the combined thermal resistance of the oxide, gate stack, and contacts (R_{OGC}), and the thermal resistance of the substrate (R_{sub}). Here, R_{OGC} incorporates most of the geometric complexity of the device and can be estimated from measurements[9,29] or from 3D device thermal simulations. R_{OGC} can include the various geometry-dependent device heat dissipation pathways, including contacts and gate stack, and their particular materials. This term can be updated for the specific device layout, allowing us to focus here on the fundamentals of self-heating in the TMD channel without loss of generality. To include Joule self-heating, we simulate electron−phonon scattering during device operation, then use a simplified thermal resistance model to capture the temperature rise, which is self-consistently used to update the scattering rates.

Our Monte Carlo simulation computes the trajectories and scattering of electrons in a monolayer MoS_2 channel, as shown in Figure 1d. This approach is advantageous vs first-principles or finite element methods because the time-dependent electron trajectories are explicitly simulated, incorporating fundamental physical details in the electron−phonon scattering rates, while remaining computationally inexpensive. The details of the general Monte Carlo approach are described elsewhere,[15,31,32] and some choices regarding our implementation (e.g., vs earlier Si work) are given in Supporting Information Section A. Briefly, conduction band electrons are treated as charged particles, freely drifting in the x-y plane of the 2D channel between scattering events. The energy band structure of the 2D semiconductor enters both the drift and scattering calculation, through the effective mass and density of states. The simulation takes place in constant time steps (1 fs), smaller than the shortest scattering time even at the highest temperatures considered. Electrons experience net drift due to the electric field, and at the end of each time step a scattering event (including self-scattering, where no electron−phonon scattering occurs) is selected by drawing a random number.[15,31] When electron−phonon scattering occurs, the energy exchanged with the TMD lattice is tallied (as heat) and the scattering angle is selected at random, isotropically.[15,31] This procedure repeats for the duration of the simulation, and the steady-state electron drift velocity is averaged for a given electric field. The low-field mobility is simply obtained as the ratio of this drift velocity and the magnitude of the field. Joule self-heating is captured by calculating the channel temperature rise from its power dissipation and thermal resistance ($\Delta T = PR_{th}$), while iteratively updating the temperature-dependent scattering rates with the new temperature.[22]

We first simulate charge transport along a MoS_2 channel considering intrinsic electron−phonon scattering without Joule heating. The TA, LA, TO(E'), LO(E'), and A_1 phonons are considered, which have the strongest electron−phonon coupling.[16] Figure 2a shows a schematic of the conduction band structure of monolayer MoS_2. In unstrained MoS_2, the K valley has a degeneracy of 2, and the Q valley has a degeneracy of 6 (the Q valley is sometimes called Λ or I,[33,34] approximately halfway along the Γ-K line[35]). Electrons experience both intravalley (K−K and Q−Q) and intervalley (K−Q) scattering, the latter more likely when the intervalley energy separation ΔE_{QK} is relatively small. Here, we use electron−phonon scattering rates for intravalley and intervalley scattering with deformation potentials and phonon energies reported by Li et al.[16] for ΔE_{QK} = 70 meV (varying this as a function of strain, below). The Monte Carlo simulation parameters are summarized in Supporting Information Section

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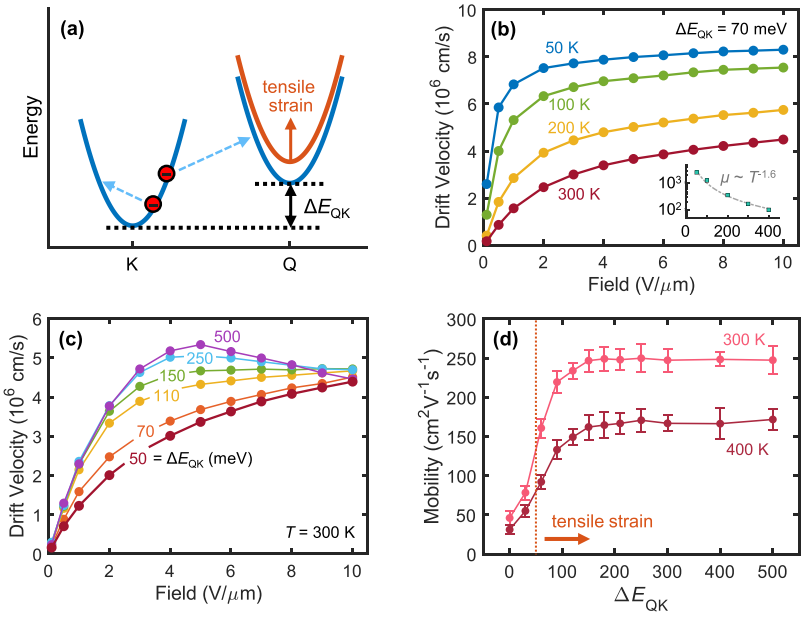

Figure 2. (a) Schematic of the monolayer MoS_2 conduction band. Tensile strain increases the energy separation ΔE_{QK}. Dashed arrows mark electrons undergoing intravalley (K−K) and intervalley scattering (K−Q), here via phonon absorption. (b) Monte Carlo (MC) simulation of phonon-limited drift velocity vs electric field at various temperatures, as labeled. The inset shows the low-field electron mobility ($cm^2V^{-1}s^{-1}$) vs temperature (K) with the dashed line indicating a fit of $\mu \propto T^{-1.6}$. The mobilities at 50 and 100 K (200 and 300 K) are extracted at a field of 0.1 V/μm (0.5 V/μm). (c) MC simulation of phonon-limited drift velocity vs electric field for different ΔE_{QK} values, at 300 K. (d) Low-field electron mobilities vs ΔE_{QK} at 300 and 400 K. Error bars represent standard deviations due to the statistical nature of MC simulations. The vertical dashed line marks a ΔE_{QK} of 50 meV, the lowest bound predicted in the literature at 0% strain, and ΔE_{QK} increases with tensile strain. The mobility saturates for ΔE_{QK} > 150 meV, but the high-field drift velocity benefits with an increased ΔE_{QK}, as shown in panel (c).

B, and details of scattering rate calculations are discussed in Supporting Information Section C.

Effective masses at the K and Q valley minima are taken as $m_c = 0.48m_0$ and $0.57m_0$ respectively,[36] where m_0 is the free electron rest mass. Additionally, because high-field transport reaches higher electron energies, we incorporate a non-parabolicity mass enhancement during electron drift, with $m_{eff} = m_c(1 + 2\alpha E)$, where $\alpha = 2$ eV^{-1} for both K and Q valleys,[20] and E is the kinetic energy referenced to the bottom of the respective valley. (Other work[37] reported $\alpha \approx 1$ eV^{-1}, but we have found using this value makes only a subtle difference in our high-field results, see Supporting Information Section D.) Figure 2b displays the simulated drift velocity vs electric field at various ambient temperatures, with $\Delta E_{QK} = 70$ meV. The figure inset also shows that the low-field mobility decreases as $\mu \propto T^{-1.6}$ when the temperature increases. (For a larger $\Delta E_{QK} = 150$ meV, the low-field mobility decreases as $\mu \propto T^{-1.4}$.) The exponent of this temperature dependence is comparable to the theoretically predicted[38,39] value of −1.70 and falls between experimental[23,40,41] values of −1.1 and −1.9.

Tensile strain is known to increase the ΔE_{QK} valley separation of monolayer TMDs, which was predicted to enhance electron mobility[42,43] by decreasing the intervalley (K-Q) scattering rate. Recent experiments have confirmed that tensile strain in monolayer MoS_2 can lead to between 1.6× to 2× mobility enhancement[44,45] (depending on strain type and magnitude), while biaxial tensile strain in monolayer WS_2 can lead to 2.3× mobility enhancement,[46] even in the presence of some disorder in experimental films. Note that ΔE_{QK} in unstrained monolayer MoS_2 is presently not well-known, with theoretical calculations ranging from 50 to 270 meV,[16−19,41−43,47,48] and an experimental estimate of 110 meV.[49] To account for this range and the effect of tensile strain, we simulate the drift velocity with ΔE_{QK} between 50 to 500 meV in Figure 2c. (Here we raise all six Q valleys equally, which is more representative of biaxial strain, while uniaxial tensile strain may split the Q valleys[42] into degeneracies of 4 and 2, albeit with a relatively small energy difference.)

The drift velocities are sensitive to ΔE_{QK}, i.e., a larger ΔE_{QK} partially suppresses intervalley scattering, because fewer K valley electrons have sufficient energy to scatter into the Q valley. As a result, both the low-field mobility and high-field drift velocity increase when ΔE_{QK} increases. When $\Delta E_{QK} \leq$ 150 meV in Figure 2c, the drift velocities appear to converge at the highest electric fields (>8 V/μm), because sufficient K valley electrons have energies in excess of the valley separation. However, for ΔE_{QK} > 150 meV we observe slight negative differential velocity (NDV) at the highest fields, as electrons access higher regions of the K valley with higher effective mass[18] due to band nonparabolicity. This is somewhat similar to the Gunn effect in GaAs and GaN,[50] however in these materials the NDV is primarily due to the much heavier effective mass of the upper valley.

The simulations carried out here are for electrons in uniform electric fields, at constant temperature and/or constant ΔE_{QK} separation. In nanoscale transistors, the electric field can be very nonuniform,[51] and in strained transistors the strain can also be nonuniform.[52−54] Thus, our simulations cover the *range* of electric fields and strains likely to occur in practical devices. Nanoscale devices may also exhibit quasi-ballistic transport, with some electrons only scattering a few times before exiting the channel. (The phonon-limited electron mean free path for $\Delta E_{QK} = 70$ meV ranges from ∼ 5 nm at low-field to ∼ 3 nm at high-field in our simulations, at room temperature. At lower mobilities, <80 $cm^2V^{-1}s^{-1}$, the mean free path was previously estimated[55] to be <3 nm.) Thus, some electrons may

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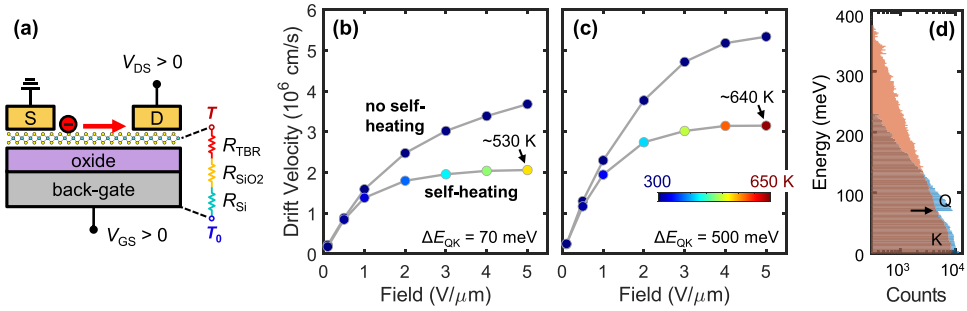

Figure 3. (a) Schematic of a back-gated monolayer MoS_2 transistor. The total thermal resistance includes the thermal boundary resistance of MoS_2 with the oxide (R_{TBR}), the thermal resistance of the gate oxide (R_{SiO2}), and the gate or substrate thermal resistance (R_{Si}). This model can be generalized to other device geometries.[5] (b) Simulated electron drift velocity vs electric field along the channel, for a ΔE_{QK} of 70 meV, with and without Joule self-heating. This represents the case with approximately no strain applied, and significant K−Q intervalley scattering. (c) Drift velocity vs field, for a ΔE_{QK} of 500 meV, with and without Joule self-heating. This represents the case with significant tensile strain applied and K−Q intervalley scattering greatly suppressed. For panels (b) and (c), the initial temperature (T_0) is 300 K and the electron density (n) is 10^{13} cm^{-2}. These panels illustrate the upper and lower drift velocity limits, including both strain and self-heating effects. (d) Simulated electron distribution during high-field transport (5 V/μm), including self-heating, for ΔE_{QK} values of 70 meV (blue) and 500 meV (orange). The zero energy is the K-valley minimum. The arrow marks the Q-valley minimum for the case with ΔE_{QK} of 70 meV. Note the presence of high-energy ("hot") electrons at hundreds of meV, which contribute to high-field transport, heating, and potential reliability concerns.[59]

overshoot the saturation velocity predicted here, as was observed in nanoscale Si transistors;[56] however, many electrons undergo sufficient scattering to render our results relevant even in quasi-ballistic[57] scenarios.

The low-field mobilities at 300 and 400 K for ΔE_{QK} ranging from 0 to 500 meV are shown in Figure 2d. The mobility initially grows rapidly with ΔE_{QK}, but saturates for ΔE_{QK} > 150 meV. We note that the change of ΔE_{QK} with percent strain is not well-known, but estimates range from 90 meV/% uniaxial strain to 150 meV/% biaxial strain for monolayer MoS_2.[17,41] (For monolayer WS_2, estimates range from 86 meV/% uniaxial strain to 169 meV/% biaxial strain.[46]) Over the full range of ΔE_{QK} in Figure 2d, the room-temperature mobility can be enhanced by up to a factor of ∼ 5×, depending on the valley separation before tensile strain is applied. Here, our effective masses and electron−phonon deformation potentials are unscreened and independent of strain, but *ab initio* calculations which take these into account have predicted up to ∼ 8× mobility enhancement may be possible.[41,58]

We next include the effect of Joule self-heating on electron transport, which is relevant in most practical transistors,[9] e.g. when operating at current densities >100 μA/μm on common SiO_2/Si substrates. To pick a concrete case related to existing experimental data,[9,23] we consider the simple thermal resistance of a back-gated transistor, as in Figure 3a. This thermal model can be generalized to include various heat flow paths (e.g., contacts[5,23]) and device geometries (e.g., gate-all-around or nanosheet transistors,[27] see Figure 1a-c). The thermal resistance of a long-channel back-gated transistor is $R_{th} = R_{TBR} + R_{SiO2} + R_{Si}$, where R_{TBR} is the MoS_2/SiO_2 thermal boundary resistance, R_{SiO2} is the thermal resistance of SiO_2, and R_{Si} is the thermal resistance of the Si substrate. With SiO_2 thickness of ∼90 nm and MoS_2/SiO_2 thermal boundary conductance of ∼ 15 $MWm^{-2}K^{-1}$, the area-normalized thermal resistance of the MoS_2 channel at 300 K is $R_{th} \approx 1.34 \times 10^{-7}$ m^2KW^{-1}. This is largely dominated by the (nearly equal) R_{TBR} and R_{SiO2} here, with the Si substrate thermal resistance having <5% contribution for the typical micron-scale devices in previous experiments.[9,23] We note this simple model applies for device dimensions of microns or more (and much greater than the SiO_2 thickness), whereas nanoscale devices require additional considerations, including heat loss to the contacts[5] (Supporting Information Section E).

For a power density P, normalized by the channel area, the steady-state temperature rise is $\Delta T = PR_{th}$. In our simulations, the power dissipated is obtained directly from electron−phonon scattering, as the net sum of phonon emission minus absorption energies,[22] per unit time. The power density can also be related to current flow through $P = qnv_dF$, where q is the elementary charge, n is the per-area electron density, v_d is the drift velocity, and F is the electric field magnitude. (This is equivalent to a total power I_DV_{DS} in a long-channel device, where I_D is the current.) We also iteratively update the temperature-dependent scattering rates with the calculated temperature ($T = T_0 + \Delta T$) at each value of the electric field.

Figure 3b compares the simulated phonon-limited drift velocity for an electron density of $n = 10^{13}$ cm^{-2} with and without Joule heating, at ΔE_{QK} = 70 meV, which corresponds to very small or zero strain applied. Starting with an initial temperature T_0 = 300 K, Joule heating causes a temperature rise $\Delta T \approx 230$ K under high-field transport at 5 V/μm (power density ∼ 1.7 mW/μm^2), with the device geometry considered here. This is equivalent to a temperature rise of ∼ 135 K at 1 mW/μm^2, in good agreement with the experimental measurement[9] of $\Delta T \approx$ 135−150 K in a long-channel monolayer MoS_2 transistor at this power density, with the same back-gate geometry as in our simulations. This self-heating effect, in steady-state, leads to decreased high-field electron drift velocity from 3.7 × 10^6 cm/s to 2.1 × 10^6 cm/s; correspondingly, the high-field electron mean free path drops to ∼ 2 nm.

Because electron transport at a given field depends on ΔE_{QK} (Figure 2c), which is affected by strain, we also investigate the high-field drift velocity at high ΔE_{QK} = 500 meV, with and without Joule self-heating in Figure 3c. (This corresponds to high, ∼ 3% tensile strain assuming ΔE_{QK} changes by ∼ 150 meV/% biaxial strain.[17,41]) At such high ΔE_{QK} the intervalley scattering is strongly suppressed, and electron transport is dominated by K−K intravalley scattering. Starting with an initial temperature T_0 = 300 K, Joule heating causes a temperature rise $\Delta T \approx$ 340 K at 5 V/μm lateral field, which is ∼ 50% greater than in Figure 3b at lower ΔE_{QK} = 70 meV. This occurs because the drift velocity is nearly 50% higher (3.1

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$\times 10^6$ cm/s vs 2.1 $\times 10^6$ cm/s), while keeping n and F the same. If self-heating is entirely eliminated, the high-field drift velocity can reach up 5.3 $\times 10^6$ cm/s in this scenario (Figure 3c), with the assistance of suppressed intervalley scattering at high ΔE_{QK}. Figure 3d shows the corresponding electron energy distribution at high field, with self-heating, for ΔE_{QK} = 70 meV and ΔE_{QK} = 500 meV. For the latter case, we observe that electrons reach higher energies when intervalley scattering is suppressed, which explains the higher v_{sat} seen in Figure 3c.

Table 1. Comparison of the Monolayer MoS_2 Saturation Velocities from This Work and Experimental Studies[a]

Reference	Saturation velocity v_{sat} (cm/s)
this work	2.1−5.3 $\times 10^6$
23	3.4 $\times 10^6$
24	5−7 $\times 10^6$
25	0.98 $\times 10^6$
63	3.8 $\times 10^6$
64	1.1 $\times 10^6$

[a]The lower (upper) range in our simulations includes (excludes) self-heating and considers low (high) ΔE_{QK}. We note that experimental studies automatically include material defects and strain (from fabrication) as well as self-heating effects, unless the authors explicitly tried to reduce or account for self-heating.[23,24]

We also wish to compare the saturation velocities calculated in Figures 3b,c with the few experimental studies at high fields. Smithe et al.[23] estimated $v_{sat} \approx 3.4 \times 10^6$ cm/s for electrons in monolayer MoS_2, at room temperature, after accounting for self-heating with high-field measurements at lower ambient temperature. Nathawat et al.[24] obtained a higher $v_{sat} \approx 5-7 \times 10^6$ cm/s with 4 ns voltage pulses, which limited both self-heating and electron trapping. The agreement with the range suggested by our Monte Carlo approach is good, but we recall that experimental MoS_2 samples tend to have defects and impurities, imperfectly controlled strain, as well as some uncertainty about their carrier density. These factors can lead to experimental estimates[25] (i.e., $v_{sat} \approx 0.98 \times 10^6$ cm/s) below our predicted range. Table 1 compares the present work with experimental estimates of the electron v_{sat} in this material.

While self-heating is known to limit current flow for 2D transistors in direct-current (DC) operation,[9,60] devices working at GHz frequencies and/or in digital switching with low duty cycle will heat up less when their on-state time is shorter than their thermal time constant. For reference, the thermal time constant of 2D material devices ranges between 30 to 300 ns, depending on the thickness and type of layers surrounding the channel,[61] because the 2D monolayer contributes negligible thermal capacitance. Ultrathin silicon-on-insulator (SOI) devices were also found to experience less self-heating in high frequency operation than in DC operation due to thermal time constants around 100 ns.[62]

In summary, we used Monte Carlo simulations to study the effects of Joule self-heating and strain in monolayer MoS_2 transistors, particularly during high-field operation. Tensile strain increases the K-Q valley energy separation and enhances the electron mobility by up to ∼ 5×, but this effect saturates for ΔE_{QK} > 150 meV. In contrast, larger tensile strains continue to increase the saturation velocity, until K-Q intervalley scattering is entirely suppressed. In this limit, the electron v_{sat} can reach >5.0 $\times 10^6$ cm/s, at 300 K, corresponding to a current density >1.3 mA/μm at electron densities which can be achieved in practice.[10,60] When self-heating is included in DC operation, the device temperature can rise by over 230 K, and the high-field drift velocity is reduced by over 40%. Because our simulations include only intrinsic phonon scattering, the higher predicted drift velocities (with no self-heating and extreme strain) represent upper bounds. In contrast, the lower values (with extreme self-heating and ∼ 0% strain) are likely lower bounds, because self-heating is overestimated in DC operation and because practical, nanoscale devices are expected to include strain,[53] and to benefit from heat loss to contacts.[5]

This approach can also be extended to analyze other 2D semiconductors or hole transport. Finally, while our simulations are in a long-channel regime of uniform high-field, self-heating is expected to play a role even in very short, ∼ 10 nm scale quasi-ballistic transistors[57] because the electron mean free path is estimated to be ∼ 3 nm during high-field transport (∼2 nm with self-heating). Future studies could incorporate factors relevant for nanoscale gate-all-around transistors including both the electrical and thermal effects of contacts, charged impurity scattering, as well as scattering by 'remote phonons' (interface plasmon-phonon scattering),[65] with practical gate insulators like HfO_2.[10] The latter may introduce a trade-off between additional scattering and lower direct self-heating, with some heat being generated not in the MoS_2 channel but in the surrounding dielectric (i.e., indirect heating).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.4c05254.

Additional simulation details (including simulation parameters and scattering rate calculation), band nonparabolicity analysis, and discussion of device lateral heat dissipation (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Eric Pop − *Department of Electrical Engineering and Department of Applied Physics, Stanford University, Stanford, California 94305, United States; Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0000-0003-0436-8534; Email: epop@stanford.edu

Author

Maritha A. Wang − *Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, United States;* orcid.org/0009-0002-6160-5030

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.4c05254

Notes

The authors declare no competing financial interest.

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Supporting Information

Monte Carlo Simulation of Electrical Transport with Joule Heating and Strain in Monolayer MoS_2 Devices

Maritha A. Wang[1] and Eric Pop[1,2,3,*]

[1] *Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305, USA.*

[2] *Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA.*

[3] *Department of Applied Physics, Stanford University, Stanford, CA 94305, USA.*

**Contact: epop@stanford.edu*

Section A. Monolayer MoS_2 Monte Carlo Simulation vs. Si-based Monte Carlo Simulation

The simulation code used in this study was developed from the ground up, inspired by earlier work which studied Joule heating in Si using Monte Carlo simulations[1] (Ref. [22] in our main manuscript text). The Si simulations included analytic expressions of the electron band structure (with and without strain) and phonon dispersion, while the electron-phonon scattering rates were numerically calculated in the deformation potential formalism, accounting for intravalley and intervalley scattering.[2,3] Multiple electrons were concurrently simulated (in the Ensemble Monte Carlo Method, EMC), for which statistics can be collected (e.g. the drift velocity v_d) when the simulation is run for a sufficiently long time. The EMC can also be employed to calculate the spatial distribution of heat generated in a device.[4,5] Joule heating of the Si lattice was accounted for by tallying the energy exchange between electrons and the lattice during the electron-phonon scattering processes, and the final energy (heat) dissipation rates were reported.

In the present work, to simulate electron transport with strain and self-heating in two-dimensional (2D) devices, we calculated the electron-phonon scattering rates for monolayer MoS_2 using the deformation potentials and phonon energies previously reported[6] (Ref. [16] in the main text). The electron energy bands in the K- and Q-valleys are analytically captured by effective masses and non-parabolicity parameters (described in the main text, with more details provided below), and treating the Q-K energy separation (E_{QK}) as an input parameter affected by strain. Simulations track individual electrons (in the Single-Particle Monte Carlo Method) and, similar to the Ensemble Monte Carlo Method, good statistics can be collected when the simulation is run for a sufficiently long time. As in the earlier Si work, self-heating is incorporated here by tracking the energy exchange between the electrons and lattice, such that Joule heating is the sum of all phonon energies emitted minus those absorbed, per unit time. Going beyond the earlier Si work, we estimate the temperature rise (ΔT) during device operation for a specific carrier density, as $\Delta T = PR_{th}$, where P is the power dissipated and R_{th} is the thermal resistance of the transistor, as described in the main text.

Section B. Monte Carlo Simulation Parameters

Parameter	Symbol	Value
Electron effective mass (m_c)	m_K	$0.48m_0$
	m_Q	$0.57m_0$
Non-parabolicity	α	2 eV^{-1}
Mass density	ρ	3.1×10^{-6} kg/m^2
Sound velocity	v_s	6.6×10^3 m/s
Deformation potentials (D)	$D_{ac}^{K\to K}(\Gamma)$	4.5 eV
	$D_{op}^{K\to K}(\Gamma)$	5.8×10^{10} eV/m
	$D_{ac}^{K\to K'}(\mathrm{K})$	1.4×10^{10} eV/m
	$D_{op}^{K\to K'}(\mathrm{K})$	2.0×10^{10} eV/m
	$D_{ac}^{K\to Q}(\mathrm{Q})$	9.3×10^{9} eV/m
	$D_{op}^{K\to Q}(\mathrm{Q})$	1.9×10^{10} eV/m
	$D_{ac}^{K\to Q}(\mathrm{M})$	4.4×10^{10} eV/m
	$D_{op}^{K\to Q}(\mathrm{M})$	5.6×10^{10} eV/m
	$D_{ac}^{Q\to Q}(\Gamma)$	2.8 eV
	$D_{op}^{Q\to Q}(\Gamma)$	7.1×10^{10} eV/m
	$D_{ac}^{Q\to Q'}(\mathrm{Q})$	2.1×10^{10} eV/m
	$D_{op}^{Q\to Q'}(\mathrm{Q})$	4.8×10^{10} eV/m
	$D_{ac}^{Q\to Q'}(\mathrm{M})$	2.0×10^{10} eV/m
	$D_{op}^{Q\to Q'}(\mathrm{M})$	4.0×10^{10} eV/m
	$D_{ac}^{Q\to Q'}(\mathrm{K})$	4.8×10^{10} eV/m
	$D_{op}^{Q\to Q'}(\mathrm{K})$	6.5×10^{10} eV/m
	$D_{ac}^{Q\to K}(\mathrm{Q})$	1.5×10^{10} eV/m
	$D_{op}^{Q\to K}(\mathrm{Q})$	2.4×10^{10} eV/m
	$D_{ac}^{Q\to K}(\mathrm{M})$	4.4×10^{10} eV/m
	$D_{op}^{Q\to K}(\mathrm{M})$	6.6×10^{10} eV/m
Phonon energies (E_{ph})	$E_{op}(\Gamma)$	49.5 meV
	$E_{ac}(\mathrm{K})$	26.1 meV
	$E_{op}(\mathrm{K})$	46.8 meV
	$E_{ac}(\mathrm{Q})$	20.8 meV
	$E_{op}(\mathrm{Q})$	48.1 meV
	$E_{ac}(\mathrm{M})$	24.2 meV
	$E_{op}(\mathrm{M})$	47.5 meV

Table S1. For the deformation potentials (D), the superscript denotes the electron transition. The intravalley scattering transitions are K→K and Q→Q. For intervalley scattering, primed final valleys denote scattering between degenerate valleys (K→K' and Q→Q'). The subscript denotes the type of phonon involved in the transition ('op' for optical and 'ac' for acoustic). The momentum of the phonon involved in the transition is specified in parentheses. For the phonon energies (E_{ph}), the subscript denotes the type of phonon, and the phonon momentum is specified in parentheses. Deformation potentials and phonon energies are from [6] (Ref. [16] in the main text). The electron rest mass is m_0.

Section C. Electron-Phonon Scattering Rates

Eq (1) gives the *intravalley* acoustic phonon scattering rate[6]:

$$\frac{1}{\tau_1} = \frac{m_c D^2 k_B T}{\hbar^3 \rho v_s^2}. \quad (1)$$

Here, k_B is the Boltzmann constant, T is the absolute temperature, $\hbar$ is the reduced Planck constant, and the deformation potential D, as well as other inputs, are defined in **Table S1** above.

Eq (2) gives the *intravalley* optical phonon scattering rate as well as the *intervalley* (both acoustic and optical phonon) scattering rates.[6] These scattering rates have an energy dependence through the onset of phonon absorption and emission in the brackets, and the ΔE_{QK} valley separation:

$$\frac{1}{\tau_2} = \frac{g_d m_c D^2}{2\hbar\rho E_{ph}} [N_{ph}\Delta_1 + (N_{ph}+1)\Delta_2]. \quad (2)$$

Here g_d is the degeneracy of the final valley, $E_{ph} = \hbar\omega_{ph}$ is the phonon energy (from **Table S1**), and $N_{ph} = \{\exp[E_{ph}/(k_B T)] - 1\}^{-1}$ is the phonon occupation. In Eq (2), the first term in the brackets corresponds to phonon absorption and the second term corresponds to phonon emission, where Δ_1 and Δ_2 are Heaviside functions including the energy onset of phonon absorption and emission, respectively. When the intervalley separation ΔE_{QK} changes (e.g. due to strain), the scattering rates in Eq (2) are modified by adjusting Δ_1 and Δ_2.

For example, for an electron scattering between K → Q valleys by phonon *absorption*, scattering can only occur when $E + E_{ph} > \Delta E_{QK}$, where E is the electron energy with respect to the K valley. This condition is accounted for by adjusting the Heaviside function in Eq (2) such that $\Delta_1 = \Theta(E - \Delta E_{QK} + E_{ph})$. Similarly, for K → Q valley scattering by phonon *emission*, $\Delta_2 = \Theta(E - \Delta E_{QK} - E_{ph})$. The Heaviside functions for other electron transitions can be similarly constructed.

Section D. The Role of Band Non-Parabolicity

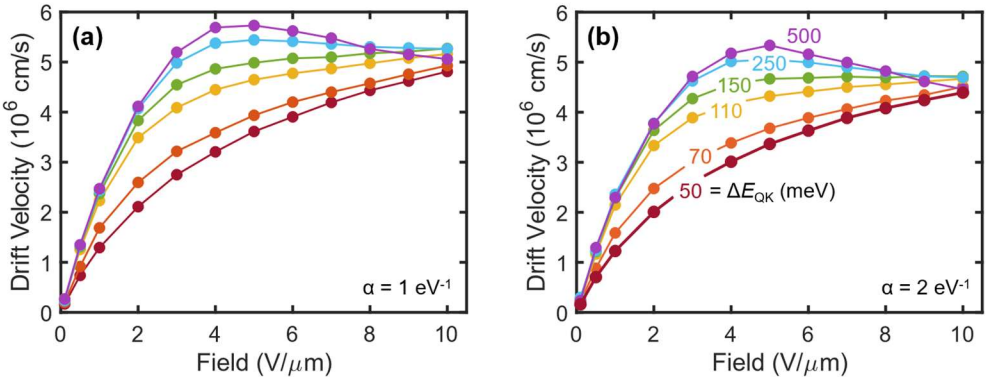


Figure S1. Monte Carlo simulation of phonon-limited drift velocity vs. electric field in monolayer MoS_2, for different ΔE_{QK} at 300 K considering a non-parabolicity factor of **(a)** α = 1 eV^{-1} and **(b)** α = 2 eV^{-1}, where **(b)** is reproduced from **Fig. 2c** in the main text. The ΔE_{QK} labels in **(b)** apply to both plots, which share the same color scheme.

As α increases, the electron effective mass $m_{eff} = m_c(1+2\alpha E)$ grows more rapidly with energy resulting in a heavier effective mass that reduces the electron group velocity v_g, which is given in Eq (3). This

results in ~8% larger high-field drift velocity in **Figure S1(a)**, where α is reduced to 1 eV^{-1}, compared to **Figure S1(b)**.

$$v_g(E) = \sqrt{\frac{2E}{m_c}}\sqrt{\frac{1+\alpha E}{1+4\alpha E(1+\alpha E)}} \quad (3)$$

Section E. Lateral Heat Dissipation

We note there are multiple length scales for the electronic and thermal behavior of transistors based on 2D semiconductors. These are roughly separated by the electron mean free path in monolayer MoS_2 (2-5 nm), the phonon mean free path[7] in monolayer MoS_2 (~100 nm), the electrostatic scale length[8] [$\approx (\epsilon_{ch} t_{ch} t_{ox}/\epsilon_{ox})^{1/2}$], and the thermal healing length [L_H, eq. (5) below]. Here, ϵ and t are the permittivity and thickness of the respective material layer, and the subscripts 'ch' and 'ox' refer to the MoS_2 channel and gate oxide, respectively. The electrical and thermal contact resistance[7,9] (between MoS_2 channel and metal contacts) can also influence heat generation and heat spreading, respectively.

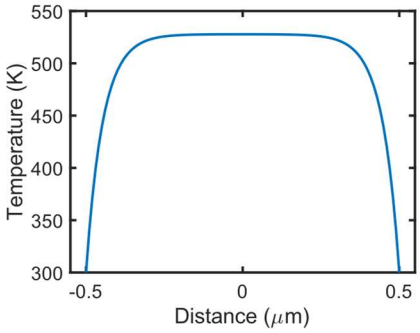
In the main text of our manuscript (**Figure 3a**), we used the simplest thermal resistance model for long-channel devices, which accounts only for heat dissipation to the substrate. This is sufficient for channel lengths $L \gg 3L_H$. At shorter channel lengths, heat dissipation to the contacts can be captured as a first approximation (under steady-state conditions) by assuming perfect heat sinking at the source and drain [$T(\pm L/2) = T_0$, where L is the channel length], and the temperature profile[10] is given by:

$$T(x) = T_0 + PR_{th}\left(1 - \frac{\cosh\left(\frac{x}{L_H}\right)}{\cosh\left(\frac{L}{2L_H}\right)}\right) \quad (4)$$

$$L_H = \sqrt{R_{th} k_{ch} t_{ch}}. \quad (5)$$

Here, P is the area-normalized power density [$= I_D V_{DS}/(LW)$ if the electrical contact resistance, R_C, can be neglected, and W is the channel width], R_{th} is the area-normalized (vertical) thermal resistance, k_{ch} is the in-plane thermal conductivity of monolayer MoS_2 on an SiO_2 substrate,[7] t_{ch} is the thickness of monolayer MoS_2, and x is the distance along the channel, with the channel midpoint at $x = 0$.

The temperature profile along a 1 μm long channel and the relevant parameters are shown in **Figure S2**. Here, R_{th} is the thermal resistance of the MoS_2 channel used in the main text (including the MoS_2-SiO_2 thermal boundary resistance, the thermal resistance of 90 nm of SiO_2, and a small thermal spreading resistance into the Si substrate) and P is the power density in **Figure 3b** in the main text.



Parameter	Value
T_0	300 K
P	1.7 mW/μm^2
R_{th}	1.34×10^{-7} m^{2}K/W
L	1 μm
k_{ch}	33 Wm^{-1}K^{-1}
t_{ch}	6.15×10^{-10} m

Figure S2. (Left) Estimated temperature profile $T(x)$ along a 1 μm long monolayer MoS_2 transistor, with 'lateral' heat dissipation to the metal contacts (here, assumed to be perfect heat sinks) and 'vertical' heat dissipation to the substrate, as described in the main text. (Right) Table listing the parameters used. Other scenarios where the electrical and thermal contact resistance were included in nanomaterial devices have been treated by Pop, Liao, and Gabourie.[7,11,12]

We note that k_{ch} above was slightly modified (from its value for 'long' monolayer MoS_2 on SiO_2) based on the work of Gabourie *et al*.[7] for a 1 μm channel, and can be further reduced in shorter channels,[7] to account for quasi-ballistic heat flow. This simple model estimates $L_H \approx 52$ nm for the geometry considered here, which is the lateral length scale of heat sinking from the channel into the metal contacts (seen as the 'drop' in temperature near the contacts in **Figure S2**). This signifies that for channel lengths of even ~0.25 μm and above, the simpler model in the main text (which includes only 'vertical' heat sinking) is sufficient to estimate the average temperature of the MoS_2 channel.

For shorter-channel devices, especially those shorter than L_H, numerous complexities appear, including the thermal resistance of the contacts themselves[7,11,12] and a non-uniform heat generation profile, which depends on the electrostatic scale length and the transistor operating regime (i.e. linear vs. saturation). In sub-10 nm channel devices there are also quasi-ballistic electron transport effects, which are natively captured by the Monte Carlo simulation, but must be self-consistently coupled with a similar treatment of phonons,[4,13] a task which is the subject of future work. Outside the transistor channel, the device geometry and layout ultimately determine how heat is spread, which can be described with three-dimensional finite-element thermal simulations.[14] For simpler geometries, this heat spreading term can be reduced to an effective R_{th}, as we have done in **Figure 3a** of our main manuscript text.

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